SapphireSOC FAE Training

国产化中高端FPGA领军厂商 —— 加速您的创芯！

易灵思(深圳)科技有限公司

2022-02-23

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版本

日期	版本	版本描述
2022/02/23	V1.0	初稿

主要内容

- SapphireSOC Features
- 在IPM里自定义SOC IP
- SapphireSOC 软件开发环境搭建
- SapphireSOC 软硬件开发实例

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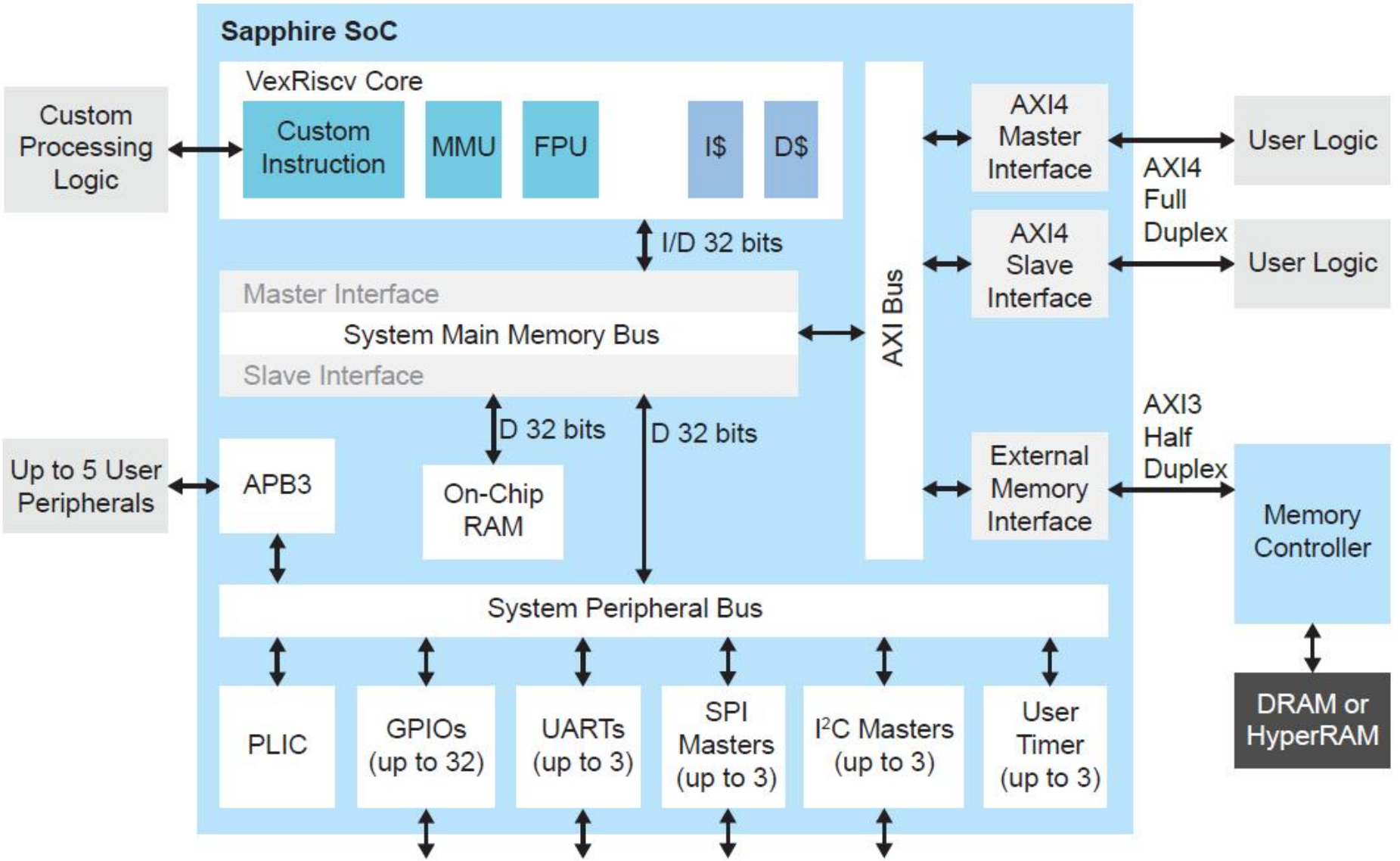
SapphireSOC

——Features

SapphireSOC Core Block Diagram



SapphireSOC Core Feature

- VexRiscv processor with 5 pipeline stages (fetch, decode, execute, memory, and write back), interrupts and exception handling with machine mode
- Up to 1.05DMIPS/MHz (Dhrystone)
- 20 - 400 MHz system clock frequency
- 4 - 512 KB on-chip RAM with boot loader for SPI flash
- Memory controller for DDR or HyperRAM memories
  - Supports memory module sizes from 4 MB to 3.5 GB
  - User-configurable external memory bus frequency
  - 1 half duplex AXI3 interface (up to a 256-bit) to communicate with the external memory
  - 400 MHz DDR clock frequency, 800 Mbps
  - 200 MHz HyperRAM clock frequency, 400 Mbps
- Up to 2 AXI master channels for user logic SapphireSOC Core Feature
- 1 AXI slave channel to user logic

SapphireSOC Core Feature

- Includes a floating point unit
- Includes an optional Linux memory management unit
- Includes a custom instruction interface with 1,024 IDs to perform different functions
- Supports optional RISC-V extensions such as atomic and compressed
- APB3 peripherals:
  - Up to 32 GPIOs
  - Up to 3 I2C masters
  - Clint timer
  - PLIC
  - Up to 3 SPI masters with a maximum clock frequency of 25 MHz
  - Up to 3 user timers
  - Up to 3 UARTs with 115,200 baud

配置 VS 参考资源 – 钛金FPGA

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FPGA	Cache	External Memory	Custom Instruction	FPU	Logic/ Adders	FlipFlops	Memory Blocks	DSP48 Blocks	fMAX (MHz)
Ti60 F225 C4	No	No	No	No	4,489	3,018	12	4	268
	No	No	Yes	No	4,555	3,065	12	4	268
	No	Yes	No	No	7,118	7,527	46	4	333
	No	Yes	Yes	No	7,111	7,567	46	4	308
	Yes	No	No	No	5,004	3,630	24	4	280
	Yes	No	Yes	No	5,129	3,667	24	4	295
	Yes	No	No	Yes	11,707	7,900	44	13	276
	Yes	Yes	No	No	7,716	8,155	58	4	280
	Yes	Yes	Yes	No	7,772	8,197	58	4	295
	Yes	Yes	No	Yes	14,250	12,417	79	13	276

注：参照《Sapphire RISC-V SoC Data Sheet V2.0》

配置 VS 参考资源 – Trion FPGA

FPGA	Cache	External Memory	Custom Instruction	FPU	Logic Utilization (LUTs)	Memory Blocks	fMAX (MHz)
T120 F576 C4	No	No	No	No	5,969	16	110
	No	No	Yes	No	6,176	16	113
	No	Yes	No	No	11,242	50	93
	No	Yes	Yes	No	11,234	50	97
	Yes	No	No	No	6,893	35	106
	Yes	No	Yes	No	7,031	35	117
	Yes	No	No	Yes	16,400	47	85
	Yes	Yes	No	No	12,113	69	107
	Yes	Yes	Yes	No	12,267	69	106
	Yes	Yes	No	Yes	21,743	87	87

注：参照《Sapphire RISC-V SoC Data Sheet V2.0》

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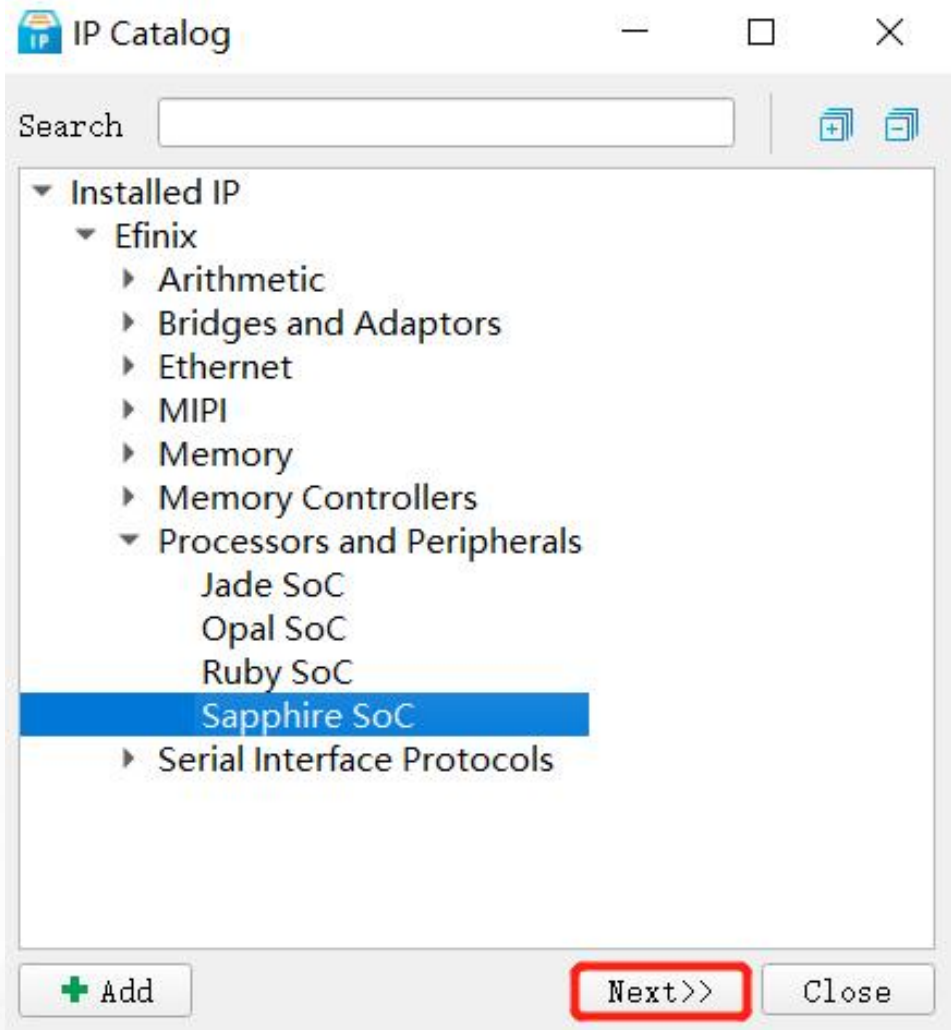
SapphireSOC

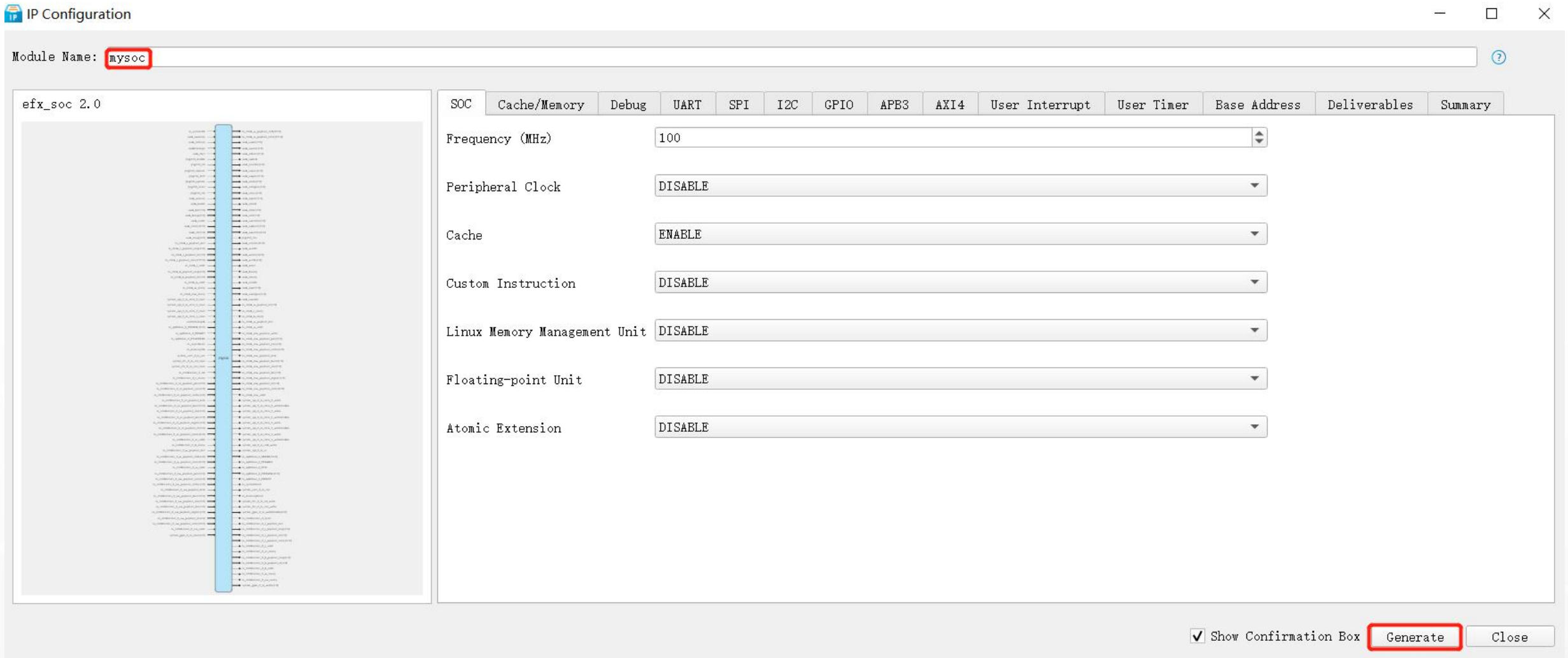
——在IPM里配置SOC IP

SapphireSOC IPM

- 安装Efinity 2021.2.323.1.8
  - https://pan.baidu.com/s/1Pre8xNGhYez6yzLI9IGiYA?pwd=1234
- 安装Java JRE 8
  - https://pan.baidu.com/s/1YcJPO55m8mf3R-l8-5FdPg?pwd=1234



SapphireSOC IPM



SapphireSOC IPM - SoC Tab

Parameter	Options	Description
Frequency (MHz)	20 - 400	Enter the frequency in MHz. Default: 100
Peripheral Clock	DISABLE, ENABLE	Choose whether you want to run a dedicated clock for the APB3 slaves (SPI, I2C, GPIO, UART, and user timer) and AXI4 slave.
Peripheral Clock Frequency (MHz)	20 - 200	Enter the peripheral clock frequency in MHz.
Cache	DISABLE, ENABLE	Choose whether you want to include I$ and D$ caches.
Custom Instruction	DISABLE, ENABLE	Choose whether to enable the custom instruction interface.
Linux Memory Management Unit	DISABLE, ENABLE	Choose whether to enable the Linux MMU.
Floating-point Unit	DISABLE, ENABLE	Choose whether to enable the FPU.
Atomic Extension	DISABLE, ENABLE	Choose whether to enable atomic extension instruction support. If you enable the Linux MMU, this option must be enabled and is turned on by default.
Compressed Extension	DISABLE, ENABLE	For cacheless configurations only, choose whether to enable compressed instruction support.

SapphireSOC IPM - Cache/Memory Tab

Parameter	Options	Description
Data Cache Way	1, 2, 4, 8	Choose the number of ways for the data cache. Default: 1
Cache Size	1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 32 KB	Choose the size of the data cache. Default: 4 KB
Instruction Cache Way	1, 2, 4, 8	Choose the number of ways for the instruction cache. Default: 1
Cache Size	1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 32 KB	Choose the size of the instruction cache. Default: 4 KB
External Memory AXI3 Interface	ENABLE, DISABLE	ENABLE: Instantiate the AXI3 interface. DISABLE: Do not use the AXI3 interface.
External Memory AXI3 Data Width	32, 64, 128, 256	Choose the data width for the AXI3 interface. Default: 128
External Memory AXI3 Address Size	4 MB, 8 MB, 16 MB, 32 MB, 0.5 GB, 1 GB, 1.5 GB, 2 GB, 2.5 GB, 3 GB, 3.5 GB	Choose the address size for the AXI3 interface. Default: 3.5 GB
On-Chip RAM Size	1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 24 KB, 32 KB, 48 KB, 64 KB, 80 KB, 96 KB, 128 KB, 144 KB, 160 KB, 192 KB, 224 KB, 256 KB, 384 KB, 512 KB	Choose the size of the internal BRAM. Default: 4 KB

SapphireSOC IPM – Debug Tab

Parameter	Options	Description
Soft Debug Tap	DISABLE, ENABLE	Choose whether you want to include a soft debug TAP for debugging. DISABLE: Default. The SoC uses the JTAG User TAP interface block to communicate with the OpenOCD debugger. ENABLE: The SoC has a soft JTAG interface to communicate with the OpenOCD debugger. You need to use this setting if you want to use the soft JTAG interface instead of the JTAG User TAP.
Target OpenOCD	Trion T120 BGA324 Development Board Trion T120 BGA576 Development Board Trion T20 BGA256 Development Board Xyloni Titanium Ti60 F225 Development Kit Custom	Chose which board you want to target with OpenOCD. Choose **Custom** to target your own board.
Custom Target OpenOCD	-	Enter the name of your board.
OpenOCD Debug Mode	Turn on by default Turn off by default	Choose whether you want software applications to run in debug mode by default or not. See Debug with the OpenOCD Debugger on page 27 for more details.

SapphireSOC IPM – UART/SPITab

Parameter	Options	Description
UART *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
UART *n* Interrupt ID	1 - 25	Choose the interrupt ID for the UART. The IDs default to: UART 0: 1 UART 1: 2 UART 2: 3

Parameter	Options	Description
SPI *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
SPI *n* Interrupt ID	1 - 25	Choose the interrupt ID for the SPI. The IDs default to: SPI 0: 4 SPI 1: 5 SPI 2: 6

SapphireSOC IPM –I2C/GPIO Tab

Parameter	Options	Description
I2C *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
I2C *n* Interrupt ID	1 - 25	Choose the interrupt ID for the I^2C. The IDs default to: I2C 0: 8 I2C 1: 9 I2C 2: 10

Parameter	Options	Description
GPIO *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
GPIO *n* Pin Width	1, 2, 4, 8, 16	Choose the number of pins for the GPIO. Default: 8
GPIO *n* Interrupt ID 0	1 - 25	Choose the interrupt ID for the I2C. The IDs default to: GPIO 0: 12 GPIO 1: 14
GPIO *n* Interrupt ID 1	1 - 25	Choose the interrupt ID for the I2C. The IDs default to: GPIO 0: 13 GPIO 1: 15

SapphireSOC IPM – APB3 Tab

Parameter	Options	Description
APB Slave Address Size	4 KB - 1 MB	Choose the APB slave size. This setting applies to all APB slaves.
APB3 *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.

SapphireSOC IPM – AXI4 Tab

Parameter	Options	Description
AXI Master	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
AXI Slave Size	1 KB, 2 KB, 4 KB, 8 KB, 16 KB, 32 KB, 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB, 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB, 256 MB	Choose the size of the AXI slave.
AXI Master *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
AXI Master *n* Data Width	32, 64, 128	Choose the width of the AXI master. Do not specify an AXI master width that is larger than the external memory data width.

SapphireSOC IPM – User Interrupt

Parameter	Options	Description
User *n* Interrupt	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
User *n* Interrupt ID	1 - 25	Choose the interrupt ID. The defaults are: User 0 Interrupt: 16 User 1 Interrupt: 17

SapphireSOC IPM – User Timer Tab

Parameter	Options	Description
User Timer *n*	ENABLE, DISABLE	ENABLE: Instantiate the interface. DISABLE: Do not use the interface.
User Timer *n* Counter Width	12, 16, 32	Choose the user timer bit width. Default: 12
User Timer *n* Prescaler Width	8, 16	Choose the prescaler bit width. Default: 8
User Timer *n* Interrupt ID	1 - 25	Choose the interrupt ID. The defaults are: User Timer 0: 19 User Timer 1: 20 User Timer 2: 21

SapphireSOC IPM – Base Address Tab

Parameter	Options	Description
Address Assignment Method	AUTO, Manual	AUTO: Automatically assign an address to the enabled peripherals. Manual: The user can assign addresses to the enabled peripherals.
External Memory Base Address	–	Displays the base address. You cannot change it.
AXI Slave Base Address	–	Displays the base address when the **Address Assignment Method** is set to AUTO. When the **Address Assignment Method** is **Manual**, enter the base address value. The wizard automatically rounds the value to 16 MB aligned addresses during IP generation. For example, 0x41234567 is rounded to 0x41000000.
Peripheral and IO Base Address	–	
UART*n* Address Offset	–	Displays the base address when the **Address Assignment Method** is set to AUTO. When the **Address Assignment Method** is **Manual**, enter base address value. The wizard automatically rounds the value to 4 KB aligned addresses during IP generation. For example, 0x4123 is rounded to 0x41000.
SPI*n* Address Offset	–	
I2C*n* Address Offset	–	
GPIO*n* Address Offset	–	
User Timer*n* Address Offset	–	
APB3*n* Address Offset	–	Displays the base address when the **Address Assignment Method** is set to AUTO. When the **Address Assignment Method** is **Manual**, enter base address value. The wizard automatically rounds the value to APB sized aligned addresses during IP generation. For example, if the APB size is 64 KB, 0x23456 is rounded to 0x20000.
On-Chip RAM Base Address	–	Displays the base address. You cannot change it.

SapphireSOC IPM – 定义mysoc

- 主频： 50MHz
- OCR： 8KB
- Debug： SoftTAP
- UART： Enable UART 0
- SPI： Enable SPI 0
- I2C： Disable All

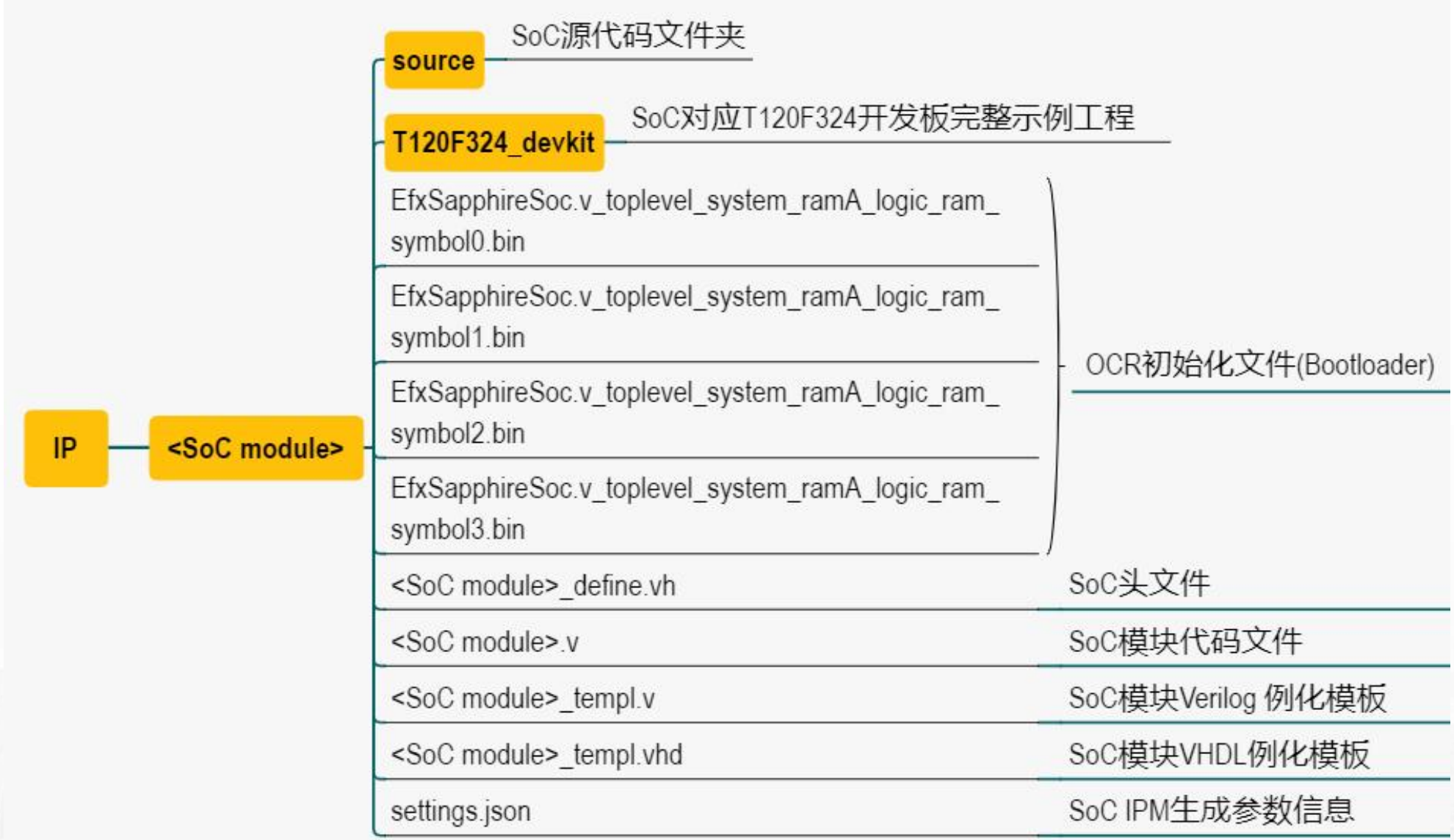
- GPIO： Bit Width = 4
- APB3： Disable
- AXI4： Enable AXI slave
  Disable All AXI Masters
- Interrupt： Enable Interrupt 0
- User Timer： Disable All

- 其他保持默认

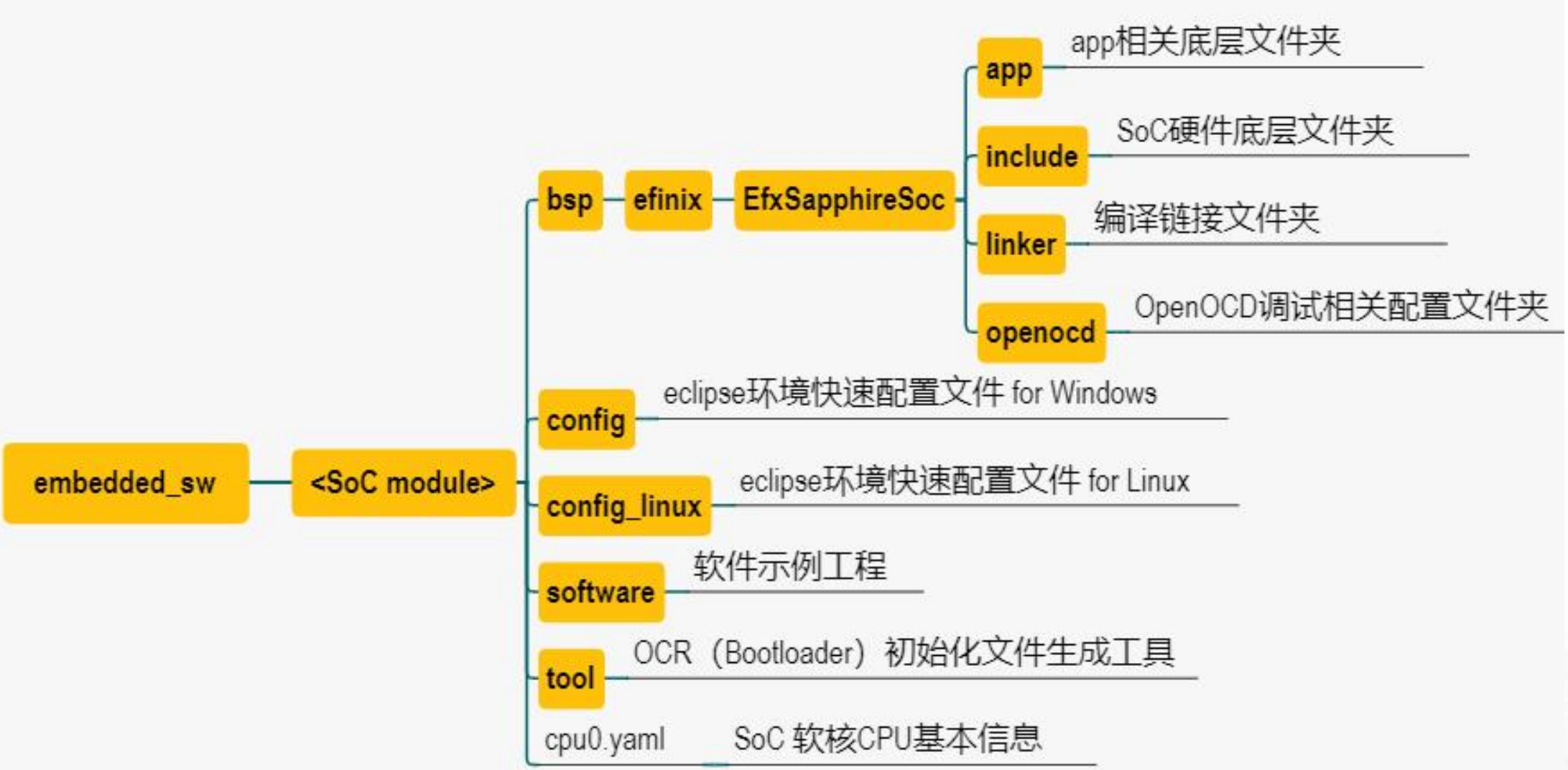
SapphireSOC IPM – 生成IP

- <Project>/embedded_sw文件夹
  - 对应配置的嵌入式软件开发包
- <Project>/IP/<SoC module>文件夹
  - 对应配置的SOC模块代码和开发板的完整示例工程

<Project>/IP/<SoC module>文件夹



<Project>/embedded_sw文件夹



SapphireSOC IPM – 编译硬件工程

- T120F324 Devkit示例工程编译结果

Periphery Resource	
DDR	1 / 1
GPIO	6 / 38
JTAG User TAP	0 / 4
LVDS RX	6.0 / 26
LVDS TX	0 / 20
MIPI RX	0 / 2
MIPI TX	0 / 2
PLL	2 / 7

Core Resources	
Inputs	149 / 1108
Outputs	232 / 1263
Clocks	3 / 16
Logic Elements	10040 / 112128
Memory Blocks	66 / 1056
Multipliers	4 / 320

Interface	
Missing Interface Pins	17
Unassigned Core Pins	0

Timing	
Worst Negative Slack (WNS)	2.001 ns
Worst Hold Slack (WHS)	0.086 ns
io_systemClk	69.091 MHz
io_memoryClk	125.013 MHz
io_jtag_tck	77.984 MHz

SapphireSOC

——软件开发环境搭建

准备工作

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- 安装Efinity 2021.2.323.1.8
  - https://pan.baidu.com/s/1Pre8xNGhYez6yzLI9IGiYA?pwd=1234
- 安装Java JRE 8
  - https://pan.baidu.com/s/1YcJPO55m8mf3R-l8-5FdPg?pwd=1234
- 安装SDK 1.4
  - https://pan.baidu.com/s/1-EpVn9OAYUD_r0XBbQgMPw?pwd=1234

软件开发环境搭建

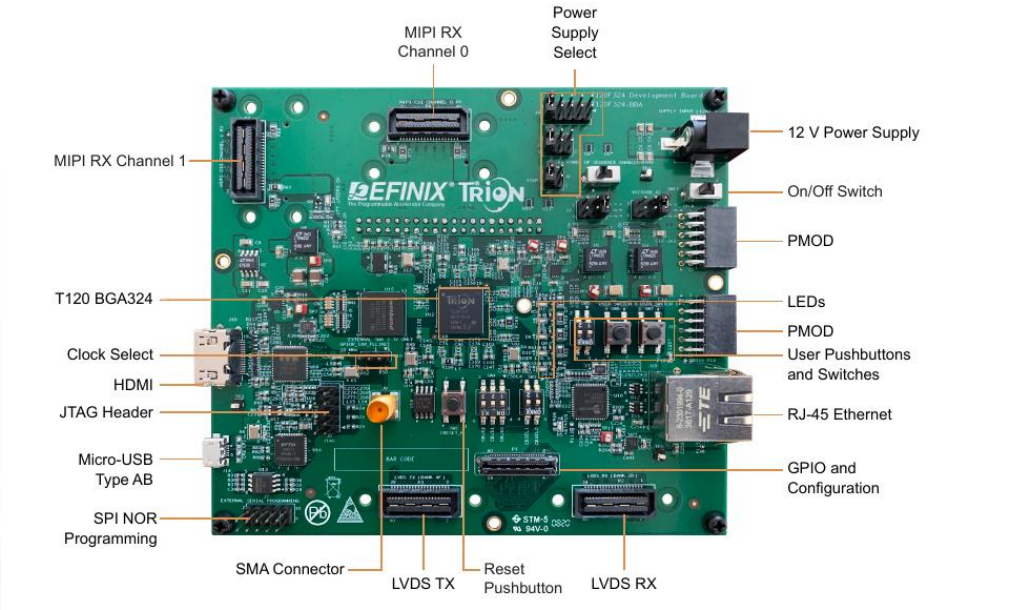
- 参照《Sapphire RISC-V SoC Hardware and Software User Guide》第5章到第7章
  - Eclipse 工作环境设置
  - 新建工程
  - 导入项目设置信息
  - 设置debug编译开关
  - 第一次编译
  - 导入debug配置信息
  - 调整debug配置信息

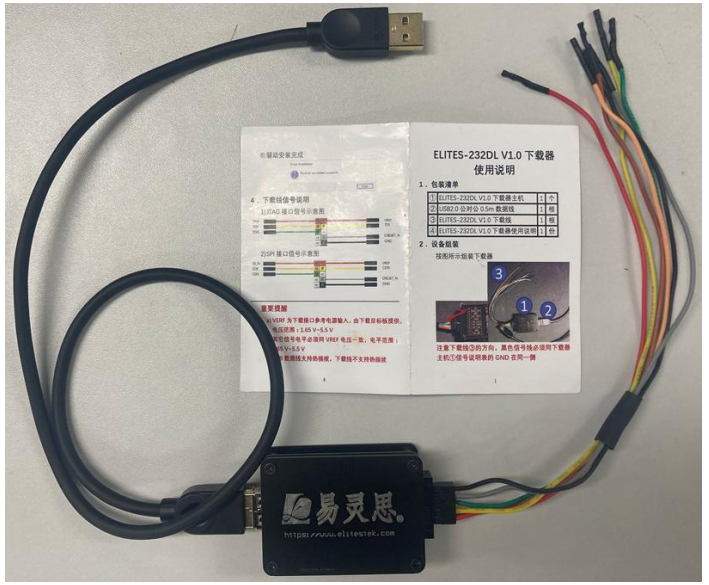
SapphireSOC

——软硬件开发实例

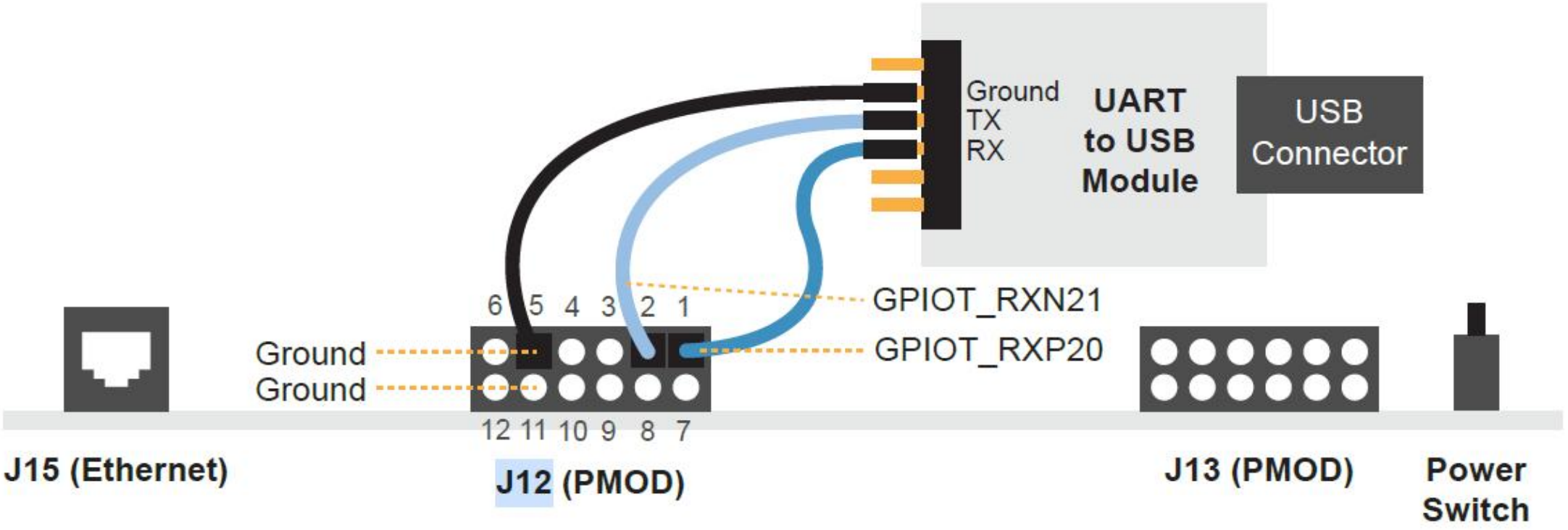
准备工作

- T120F324BBA Devkit一套
- Elites-232DL电缆一根
- USB串口电缆一根

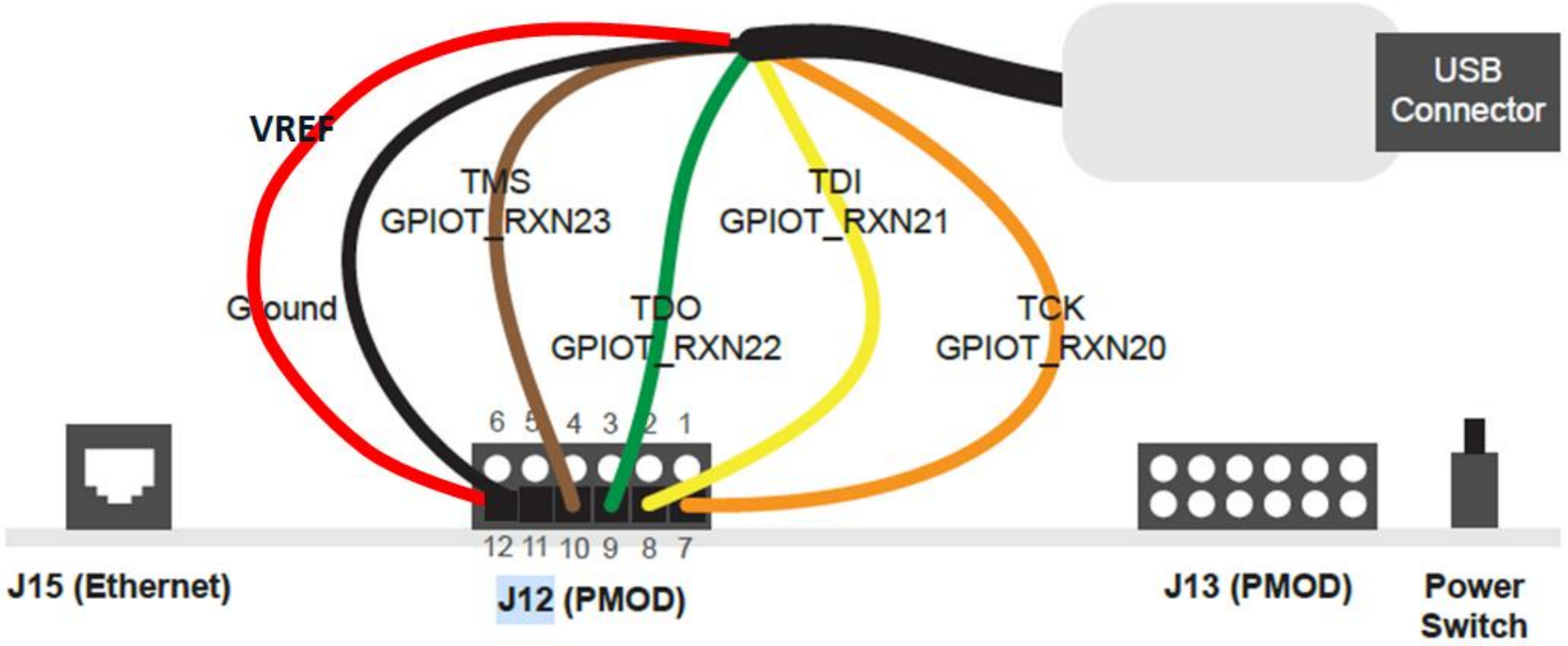




T120F324 Devkit串口连接



T120F324 Devkit softTAP连接



使用OPEN OCD进行Debug

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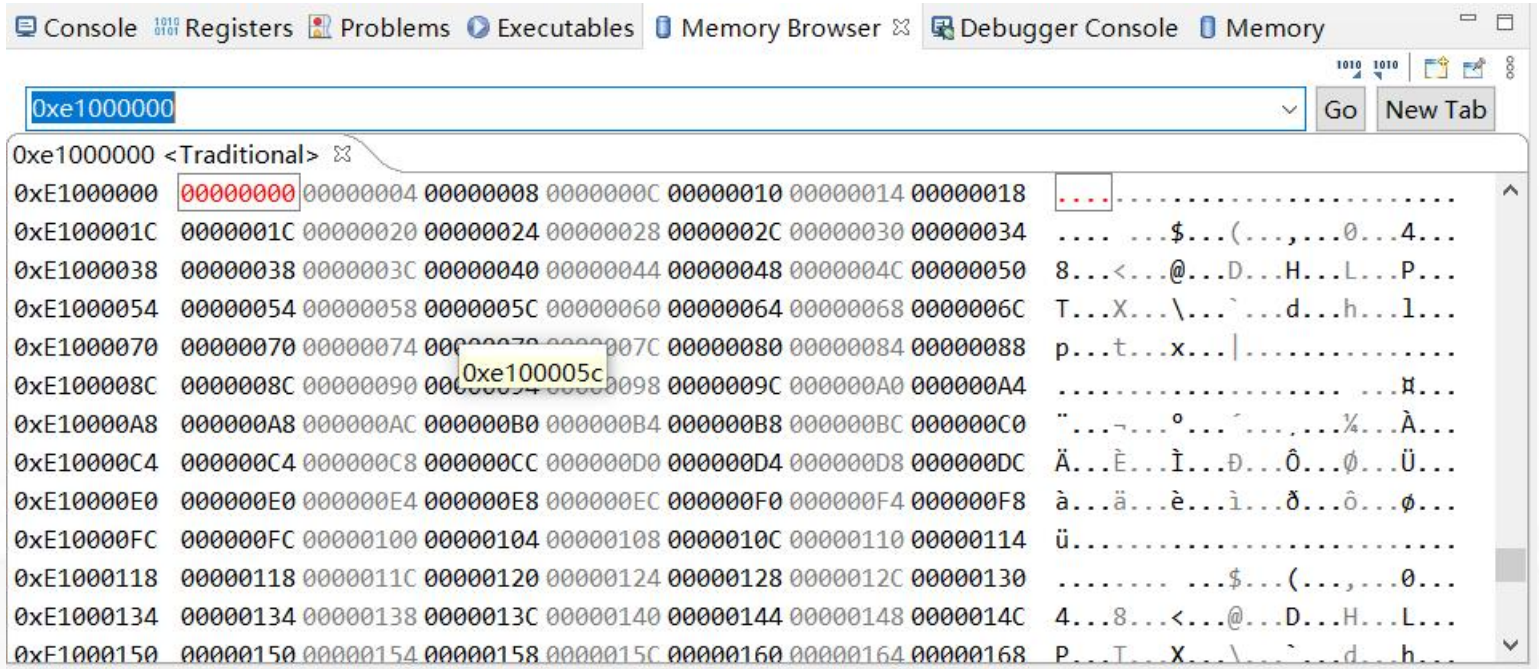
COM9

```
axi4 slave demo !
Passed!
axi4 slave interrupt demo !
Entered AXI Interrupt Routine, Passed!
```



修改Bootloader常见操作

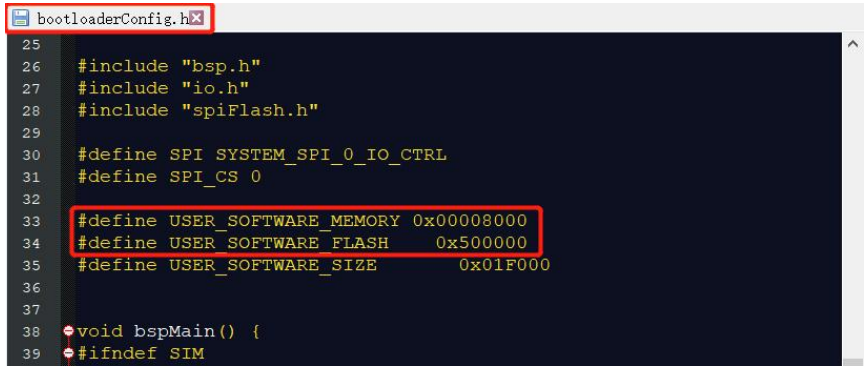
- 修改APP运行(DDR3)地址
  - USER_SOFTWARE_MEMORY
- 修改APP在FLASH的存储地址
  - USER_SOFTWARE_FLASH
- 修改APP的大小
  - USER_SOFTWARE_SIZE

bootloaderConfig.h

```
20  //  LIABILITY, WHETHER IN AN ACTION OF CONTRA
21  //  OUT OF OR IN CONNECTION WITH THE SOFTWARE
22  //  SOFTWARE.
23  //*-------------------------------------------
24  #pragma once
25
26  #include "bsp.h"
27  #include "io.h"
28  #include "spiFlash.h"
29
30  #define SPI_SYSTEM_SPI_0_IO_CTRL
31  #define SPI_CS 0
32
33  #define USER_SOFTWARE_MEMORY 0x00001000
34  #define USER_SOFTWARE_FLASH    0x380000
35  #define USER_SOFTWARE_SIZE       0x01F000
36
```

制作自己的Bootloader

- 修改APP在FLASH的存储地址
  - 0x380000->0x500000
- 修改APP运行(DDR3)地址
  - 0x00001000->0x00008000



- 编译bootloader工程，生成bootloader工程的bin文件
- 使用tool/binGen.py生成OCR初始化bin文件
- 将生成的OCR初始化文件覆盖硬件工程目录下的bin文件
- 重新编译FPGA硬件工程

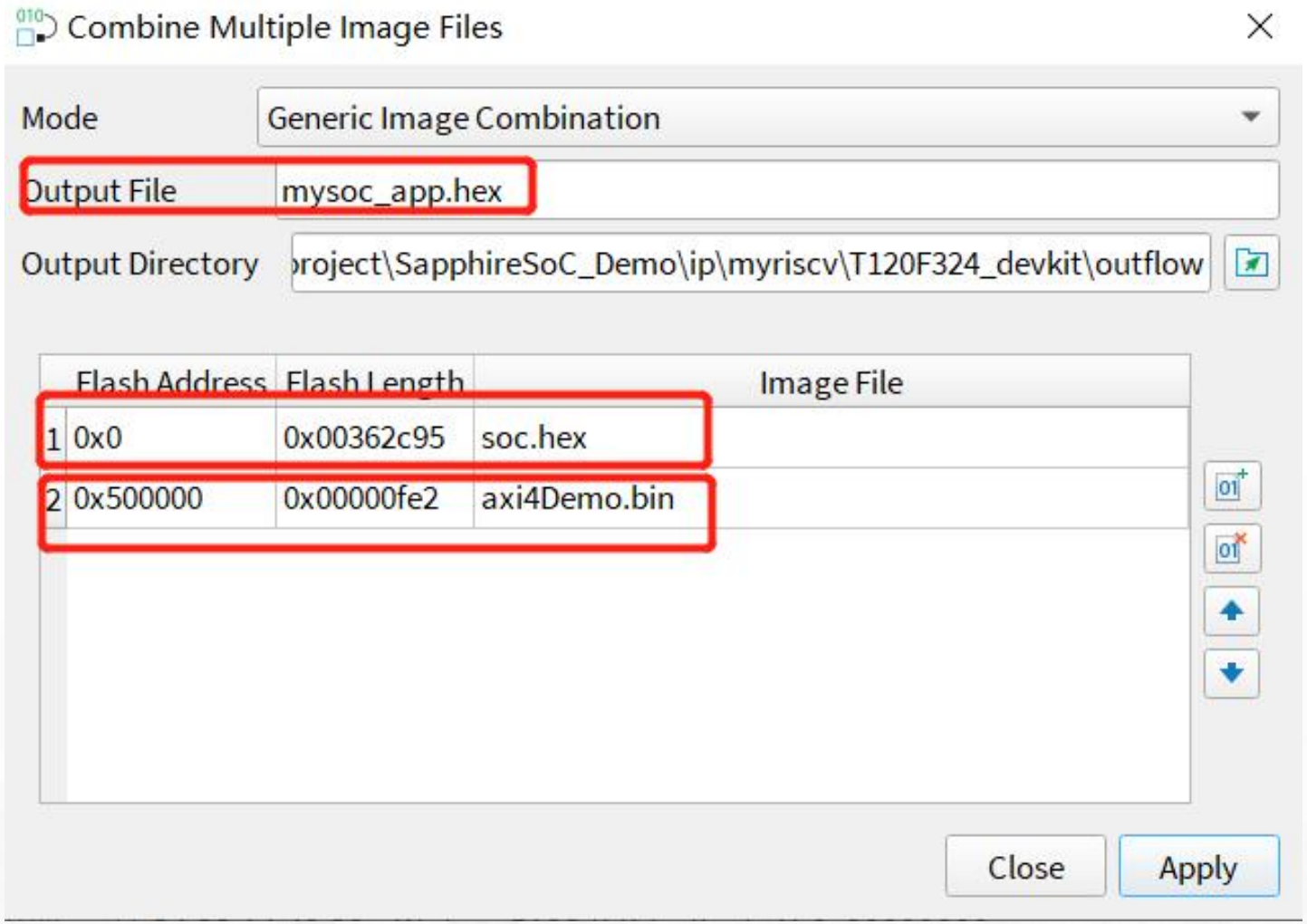
修改APP运行地址和APP程序大小限制

- 修改APP运行地址
  - ORIGIN = 0x00001000 => 0x00008000
- 修改APP程序大小限制
  - LENGTH = 124K（默认）
- 重新编译AXI4Demo

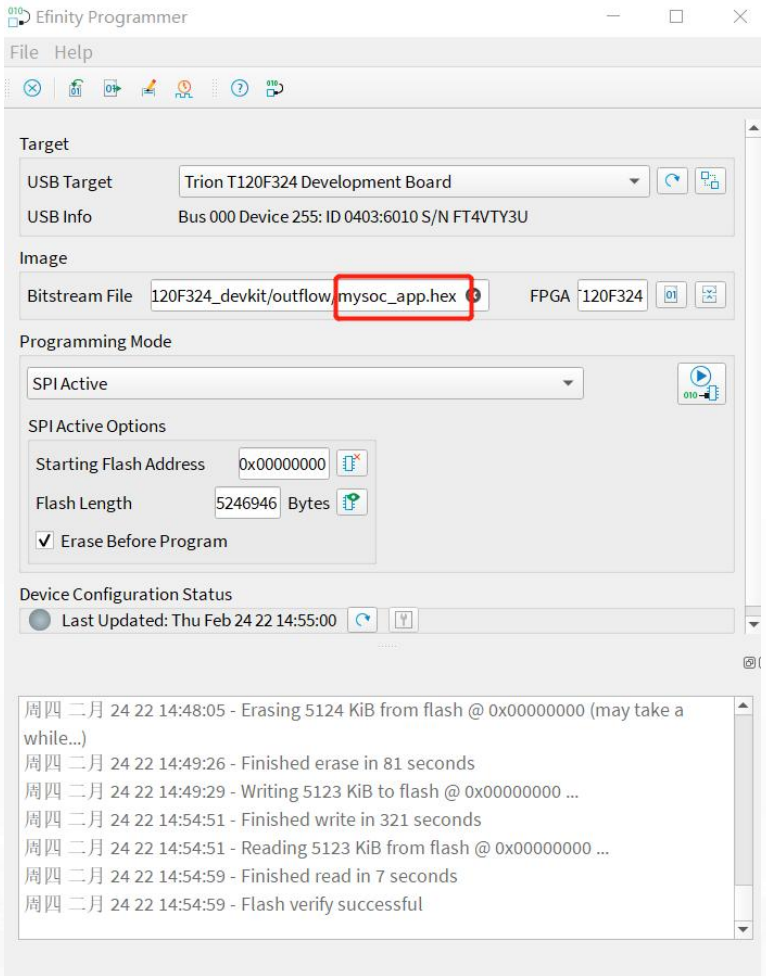
default.ld

```
1  OUTPUT_ARCH( "riscv" )
2
3  ENTRY( _start )
4
5  MEMORY
6  {
7    ram   (wxai!r) : ORIGIN = 0x00008000, LENGTH = 124K
8  }
9
```

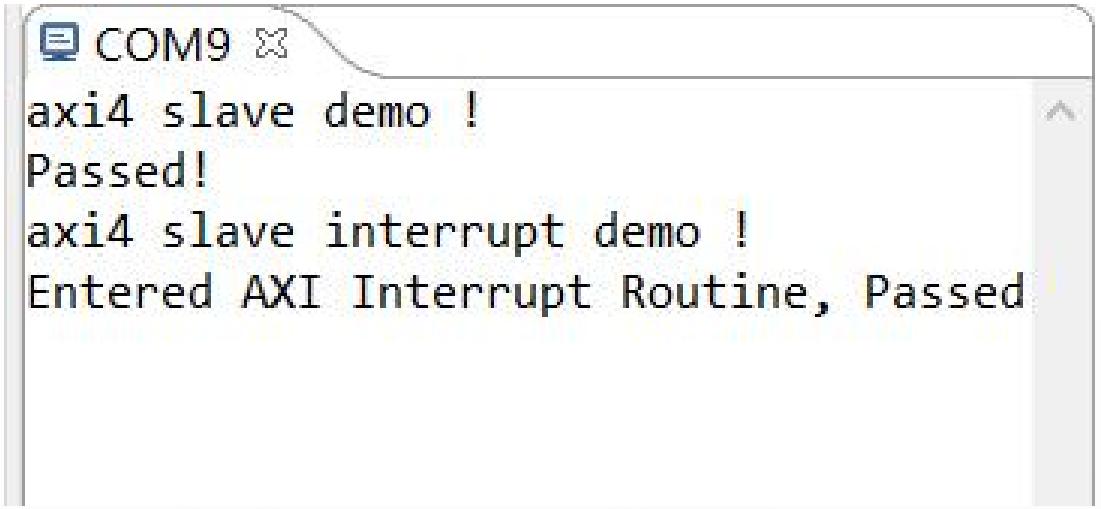
合并FPGA bitstream 和 软件APP bin



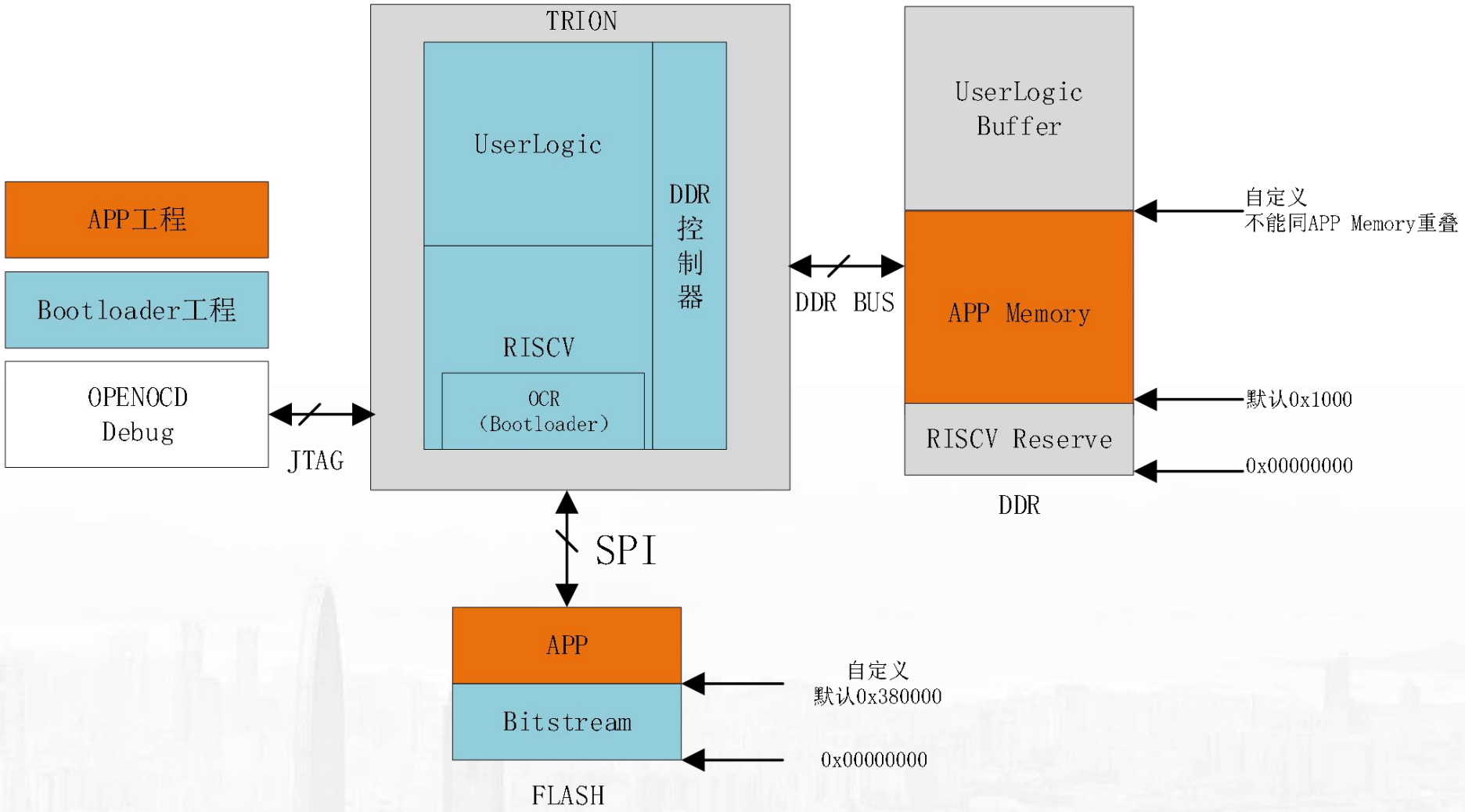
使用Programmer烧写FLASH



手动复位FPGA



Bootloader/APP 和RISCV运行



The End