易灵思Trion FPGA 基础知识

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版本

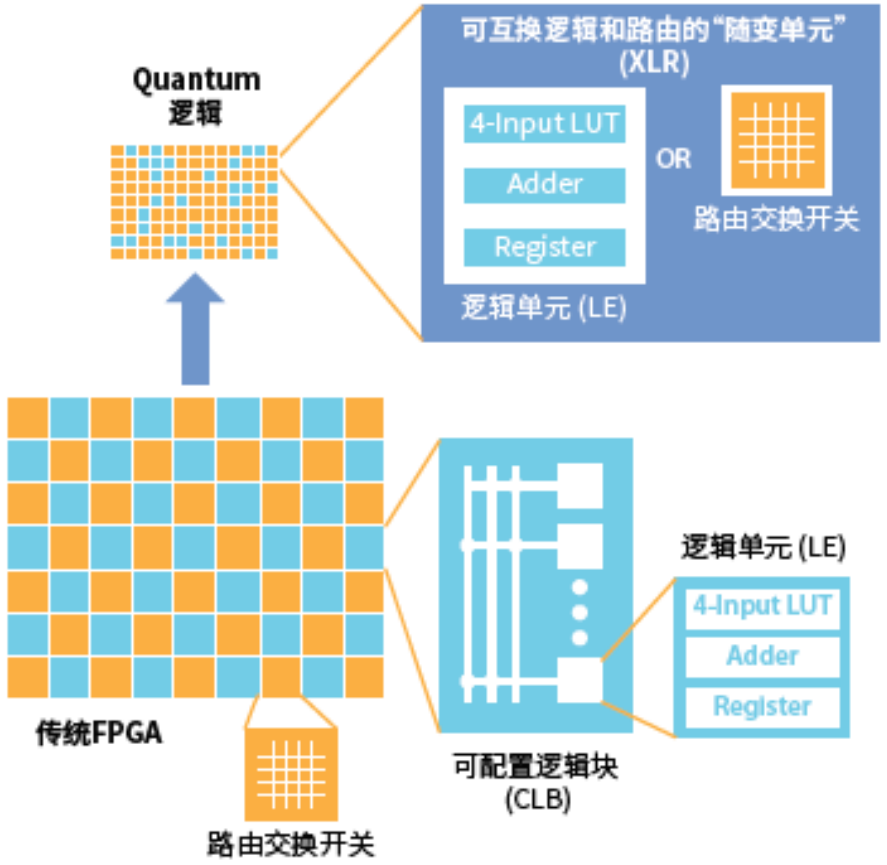
日期	版本	版本描述
2020/5/22	V1.0	初稿发布
2020/11/10	V1.1	更新Trion FPGA 资源列表
2020/11/14	V1.2	增加Core Interface关系说明
2021/9/2	V1.3	PLL输入输出频率范围更新

内容概要

- Trion FPGA基本架构
- Trion FPGA概览
- Trion FPGA逻辑资源
- Trion FPGA Interface
- Trion FPGA配置方式

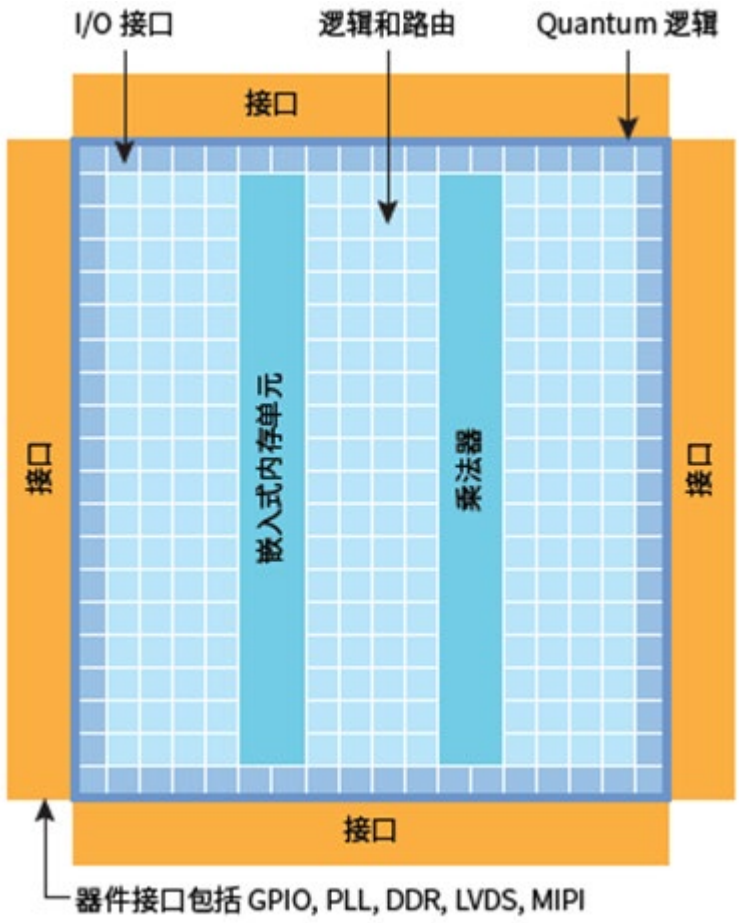
Trion FPGA基本架构

Quantumn内核：完全创新的FPGA



- **Quantum与传统FPGA优势对比**
  - “功耗-性能-成本”(PPA)优化高达4倍
  - 7层金属层 vs. 12+层金属层
  - 独特的设计架构可轻松扩展至百万以上逻辑单元（LE）密度
  - 超便捷的硅工艺可移植性

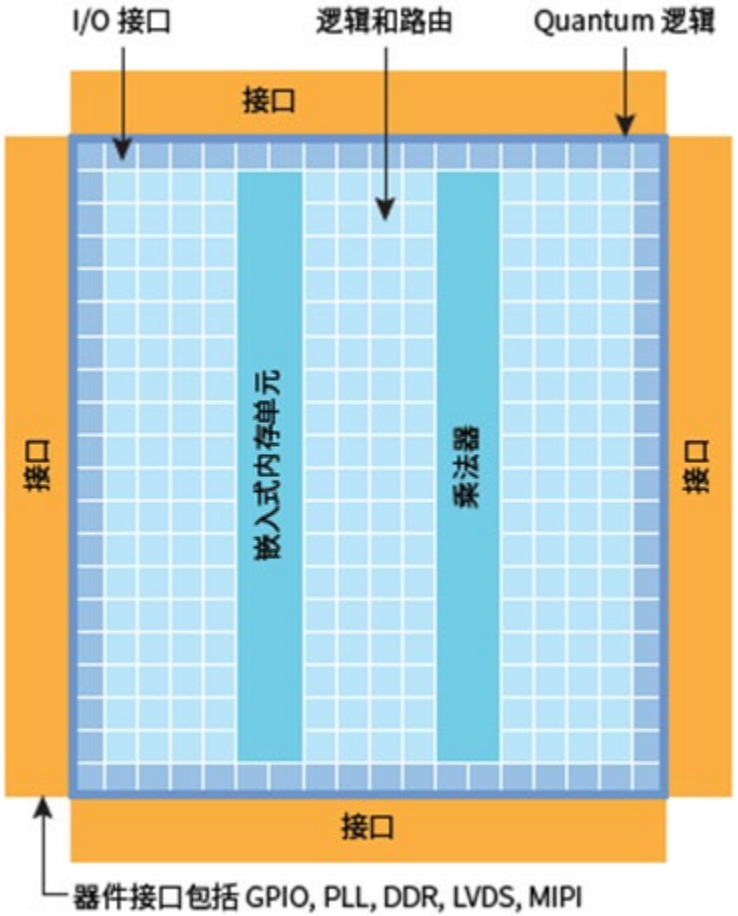
Trion FPGA



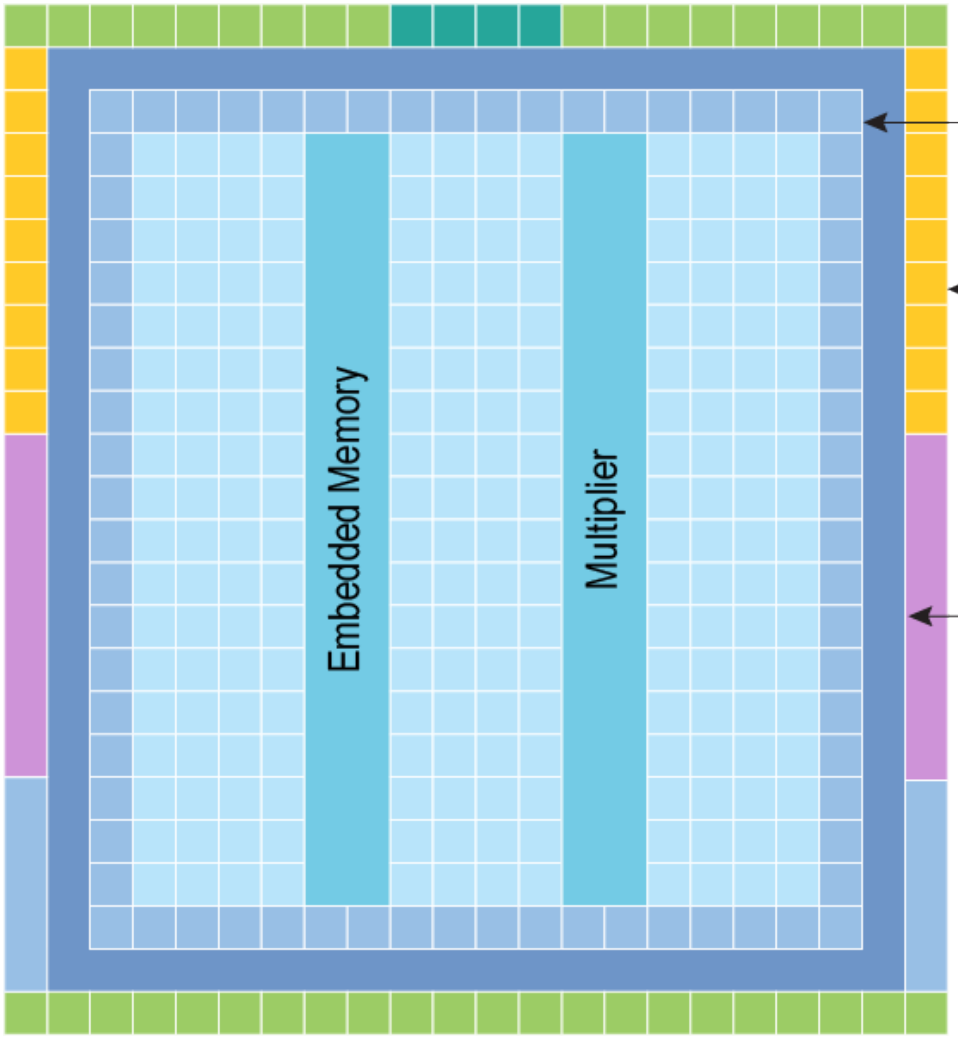
- 内核/Core
  - 易灵思® Trion® FPGA，基于独特的易灵思Quantum™架构，从根本上解决了传统FPGA由专用布线资源而导致的“功耗-性能-成本”之间的矛盾。
  - 基于于先进的Quantum™架构，Trion FPGA具备逻辑和路由互换的特性，同等资源下占据更小的硅片面积，更低的功耗。
  - 第一代 Trion® FPGA 基于SMIC中芯国际40nm工艺，覆盖4K到120K逻辑资源，并支持丰富的HardIP和接口资源

Trion FPGA

- 接口/Interface
  - GPIO
  - PLL
  - MIPI—4-lane MIPI D-PHY，内建硬核CSI-2控制器，每个MIPI D-PHY高达6Gbps带宽。具备低功耗、低成本等优势
  - LVDS—支持高达800 Mbps
  - DDR—硬核Memory控制器，支持DDR3,LPDDR3, LPDDR2器件，简单易用，通道速率800+ Mbps，最大可支持51.2Gbps或更高带宽



Core和Interface的关系



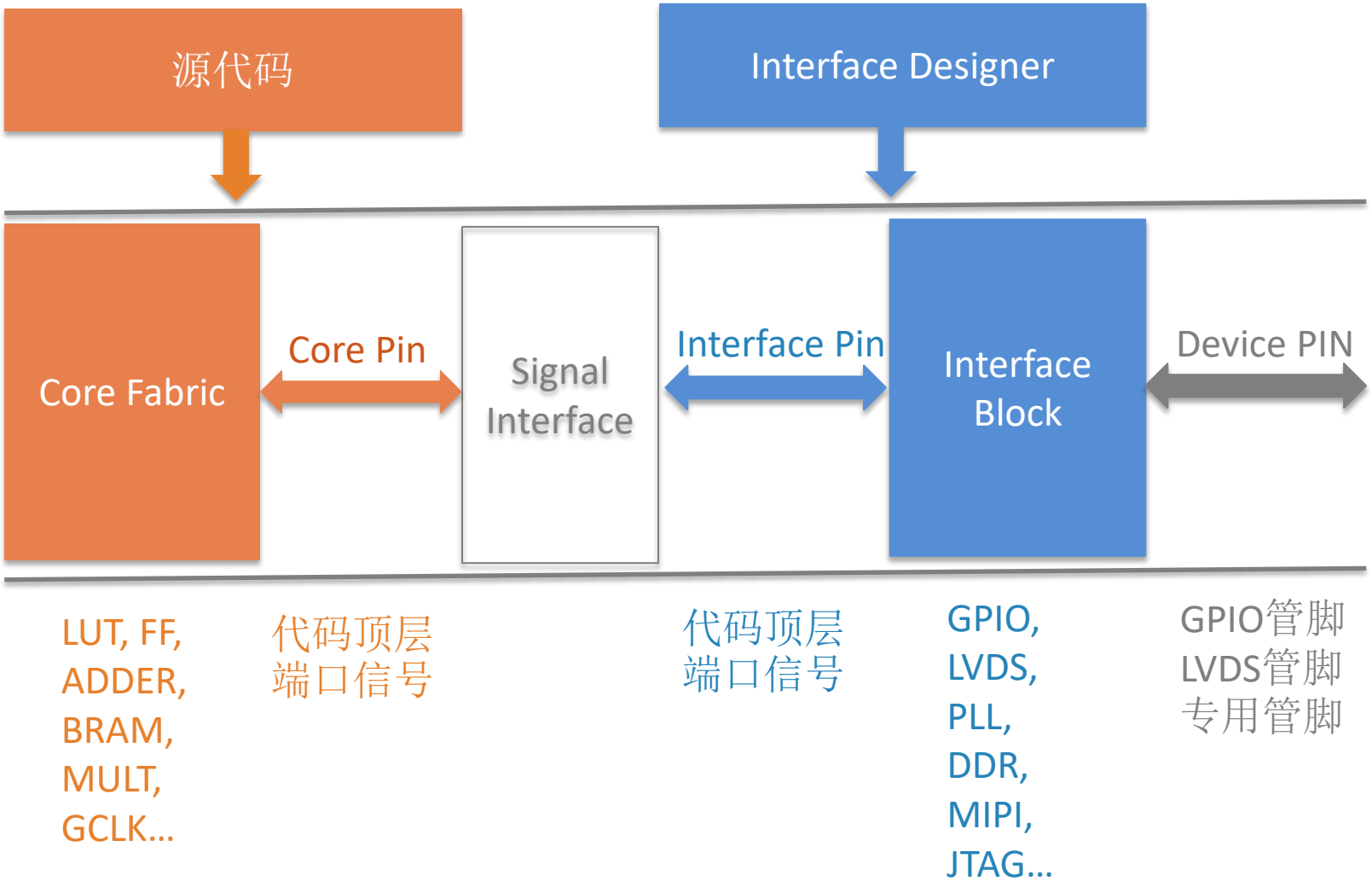
Programmable Core Fabric:
Create your RTL design for the core fabric using Efinity design tools.

Interface Blocks:
Use the Efinity Interface Designer to create and define these blocks and to connect them to your RTL design via the signal interface.

Signal Interface:
Connects the core fabric to the interface blocks

Note: The number and locations of blocks are shown for illustration purposes only. The actual number and position depends on the device.

Core和Interface的关系



Trion FPGA概览

Trion FPGA 资源列表

Features	T4	T8	T13	T20	T35	T55	T85	T120
Logic Elements (LEs)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112,128
Mask Programmable Memory	√	√	√	√	—	—	—	—
Embedded RAM bits (kb)	77	123	727	1,044	1,475	2,765	4,055	5,407
18x18 Multipliers	4	8	24	36	120	150	240	320
PLLs	1	5	5	7	7	8	8	8
Maximum GPIO (1)	55	97	195	230	230	278	278	278
LVDS (TX, RX)	—	6, 6	13, 13	20, 26	20, 26	52, 52	52, 52	52, 52
Package Options (Ball pitch , Size)	GPIO (LVDS TX, RX), MIPI, DDR							
FBGA49 (0.4 mm, 3x3 mm)	33, 0, 0	33, 0, 0						
WLCSP80 (0.4 mm, 4.5 x 3.6 mm)				33, 1, 0				
FBGA81 (0.5 mm, 5x5 mm)	55, 0, 0	55, 0, 0						
*LQFP100 (0.5 mm, 14x14 mm)			65(4,4),0,0	65(4,4),0,0				
LQFP144 (0.5 mm, 20x20 mm)		97(6, 6), 0, 0		97 (6, 6), 0, 0				
FBGA169 (0.65 mm, 9x9 mm)			73 (8, 12), 2, 0	73 (8, 12), 2, 0				
FBGA256 (0.8 mm, 13x13 mm)			195 (13, 13), 0, 0	195 (13, 13), 0, 0				
FBGA324 (0.65 mm, 12x12 mm)				130 (20, 26), 2, x16	130 (20, 26), 2, x16	130 (20, 26), 2, x16	130 (20, 26), 2, x16	130 (20, 26), 2, x16
FBGA400 (0.8 mm 16x16 mm)				230 (20, 26), 0, x16	230 (20, 26), 0, x16			
FBGA484 (0.8 mm, 18x18 mm)						256 (40, 40),0, x32	256 (40, 40),0, x32	256 (40, 40),0, x32
FBGA576 (0.65 mm, 16x16 mm)						278 (52, 52), 3, x32	278 (52, 52), 3, x32	278 (52, 52), 3, x32

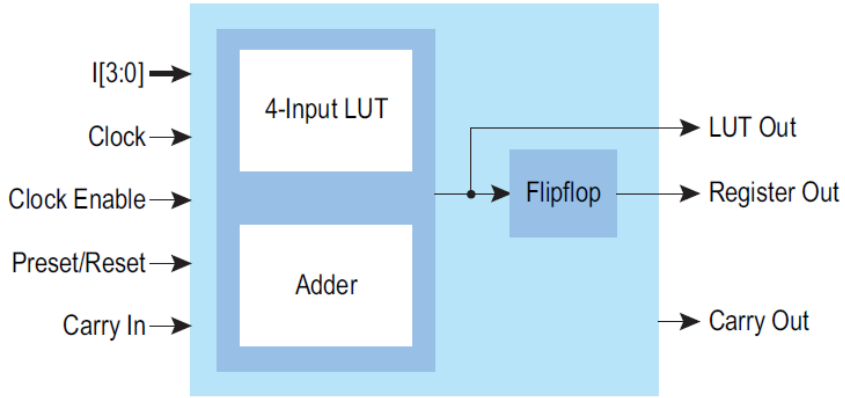
注: (1) 用户IO未包括DDR, MIPI等专用IO数量
(2) 按照温度等级和速度等级，有以下型号类别：C2,C3,C4,C4L,I2,I3,I4,I4L,Q4(AEC-Q100 Grade2 -40°-105°C)
* SiP with 16Mbits Flash

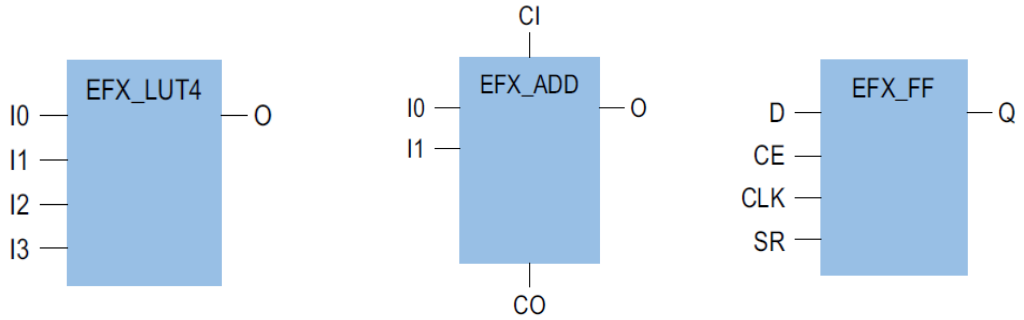
Trion FPGA逻辑资源（CORE）

Trion逻辑资源

- LE逻辑单元
- Block RAM
- MULT乘法器
- 全局时钟网络

LE——逻辑单元



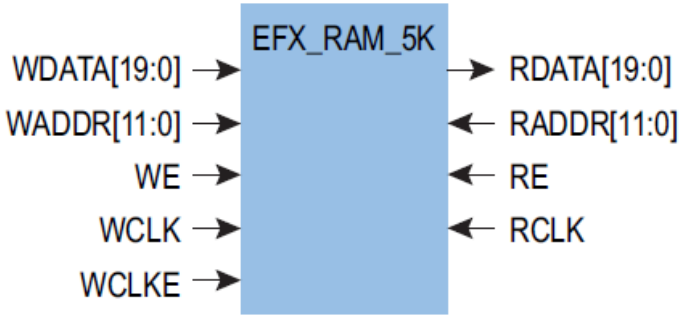


- LE
  - EFX_LUT4:4输入查找表
  - EFX_ADD:1bit全加器
    - 输入进位链carry in
    - 输出进位链carry out
  - EFX_FF:触发器

Block RAM——M5K

- M5K
  - 5120bit/Block
  - 输入/输出寄存
  - ROM
  - Pseudo DPRAM——EFX_RAM_5K
  - Ture DPRAM——EFX_DPRAM_5K

M5K——EFX_RAM_5K



Port Name	Direction	Description
WDATA[19:0]	Input	Write data
WADDR[11:0]	Input	Write address
WE	Input	Write enable
WCLK	Input	Write clock
WCLKE	Input	Write clock enable
RDATA[19:0]	Output	Read data
RADDR[11:0]	Input	Read address
RE	Input	Read enable
RCLK	Input	Read clock

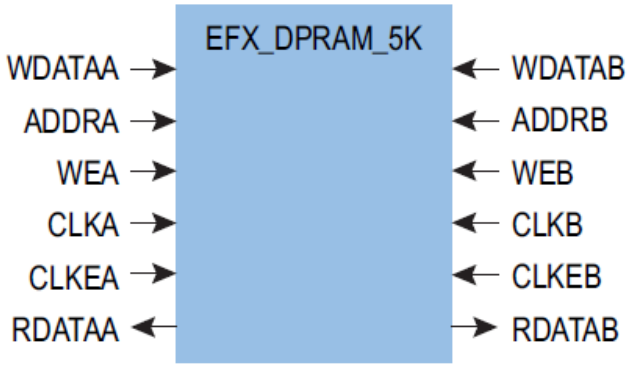
Parameter Name	Allowed Values	Default	Description
INIT_<*n*>	256 bit hexadecimal number	0	Initial RAM content
READ_WIDTH WRITE_WIDTH	16	✓	256 x 16
	8		512 x 8
	4		1024 x 4
	2		2048 x 2
	1		4096 x 1
	20		256 x 20
	10		512 x 10
	5		1024 x 5
OUTPUT_REG	0, 1	0	1 enables output register
<*port name*>_POLARITY	0, 1	1	0 active low, 1 active high
WRITE_MODE	READ_FIRST WRITE_FIRST READ_UNKNOWN	READ_FIRST	When using the same clock for RCLK and WCLK, this parameter controls whether the read data is old or new.

M5K——EFX_RAM_5K

支持模式：

	256 x 16	512 x 8	1024 x 4	2048 x 2	4096 x 1	256 x 20	512 x 10	1024 x 5
256 x 16	✓	✓	✓	✓	✓			
512 x 8	✓	✓	✓	✓	✓			
1024 x 4	✓	✓	✓	✓	✓			
2048 x 2	✓	✓	✓	✓	✓			
4096 x 1	✓	✓	✓	✓	✓			
256 x 20						✓	✓	✓
512 x 10						✓	✓	✓
1024 x 5						✓	✓	✓

M5K——EFX_DPRAM_5K



Port Name	Direction	Description
WDATAA[9:0] WDATAB[9:0]	Input	Write data port A/B
ADDRA[11:0] ADDRB[11:0]	Input	Address port A/B
WEA WEB	Input	Write enable port A/B
CLKA CLKB	Input	Clock port A/B
CLKEA CLKEB	Input	Clock enable port A/B
RDATA[9:0] RDATB[9:0]	Output	Read data port A/B

Parameter Name	Allowed Values	Default	Description
INIT_<*n*>	256 bit hexadecimal number	0	Initial RAM content
READ_WIDTH_A READ_WIDTH_B WRITE_WIDTH_A WRITE_WIDTH_B	8	✓	512 x 8
	4		1024 x 4
	2		2048 x 2
	1		4096 x 1
	10		512 x 10
	5		1024 x 5
WRITE_MODE_A WRITE_MODE_B	READ_FIRST	READ_FIRST	Old data is output to RDATA
	WRITE_FIRST		New data is output to RDATA
	NO_CHANGE		RDATA holds last value
OUTPUT_REG_A OUTPUT_REG_B	0, 1	0	1 enables output register
<*port name*>_POLARITY	0, 1	1	0 active low, 1 active high

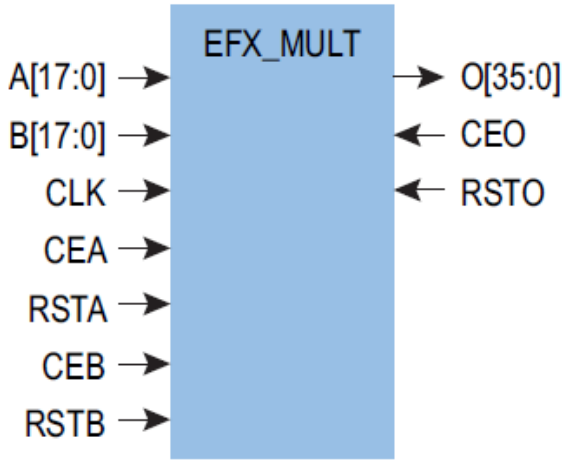
M5K——EFX_DPRAM_5K

	512 x 8	1024 x 4	2048 x 2	4096 x 1	512 x 10 (1)	1024 x 5 (1)
512 x 8	✓	✓	✓	✓		
1024 x 4	✓	✓	✓	✓		
2048 x 2	✓	✓	✓	✓		
4096 x 1	✓	✓	✓	✓		
512 x 10					✓	✓
1024 x 5					✓	✓

MULT——EFX_MULT

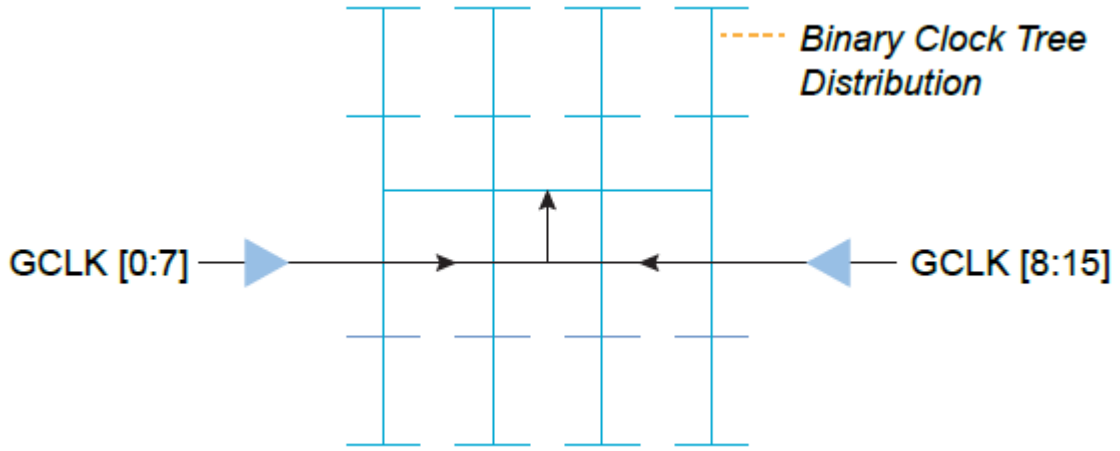
- EFX_MULT
  - 18X18有符号乘法
  - 17X17无符号乘法
  - 输入寄存器
  - 输出寄存器

Parameter Name	Allowed Values	Default	Description
WIDTH	18	18	18 x 18 multiplier
A_REG	0, 1	0	1 enable A registers
B_REG	0, 1	0	1 enable B registers
O_REG	0, 1	0	1 enable output registers
RSTA_SYNC	0, 1	0	0 asynchronous 1 synchronous on A registers
RSTA_VALUE	0, 1	0	0 reset 1 set on A registers
RSTB_SYNC	0, 1	0	0 asynchronous 1 synchronous on B registers
RSTB_VALUE	0, 1	0	0 reset 1 set on B registers
RSTO_SYNC	0, 1	0	0 asynchronous 1 synchronous on output registers
RSTO_VALUE	0, 1	0	0 reset 1 set on output registers
<*port name*>_POLARITY	0, 1	1	0 active low 1 active high



Port Name	Direction	Description
A[17:0]	Input	Operand A
B[17:0]	Input	Operand B
CLK	Input	Clock
CEA	Input	Clock enable A
RSTA	Input	Set/reset A
CEB	Input	Clock enable B
RSTB	Input	Set/reset B
O[35:0]	Output	Multiplier output
CEO	Input	Clock enable O
RSTO	Input	Set/reset O

全局时钟



- 全局时钟
  - 16个全局时钟
  - 锁相环时钟输出
  - GCLK功能的管脚输入
  - 内部逻辑产生的信号
  - T4/T8片上振荡器输出

TRION INTERFACE

Trion Interface

- GPIO
- LVDS—支持高达800 Mbps
- PLL
- MIPI—CSI + DPHY
- DDR—控制器+PHY
- JTAG USER TAP

型号/封装 VS Interface

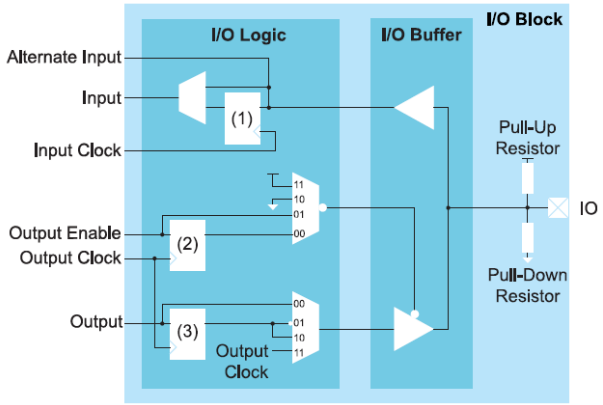
Package	T4	T8	T13	T20	T35	T55	T85	T120
F49								
W80								
F81								
QFP144								
F169								
F256								
F324								
F400								
F484								
F576								

Trion Family Legend:

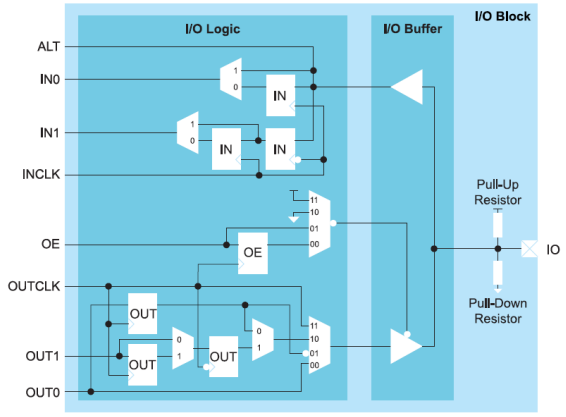
Oscillator PLL LVDS MIPI CSI-2 Controller DDR DRAM Controller

GPIO

简单GPIO Buffer:T4/T8

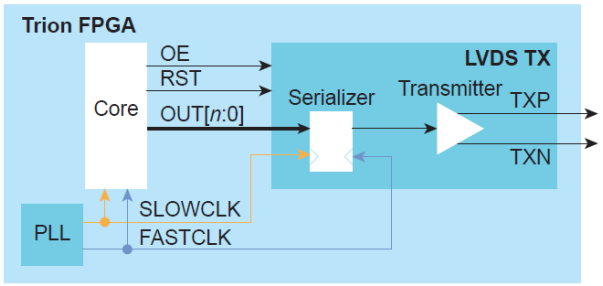


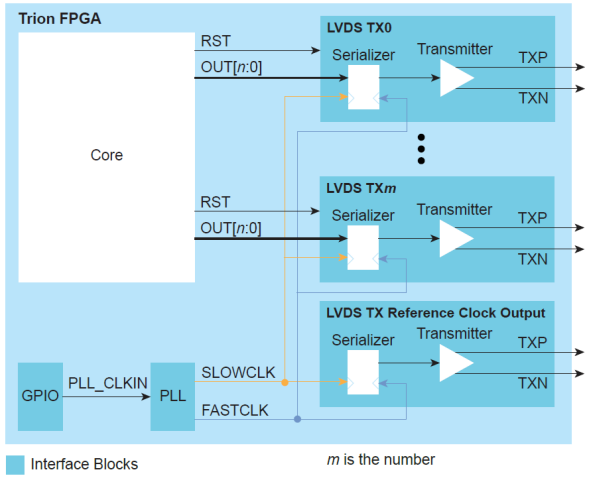
复杂GPIO Buffer： T8T144和更大的FPGA



- GPIO
  - 支持1.8V 2.5V 3.3V标准LVCOMS/LVTTL
  - INPUT/OUTPUT/Bidirection/Clock Out
  - 输入/输出寄存器
    - 支持寄存器时钟反向
    - 支持DDIO
      - 支持Resync
  - 支持输出电流驱动能力调整
  - 支持输出信号摆率(slew rate)调整
  - 支持施密特触发器整形
  - 支持内置弱上下拉电阻

LVDS-TX





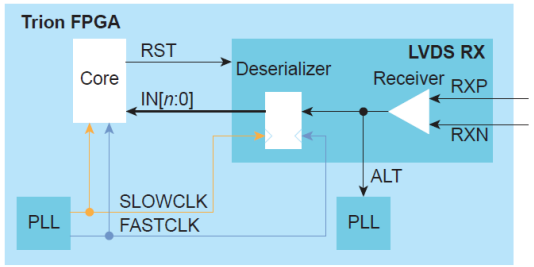
- LVDS-TX
  - 单个端口最大速率可达800Mbps
  - 并串转换
    - 支持1,2,3,4,5,6,7,8位宽
    - 1位模式，串化器旁路，作为普通LVDS输出IO功能
  - 支持1个随路时钟多端口并联
  - 不用LVDS的时候，可作为GPIO使用

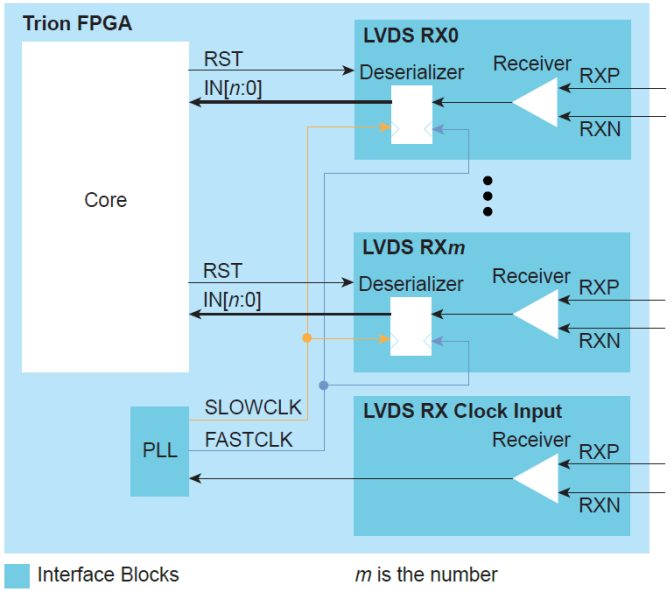
Signal	Direction	Notes
OUT[*n*-1:0]	Input	Parallel output data where *n* is the serialization factor. A width of 1 bypasses the serializer.
OE	Input	LVDS output enable, available in simple buffer (x1) mode. Unused by default.
FASTCLK	Input	Fast clock to serialize the data to the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data from the core.
RST	Input	Reset the serializer. Unused by default.

Pad	Direction	Description
TXP	Output	Differential P pad.
TXN	Output	Differential N pad.

Parameters	Choices	Notes
Mode	**serial data output** or **reference clock output**	**serial data output**—Simple output buffer or serialized output. **reference clock output**—Use the transmitter as a clock output.
Serialization Width	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the serializer is bypassed and the LVDS buffer is used as a normal output.
Reduce VOD Swing	True or False	When true, enables reduced output swing (similar to slow slew rate).
Output Load	Varies by FPGA.	Output load in pF. For T8Q144 FPGAs, use an output load of 7 pF or higher to achieve the maximum throughput of 600 Mbps.

LVDS-RX





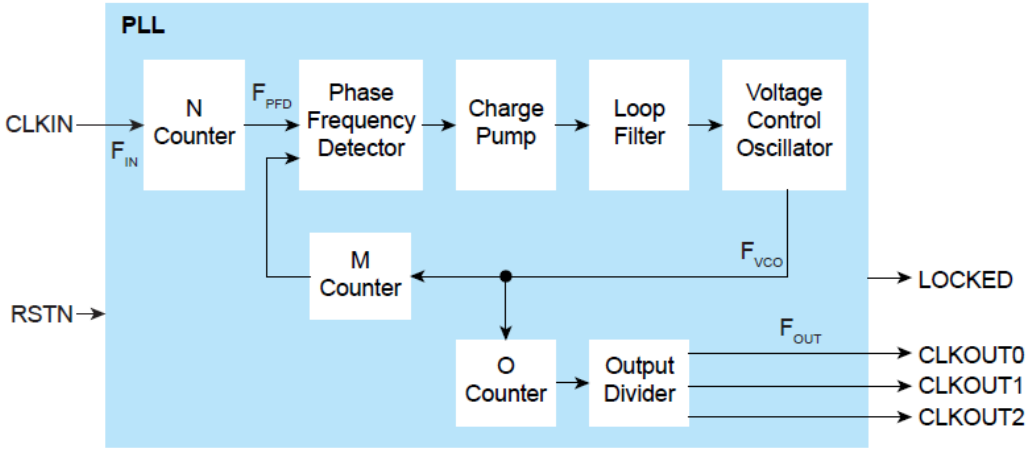
- LVDS-RX
  - 单个端口最大速率可达800Mbps
  - 串并转换
    - 支持1,2,3,4,5,6,7,8位宽
    - 1位模式，串化器旁路，作为普通LVDS输入IO功能
  - 支持1个随路时钟多端口并联
  - 不用LVDS的时候，可作为普通GPIO使用

Signal	Direction	Notes
IN[*n*-1:0]	Output	Parallel input data where *n* is the de-serialization factor. A width of 1 bypasses the deserializer.
ALT	Output	Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLLCLK and PLLFBK.
FASTCLK	Input	Fast clock to de-serialize the data from the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data to the core.
RST	Input	Reset the de-serializer. Unused by default.

Pad	Direction	Description
RXP	Input	Differential P pad.
RXN	Input	Differential N pad.

Parameter	Choices	Notes
Connection Type	**normal** or **alternate**	**alternate**—Use the alternate function of the LVDS RX resource (such as a PLL reference clock). Also choose de-serialization width of 1. **normal**—Regular RX function.
Deserialization	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the de-serializer is bypassed and the LVDS buffer is used as a normal input.
Enable On-Die Termination	True or False	When true, enables an on-die 100-ohm resistor.

PLL-Simple PLL-T4/T8

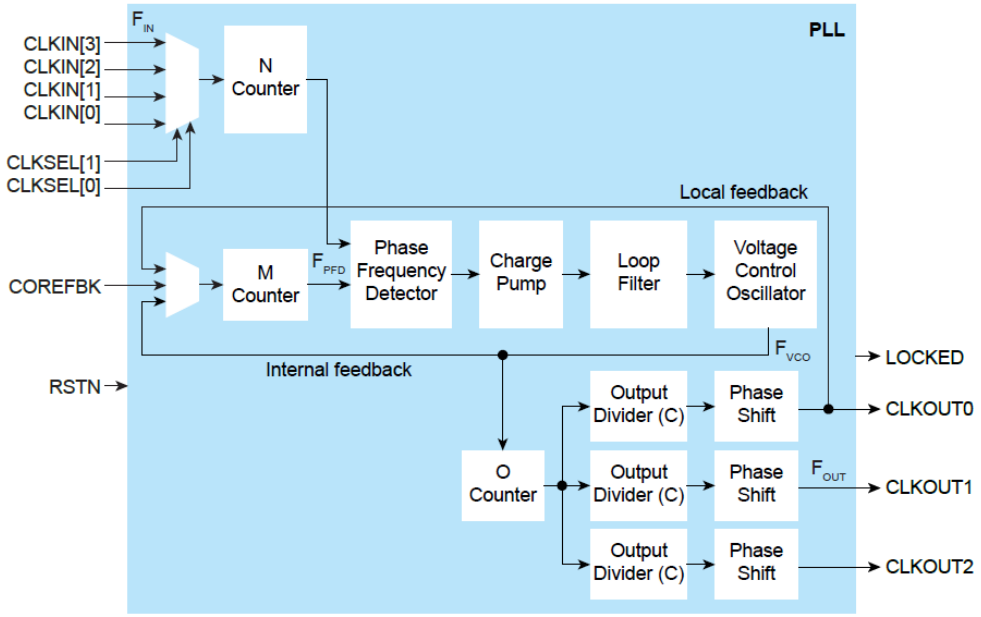


The counter settings define the PLL output frequency:	where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = F_{VCO} / (O \times \text{Output divider})$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency

Setting	Allowed Values	Notes
N counter	1 - 15 (integer)	Pre-divider
M counter	1 - 255 (integer)	Multiplier
O counter	1, 2, 4, 8	Post-divider
Output divider	2, 4, 8, 16, 32, 64, 128, 256	Output divider per output

- 输入范围:10 ~ 50 MHz.
- 输出范围：0.25~400MHz
- 输出抖动：P-P典型值100ps
- 占空比：0.45~0.55 典型值0.5
- 压控振荡器VCO频率范围：500到1500 MHz.
- 锁相环复位功能
- 锁定指示功能
- 支持三个时钟输出可配置

PLL-Advanced PLL



Internal Feedback Mode	Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$	$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ (9) $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency C is the output divider

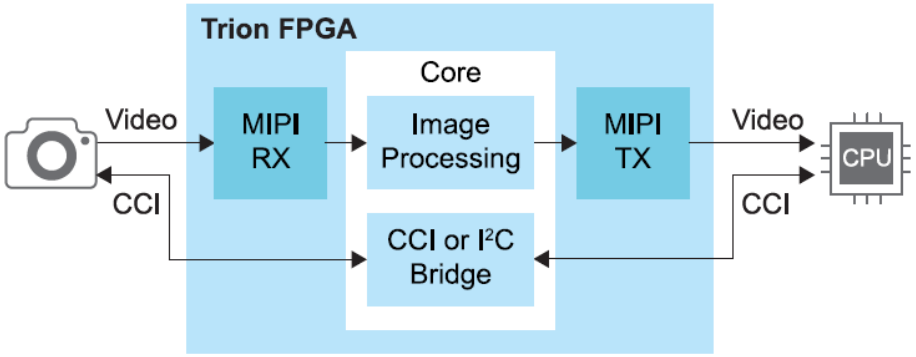
- 输入范围:10 ~ 400MHz.
- 输出范围：
  - 0.24~500MHz
  - 0.24~800MHz PLL_BR0 for DDR
- 输出抖动：P-P最大值200ps
- 占空比：0.45~0.55 典型值0.5
- 压控振荡器VCO频率范围： 500到1600MHz.
- 锁相环复位功能
- 锁定指示功能
- 支持三个时钟输出可配置

PLL-Advanced PLL

Parameter	Choices	Notes
Feedback Mode	Internal	PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out.
	Local	PLL feedback is local to the PLL. Aligns the clock out phase with clock in.
	Core	PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay.
Reference clock Frequency (MHz)	User defined	
Multiplier (M)	1 - 255 (integer)	M counter.
Pre Divider (N)	1 - 15 (integer)	N counter.
Post Divider (O)	1, 2, 4, 8	O counter.
Clock 0, Clock 1, Clock 2	On, off	Use these checkboxes to enable or disable clock 0, 1, and 2.
Pin Name	User defined	Specify the pin name for clock 0, 1, or 2.
Divider (C)	1 to 256	Output divider.
Phase Shift (Degree)	0, 45, 90, 135, 180, or 270	Phase shift CLKOUT by 0, 45, 90, 135, 180, or 270 degrees. 90, 180, and 270 require the C divider to be 2. 45 and 135 require the C divider to be 4. To phase shift 225 degrees, select 45 and invert the clock at the destination. To phase shift 315 degrees, select 135 and invert the clock at the destination.
Use as Feedback	On, off	

- 反馈模式
  - Internal
  - Core
  - Local
- 参考时钟输入模式
  - External
  - Dynamic
  - Core
- 输出时钟相位调整
  - 0, 45, 90, 135, 180, or 270

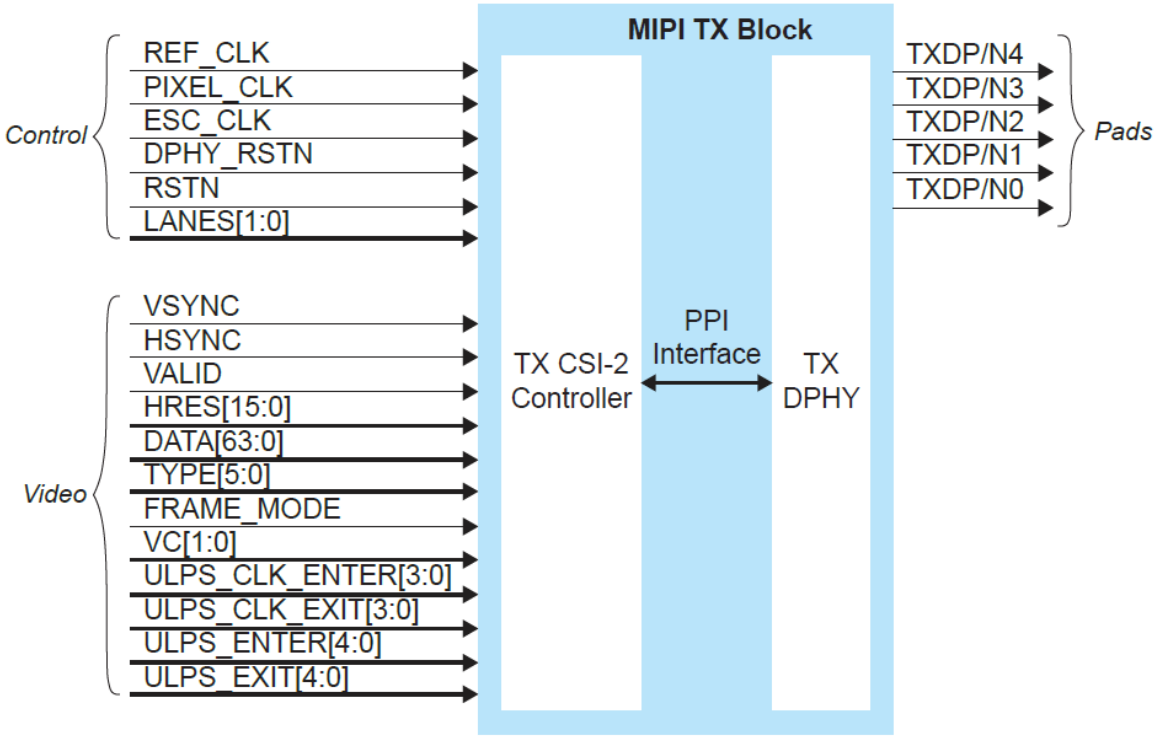
MIPI

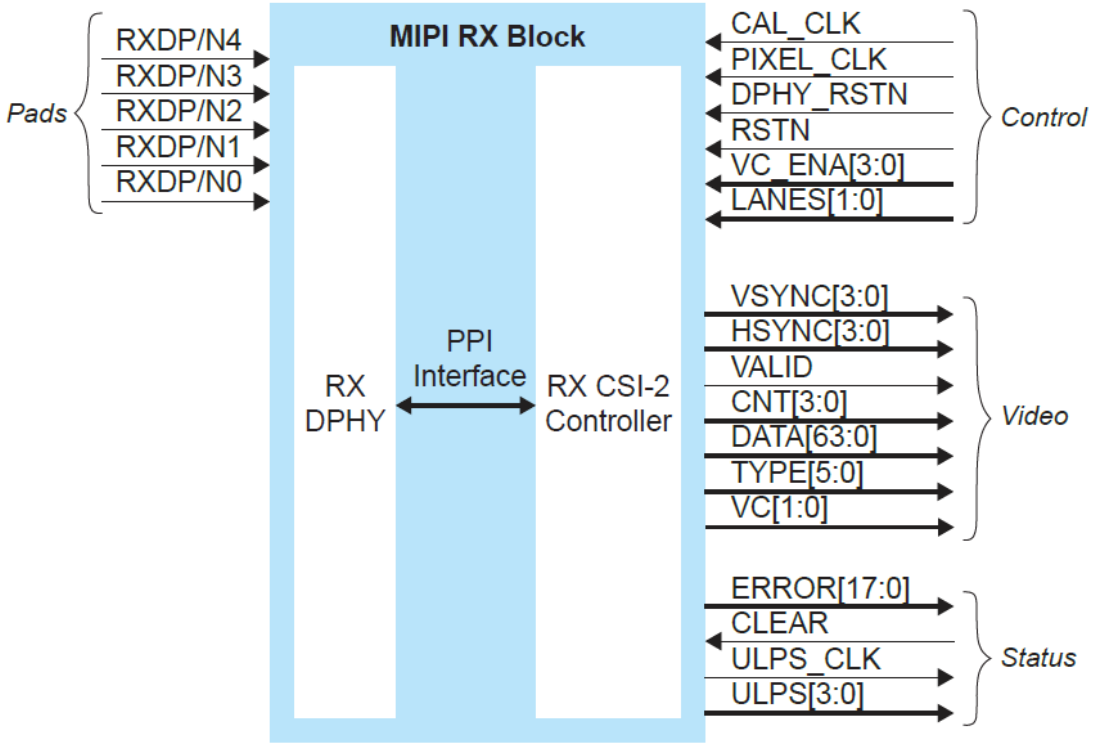


- MIPI TX/RX接口支持MIPI CSI-2规范v1.3和MIPI D-PHY规范v1.1
- MIPI D-PHY和CSI-2控制器均为硬核，用户不能绕过CSI-2控制器只使用D-PHY
- 支持配置为1、2、4Lanes模式
- 高速模式每条Lane支持高达1.5 Gbps
- 可配置为连续和非连续时钟模式
- 支持超低功耗状态(ULPS)
- 64位像素接口

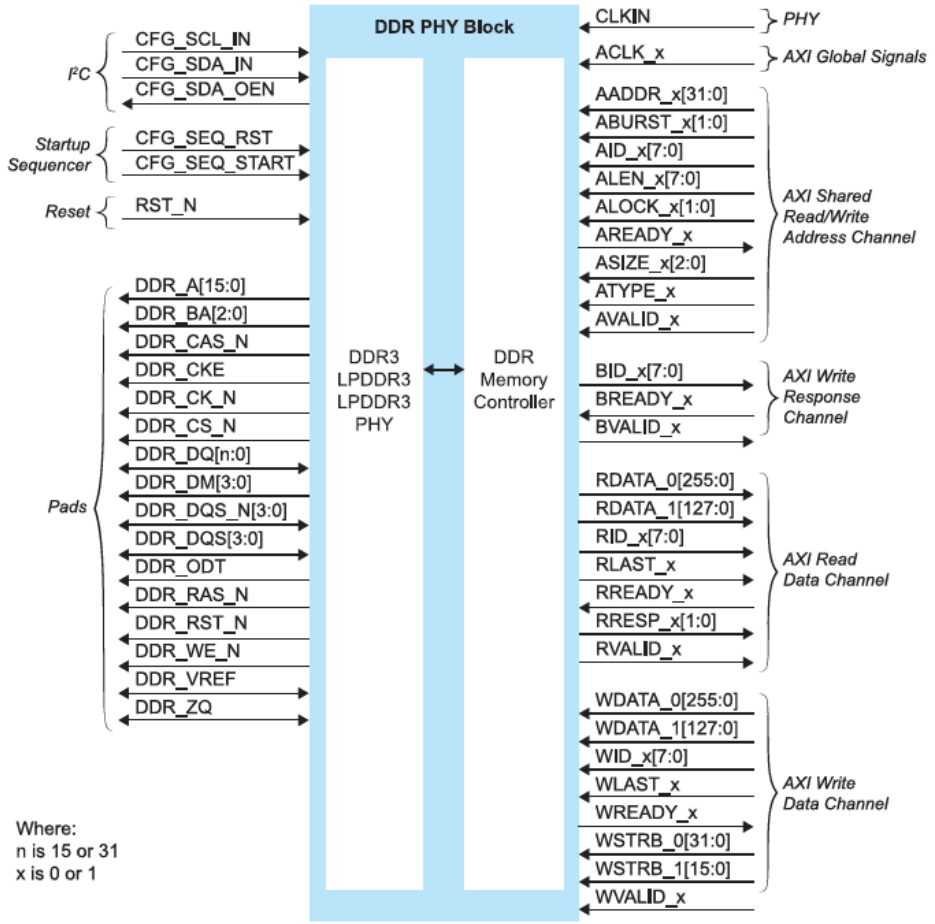
Supported Data Type	Format
RAW	RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
YUV	YUV420 8-bit (legacy), YUV420 8-bit, YUV420 10-bit, YUV420 8-bit (CSPS), YUV420 10-bit (CSPS), YUV422 8-bit, YUV422 10-bit
RGB	RGB444, RGB555, RGB565, RGB666, RGB888
User Defined	8 bit format

MIPI-TX/RX Block





DDR



- 支持X32或者X16 数据总线宽度
- 支持DDR3, DDR3L, DDR3U, LPDDR3, LPDDR2
- 控制器+PHY全硬核
- DDR PHY速率最高可达1066Mbps
- 独立的I2C总线提供数据校准功能
- 复位和配置时序控制信号
- 2个面向FPGA Core 逻辑的AXI接口
  - 接口0：128bit数据宽度
  - 接口1：128bit或者256bit数据宽度

DDR

- DDR3颗粒
  - 1066E, 1066F,1066G, 800D, 800E
  - X8，X16
  - 1G，2G，4G，8G
- LPDDR3颗粒
  - 800,1066
  - X16,X32
  - 4G,8G
- LPDDR2颗粒
  - 400, 533, 667, 800, 1066
  - X16,X32
  - 512MB, 1G, 2G, 4G
- DDR内存模式寄存器可配置
- 提供默认Profile参数
- FPGA输入/输出终端匹配阻抗可配置

JTAG USER TAP

Ports	Direction	Notes
TDI	Input	Test data in.
TCK	Input	Test clock.
TMS	Input	Test mode select.
SEL	Input	Indicates that the user instruction is active for the interface.
DRCK	Input	Gated test clock output. Toggles when SEL is high and the TAP controller is in the capture or shift state.
RESET	Input	TAP controller is in the reset state.
RUNTEST	Input	TAP controller is in the run test or idle state.
CAPTURE	Input	TAP controller is in the capture state.
SHIFT	Input	TAP controller is in the shift state.
UPDATE	Input	TAP controller in the update state.
TDO	Output	Test data out.

- JTAG用户TAP接口，允许通过专用JTAG口对内部逻辑进行操作
  - Debugger
  - JTAG to FLASH Bridge
- 支持多个用户TAP

Trion FPGA配置模式

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Trion FPGA配置模式

- 主动模式（SPI Active）— AS模式
  - 通过SPI专用插座在线烧写FLASH，FLASH离线烧写好了再焊接
  - Trion FPGA自己主动通过从非易失性的SPI FLASH读取bit流进行加载
  - 支持X1 X2 X4
- 被动模式（SPI Passive）— PS模式
  - 上位机或者MCU通过SPI接口向FPGA发送bit流文件，对FPGA进行加载
  - 支持X1 X2 X8 X16 X32
- JTAG模式
  - 上位机通过JTAG口将bit流文件发送到FPGA，对FPGA进行加载
- SPI Active using JTAG bridge — Bridge模式
  - 通过FPGA的JTAG口烧写和FPGA连接的SPI FLASH

Trion FPGA配置模式 — 模式选择

Configuration Mode	Parallel/Serial	TEST_N	SS_N	CBUS2, CBUS1, CBUS0	Width
SPI Active	Serial	1	1	3'b111	x1
	Parallel	1	1	3'b110	x2
	Parallel	1	1	3'b101	x4
SPI Passive	Serial	1	0	3'b111	x1
	Parallel	1	0	3'b110	x2
	Parallel	1	0	3'b101	x4
	Parallel	1	0	3'b100	x8
	Parallel	1	0	3'b011	x16
	Parallel	1	0	3'b010	x32

谢　　谢！