易灵思

钛金系列FPGA基础知识

Bruce Chen 2022/2/24

版本

日期	版本	版本说明
2021/02/25	V1.0	初稿
2021/10/20	V1.1	增加Ti35/Ti60封装和资源信息
2022/02/24	V1.2	增加Ti90/Ti120/Ti180逻辑资源信息和LPDDR4控制器，2.5G MIPI DPHY信息

Ti60

Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8[2]				
62,016	60,800	14,720	Up to 32	2.6	256	160

Resource		W64	F100S3F2	F225
Single-ended GPIO (Max)	HVIO (1.8, 2.5, 3.0, 3.3 V LVCMOS, 3.0, 3.3 V LVTTL)	-	-	23
	HSIO (1.2, 1.5, 1.8 V LVCMOS, HSTL and SSTL)	35	61	140
Differential GPIO (Max)	HSIO (LVDS, Differential HSTL, SSTL, MIPI TX Data and Clock Lanes)	17	30	70
	HSIO (MIPI RX Data Lanes)	8	21	58
	HSIO (MIPI RX Clock Lanes)	2	3	12
Global clock or control signals from GPIO pins		3	8	15
PLLs		2	3	4

Ti35

Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8[2]				
36,176	35,467	8,586	Up to 32	1.53	149	93

Resource		BGA100	BGA225
Single-ended GPIO (Max)	HVIO (1.8, 2.5, 3.0, 3.3 V LVCMOS, 3.0, 3.3 V LVTTL)	-	23
	HSIO (1.2, 1.5, 1.8 V LVCMOS, HSTL and SSTL)	61	140
Differential GPIO (Max)	HSIO (LVDS, Differential HSTL, SSTL, MIPI D-PHY TX Data and Clock Lanes)	30	70
	HSIO (MIPI D-PHY RX Data Lanes)	21	58
	HSIO (MIPI D-PHY RX Clock Lanes)	3	12
Global clock or control signals from GPIO pins		8	15
PLLs		3	4

Ti180/Ti20/Ti90

Ti180

Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8(1)				
176,256	172,800	32,000	Up to 32	13.11	1280	640

Ti120

Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8(1)				
123,379	120,960	22,400	Up to 32	9.18	896	448

Ti90

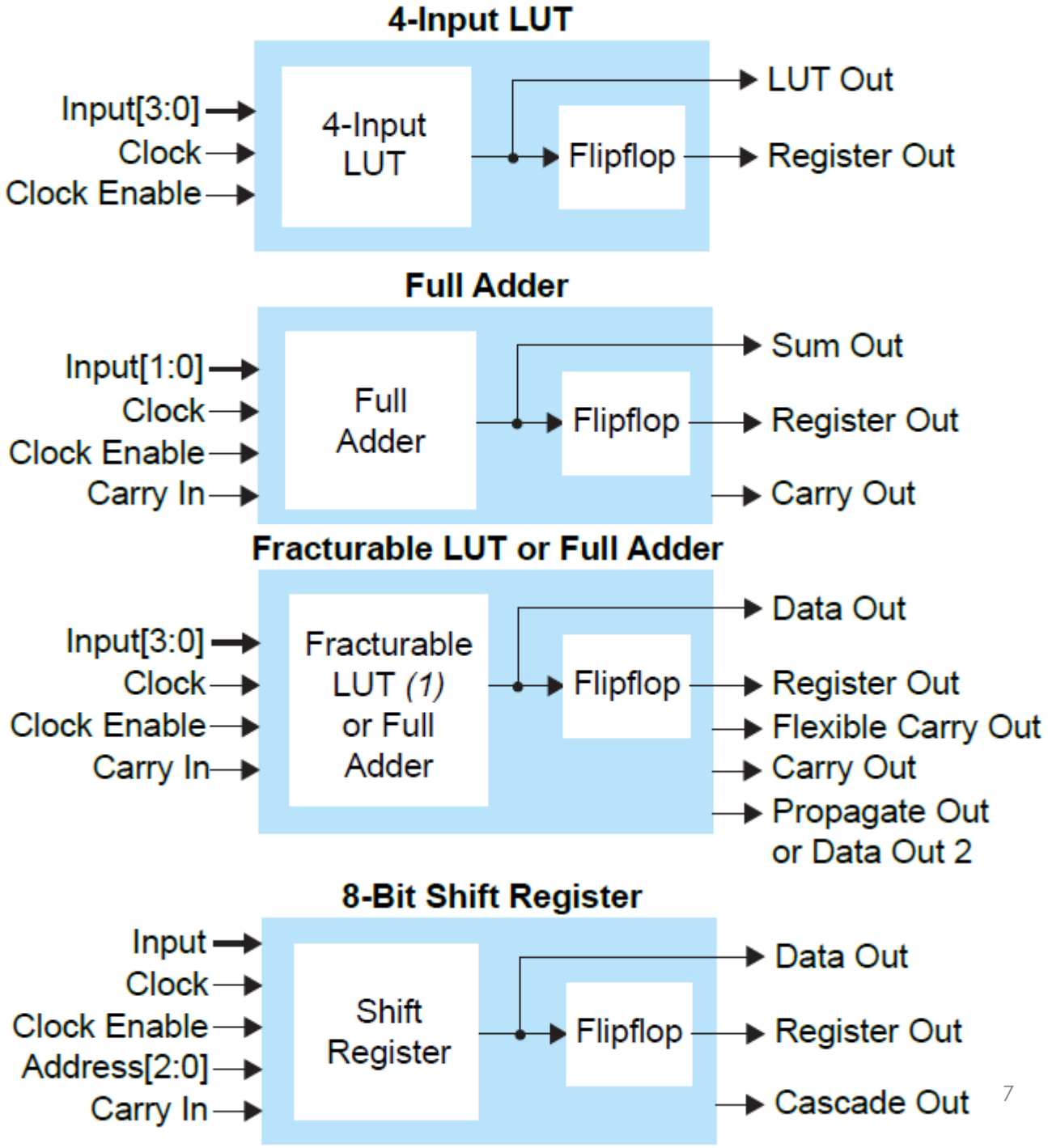
Logic Elements (LEs)	eXchangeable Logic and Routing (XLR) Cells		Global Clock and Control Signals	Embedded Memory (Mbits)	Embedded Memory Blocks (10 Kbits)	Embedded DSP Blocks
	Total	SRL8(1)				
92,534	90,719	16,800	Up to 32	6.88	671	336

主要内容

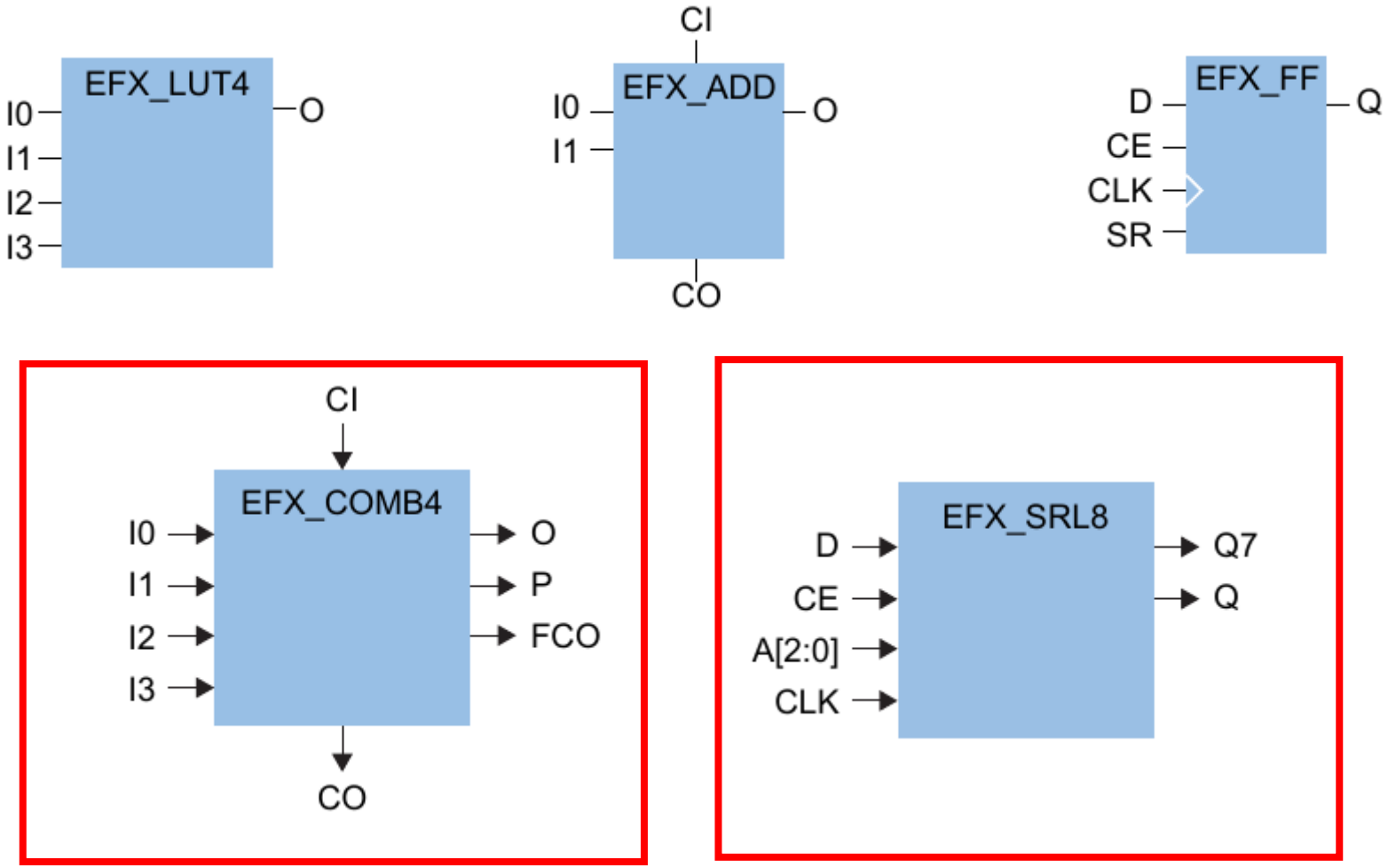
- Core Function
  - XLR
  - Embedded Memory
  - DSP Block
  - Global Network
- Interface Function
  - GPIO
  - PLL
  - Oscillator
  - SPI FLASH
  - HyperRAM
  - SEU detection
  - Internal Reconfiguration Block
- Security Feature

Core Function

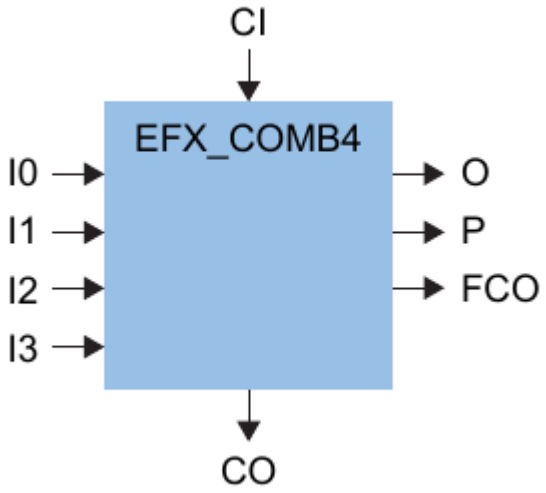
- XLR
- Embedded Memory
- DSP Block
- Global Network



XLR


EFX_LUT4
I0
I1
I2
I3
O
CI
EFX_ADD
I0
I1
O
CO
EFX_FF
D
CE
CLK
SR
Q
CI
EFX_COMB4
I0
I1
I2
I3
O
P
FCO
CO
EFX_SRL8
D
CE
A[2:0]
CLK
Q7
Q

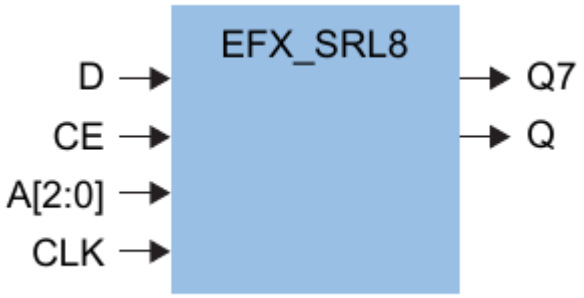
EFX_COMB4



Signal	LOGIC Mode	ARITH Mode
I0	Input.	Input.
I1	Input.	Input.
I2	Input.	Unused.
I3	Input.	Unused.
O	Is a function of the I3, I2, I1, and I0 inputs.	Is a function of the CI, I1, and I0 inputs.
P	Is a function of the I1 and I0 inputs.	Is a function of the I1 and I0 inputs.
FCO	Unused.	Is a function of the CI, I1, and I0 inputs.
CI	Unused.	Carry in.
CO	Unused.	Is a function of the CI, I1, and I0 inputs.
Notes	When just using the O output, all 4 inputs are rotatable during routing. When using the O and P outputs, only the I1 and I0 inputs may be rotated during routing. *Only a flipflop being driven by the O output may be packed with this cell.*	Unlike EFX_ADD, the function of the outputs is dependent on the LUTMASK parameter. The I1 and I0 inputs may be rotated during routing.

EFX_COMB4可以映射成比EFX_LUT4和EFX_ADD更复杂的逻辑功能。
例如:
算数模式：跳跃进位加法器（EFX_ADD只能做串联进位加法器）
逻辑模式：一个逻辑单元可实现一个3输入功能和一个2输入功能组合

EFX_SRL8



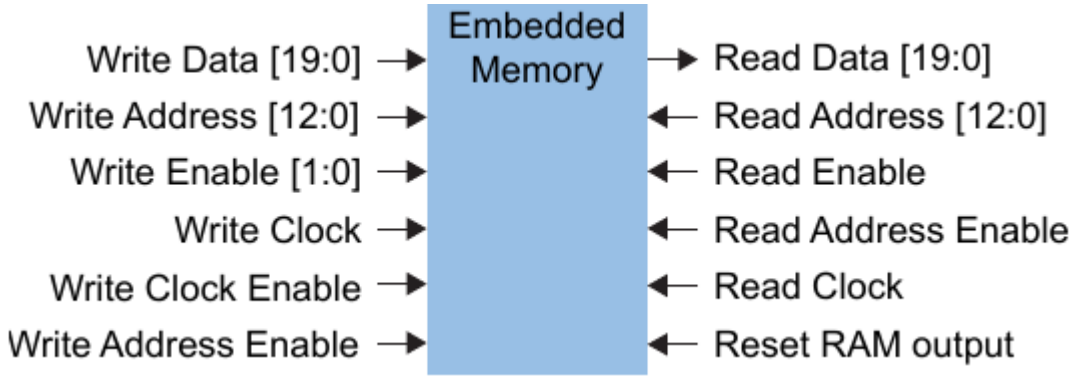
Port	Direction	Description
D	Input	Input data
CE	Input	Clock Enable
CLK	Input	Clock
A[2:0]	Input	Address of the shift register bit read.
Q	Output	Output data inverted value.
Q7	Output	Output of the last bit of the shift register used for cascading. (non-inverted)

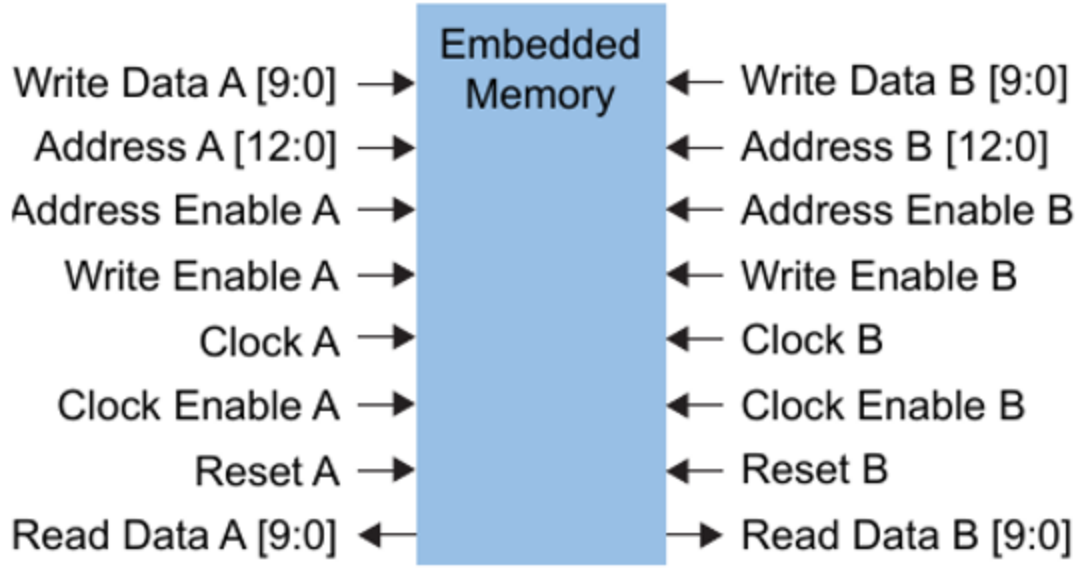
A[2:0]	Q
111	1
110	2
101	3
100	4
011	5
010	6
001	7
000	8

EFX_SRL8：8位移位寄存器，每一位内容均可以通过A[2:0]动态读出。

Core Function

- XLR
- Embedded Memory
- DSP Block
- Global Network





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EFX_RAM10

- 支持Byte Enable功能
  - 数据宽度=16/20
- 支持非对称读写位宽
- 支持输出复位

	512 x 16	1024 x 8	2048 x 4	4096 x 2	8192 x 1	512 x 20	1024 x 10	2048 x 5
512 x 16	✓	✓	✓	✓	✓			
1024 x 8	✓	✓	✓	✓	✓			
2048 x 4	✓	✓	✓	✓	✓			
4096 x 2	✓	✓	✓	✓	✓			
8192 x 1	✓	✓	✓	✓	✓			
512 x 20						✓	✓	✓
1024 x 10						✓	✓	✓
2048 x 5						✓	✓	✓

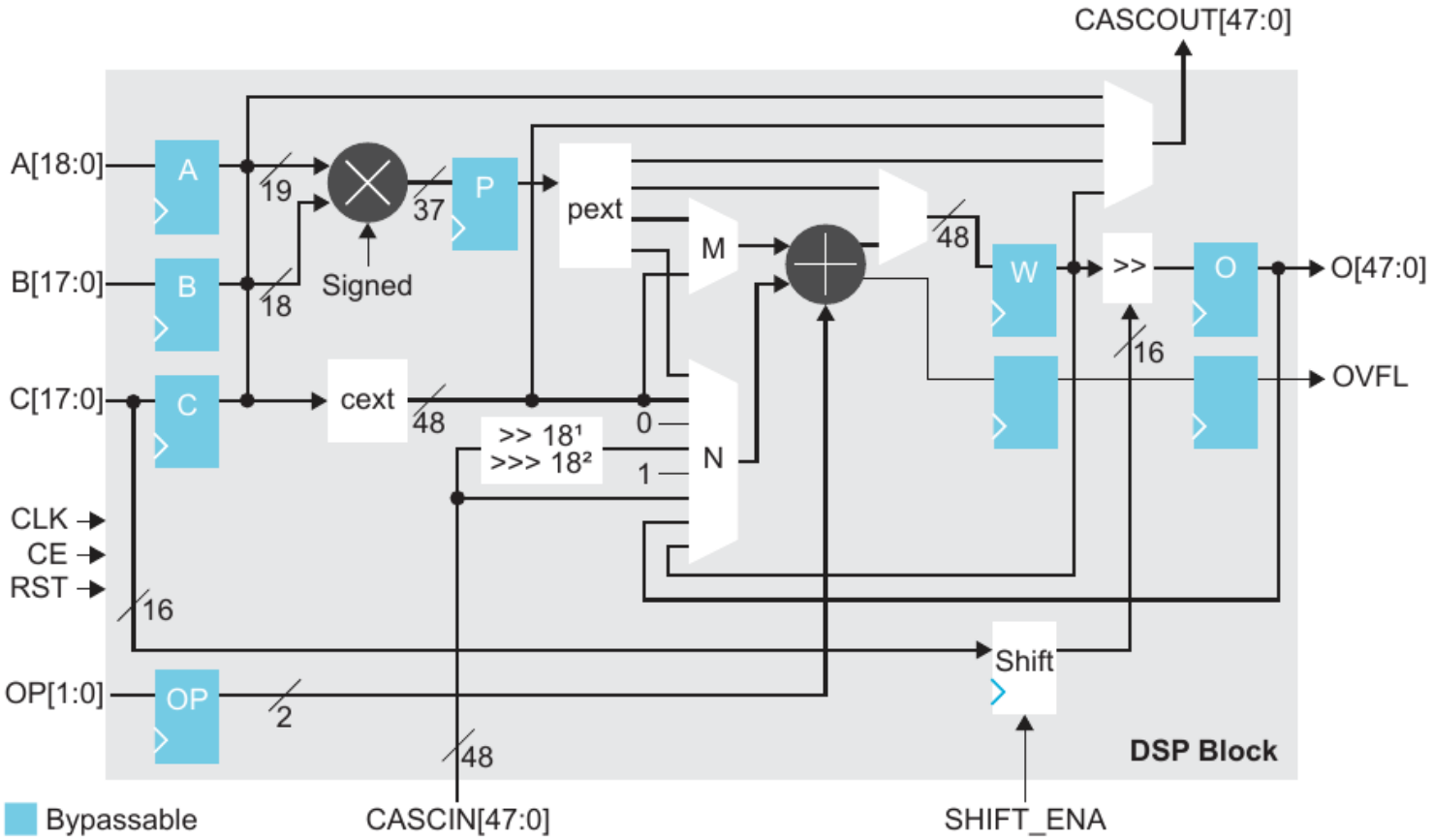
EFX_DPRAM10

- 支持非对称读写位宽
- 支持输出复位

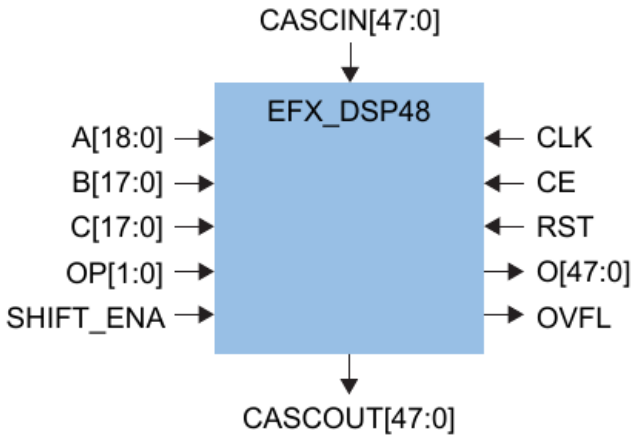
	1024 x 8	2048 x 4	4096 x 2	8192 x 1	1024 x 10	2048 x 5
1024 x 8	✓	✓	✓	✓		
2048 x 4	✓	✓	✓	✓		
4096 x 2	✓	✓	✓	✓		
8192 x 1	✓	✓	✓	✓		
1024 x 10					✓	✓
2048 x 5					✓	✓

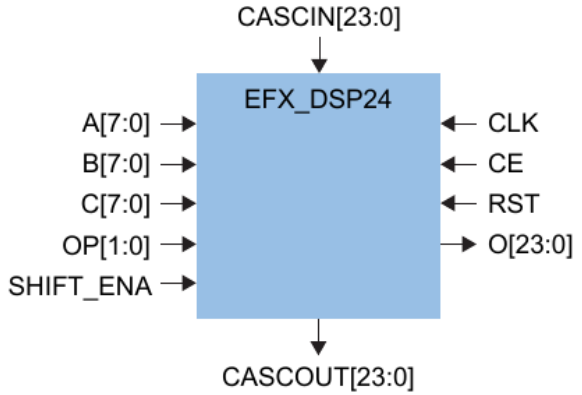
Core Function

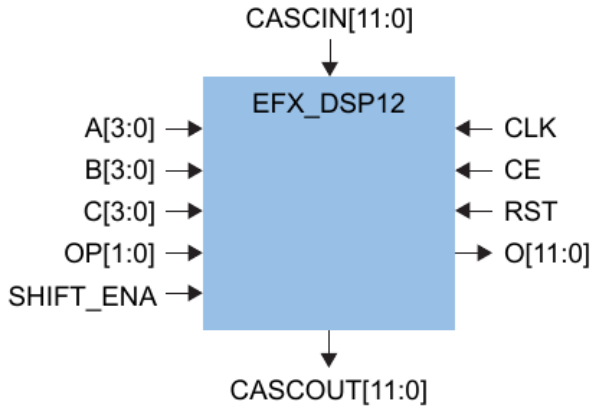
- XLR
- Embedded Memory
- DSP Block
- Global Network



DSP Block - Primitive



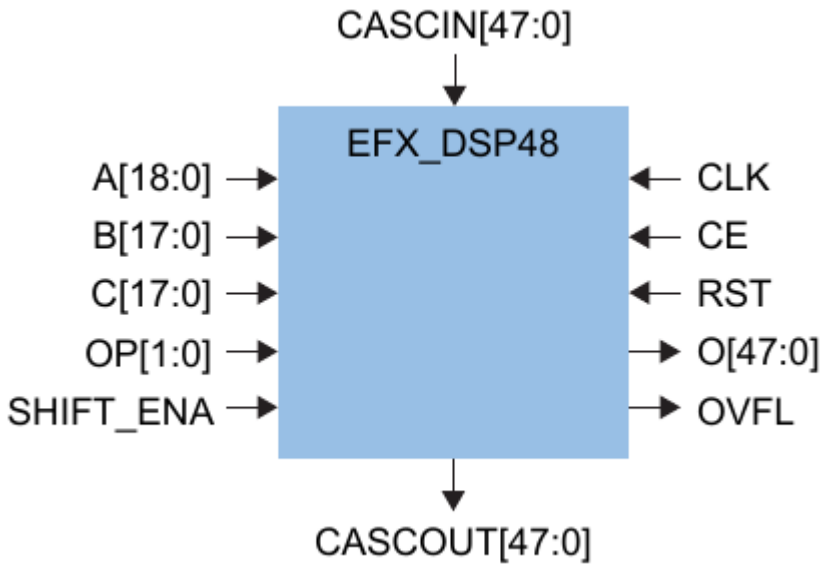




EFX_DSP48元语-支持模式

- Normal—配置为1个带48bit加法/减法的19X18整数乘法，可配置为有符号运算和无符号运算
- Dual—配置为1个11X10整数乘法和1个8X8整数乘法，带2个24位加法/减法，可配置为有符号运算和无符号运算，符号设定同时对一个block内所有运算有效
- Quad—配置为1个7 x 6整数乘法和3个4X4整数乘法，带4个12位加法/减法，可配置为有符号运算和无符号运算，符号设定同时对一个block内所有运算有效
- Float—配置为支持BFLOAT16浮点格式的FMA（Fused-multiply-add/subtract/accumulate）融合乘加器

EFX_DSP48元语

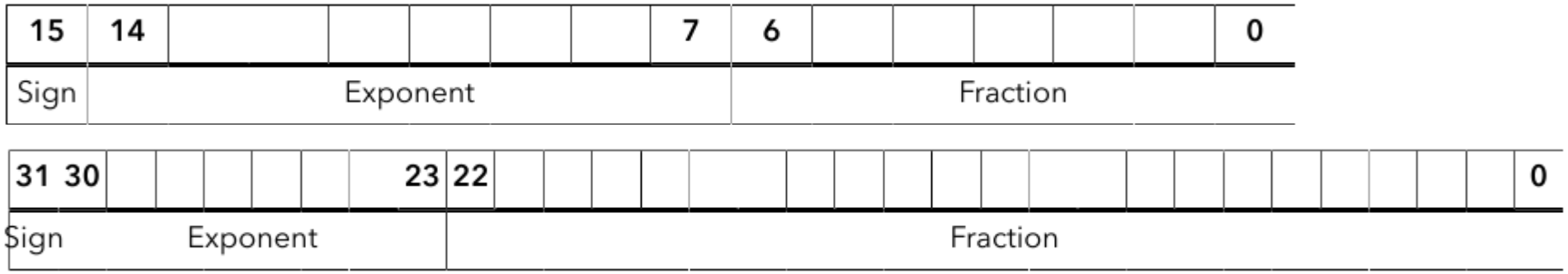


Port Name	Direction	Description
A[18:0]	Input	Operand A.
B[17:0]	Input	Operand B.
C[17:0]	Input	Operand C.
OP[1:0]	Input	Add/subtract function control. 00: M + N 01: M - N 10: -M + N 11: -M - N
SHIFT_ENA	Input	Load the shifter register S from the C input.
CASCIN[47:0]	Input	Dedicated input from the DSP block below.
CLK	Input	Clock.
CE	Input	Clock enable.
RST	Input	Set/reset.
O[47:0]	Output	DSP output.
CASCOUT[47:0]	Output	Dedicated output to the DSP block above.
OVFL	Output	Overflow/underflow flag.

EFX_DSP48-不同模式的端口划分

MODE	Multiplier Size	A	B	C	Shift	O
NORMAL	19 x 18	A[18:0]	B[17:0]	C[17:0]	C[3:0]	O[47:0]
DUAL	11 x 10	A[18:8]	B[17:8]	C[17:8]	C[7:4]	O[47:24]
	8 x 8	A[7:0]	B[7:0]	C[7:0]	C[3:0]	O[23:0]
QUAD	7 x 6	A[18:12]	B[17:12]	C[17:12]	C[15:12]	O[47:36]
	4 x 4	A[11:8]	B[11:8]	C[11:8]	C[11:8]	O[35:24]
	4 x 4	A[7:4]	B[7:4]	C[7:4]	C[7:4]	O[23:12]
	4 x 4	A[3:0]	B[3:0]	C[3:0]	C[3:0]	O[11:0]
BFLOAT	16 x 16	A[15:0]	B[15:0]	C[15:0]	N/A	O[47:0]

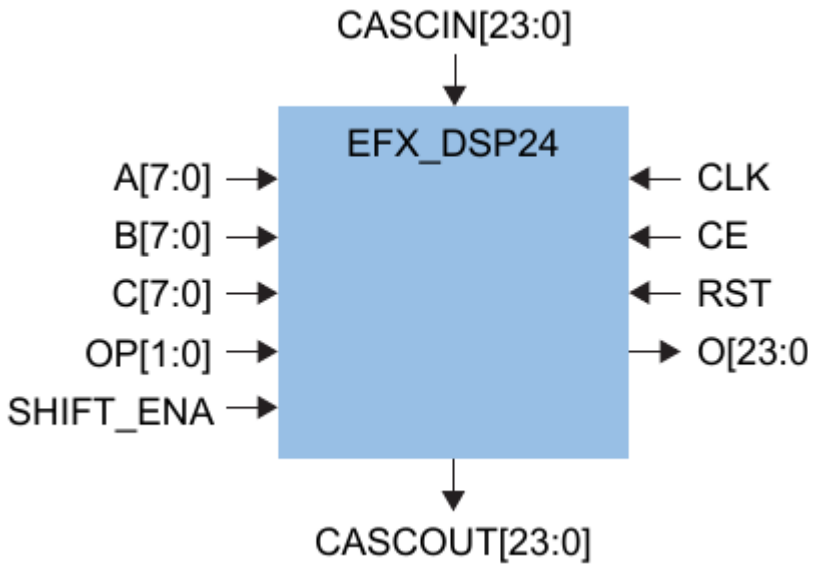
EFX_DSP48-BFLOAT MODE



- BFLOAT16是介于FP16和FP32之间的浮点数格式。 BF16的指数位比FP16多，跟FP32一样，不过小数位比较少。通过降低精度的方式，来获得更大的数值空间。
- BF16格式的浮点数已经成为AI深度学习事实上的标准。

Dual-Mode 8 x 8 DSP Block

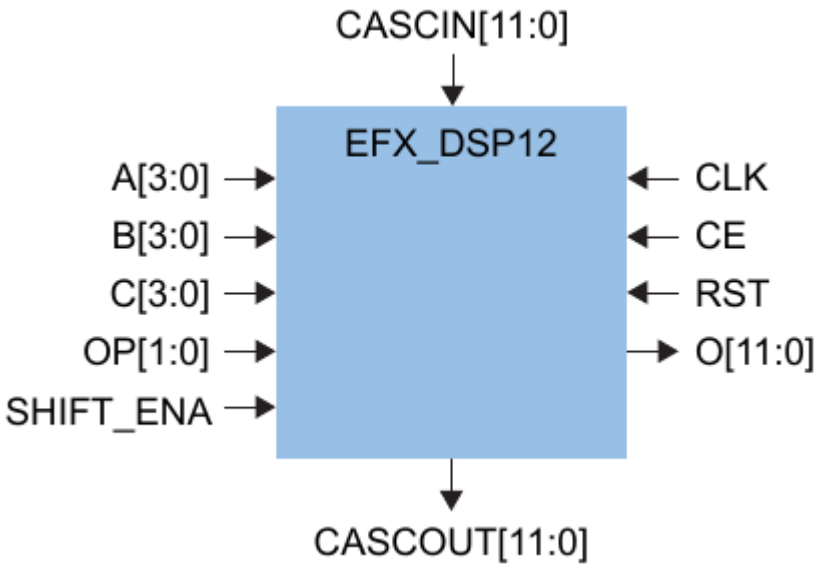
- 调用EFX_DSP24元语，可例化为两个独立的8X8



Port Name	Direction	Description
A[7:0]	Input	Operand A.
B[7:0]	Input	Operand B.
C[7:0]	Input	Operand C.
OP[1:0]	Input	Add/subtract function control 00: M + N 01: M - N 10: -M + N 11: -M - N
SHIFT_ENA	Input	Load the shifter register S from the C input.
CASCIN[23:0]	Input	Dedicated input from the DSP block below.
CLK	Input	Clock.
CE	Input	Clock enable.
RST	Input	Set/reset.
O[23:0]	Output	DSP output.
CASCOUT[23:0]	Output	Dedicated output to the DSP block above.

Quad-Mode 4 x 4 DSP Block

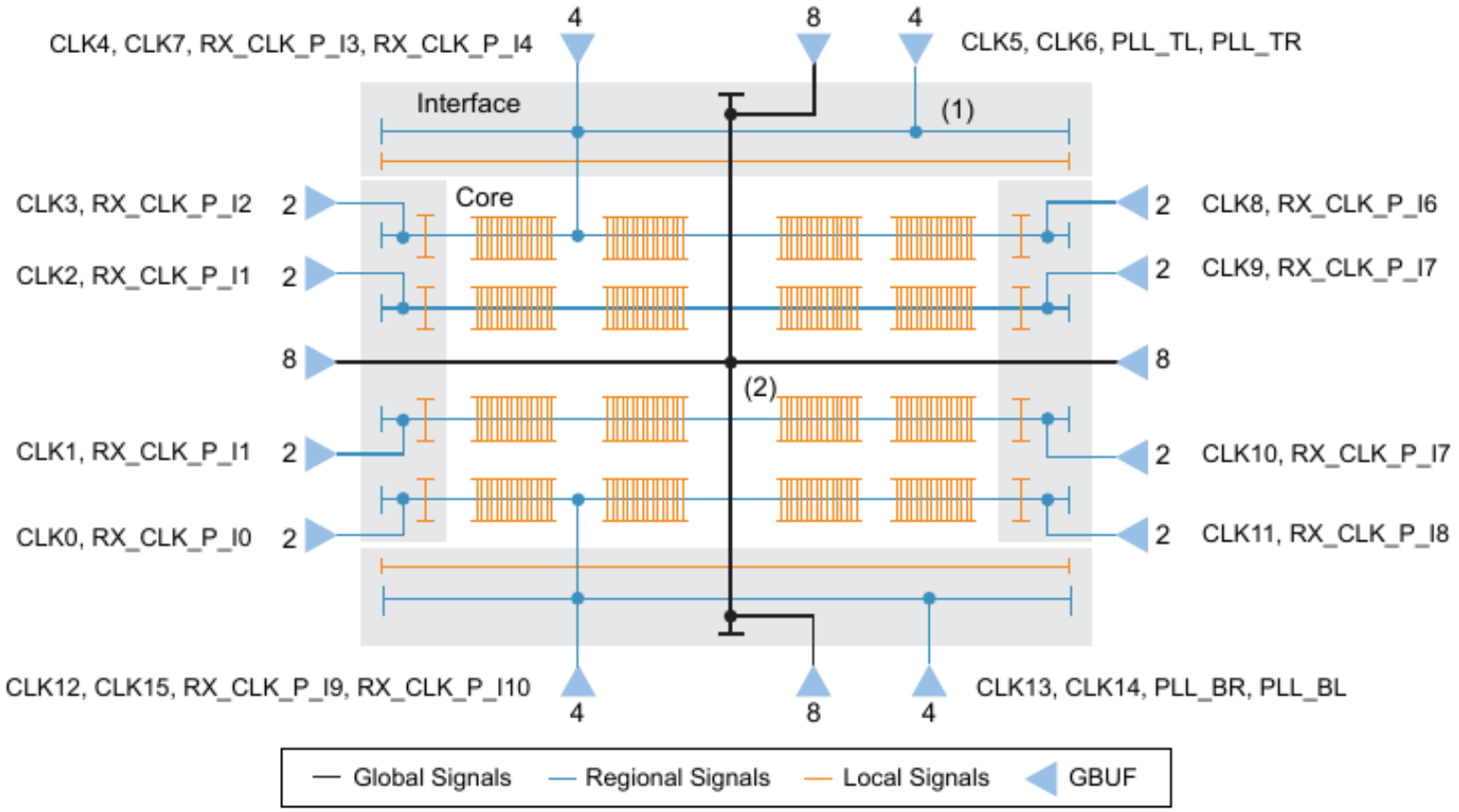
- 调用EFX_DSP12元语，可例化为4个独立的4X4



Port Name	Direction	Description
A[3:0]	Input	Operand A.
B[3:0]	Input	Operand B.
C[3:0]	Input	Operand C.
OP[1:0]	Input	Add/subtract function control. 00: M + N 01: M - N 10: -M + N 11: -M - N
SHIFT_ENA	Input	Load the shifter register S from the C input.
CASCIN[11:0]	Input	Dedicated input from the DSP block below.
CLK	Input	Clock.
CE	Input	Clock enable.
RST	Input	Set/reset.
O[11:0]	Output	DSP output.
CASCOUT[11:0]	Output	Dedicated output to the DSP block above.

Core Function

- XLR
- Embedded Memory
- DSP Block
- Global Network



1. Each blue horizontal line represents a region.
2. The number of local signals shown is for illustration only.

Global Network

- 32个全局信号
  - 上下左右各8个
- 6个局域信号
  - 左右两边的interface block和core有4个局域信号
  - 上下两边的interface block各有1个局域信号

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

- HVIO（High-voltage I/O）
  - 支持高电压单端信号
- HSIO（High-speed I/O）
  - 支持低电压高速单端和差分信号

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GPIO

Resource		W64	F100	F225
Single-ended GPIO (Max)	HVIO (1.8, 2.5, 3.0, 3.3 V LVCMOS, 3.0, 3.3 V LVTTL)	-	-	23
	HSIO (1.2, 1.5, 1.8 V LVCMOS, HSTL and SSTL)	35	61	140
Differential GPIO (Max)	HSIO (LVDS, Differential HSTL, SSTL, MIPI TX Data and Clock Lanes)	17	30	70
	HSIO (MIPI RX Data Lanes)	8	21	58
	HSIO (MIPI RX Clock Lanes)	2	3	12
Global clock or control signals from GPIO pins		3	8	15
PLLs		2	3	4

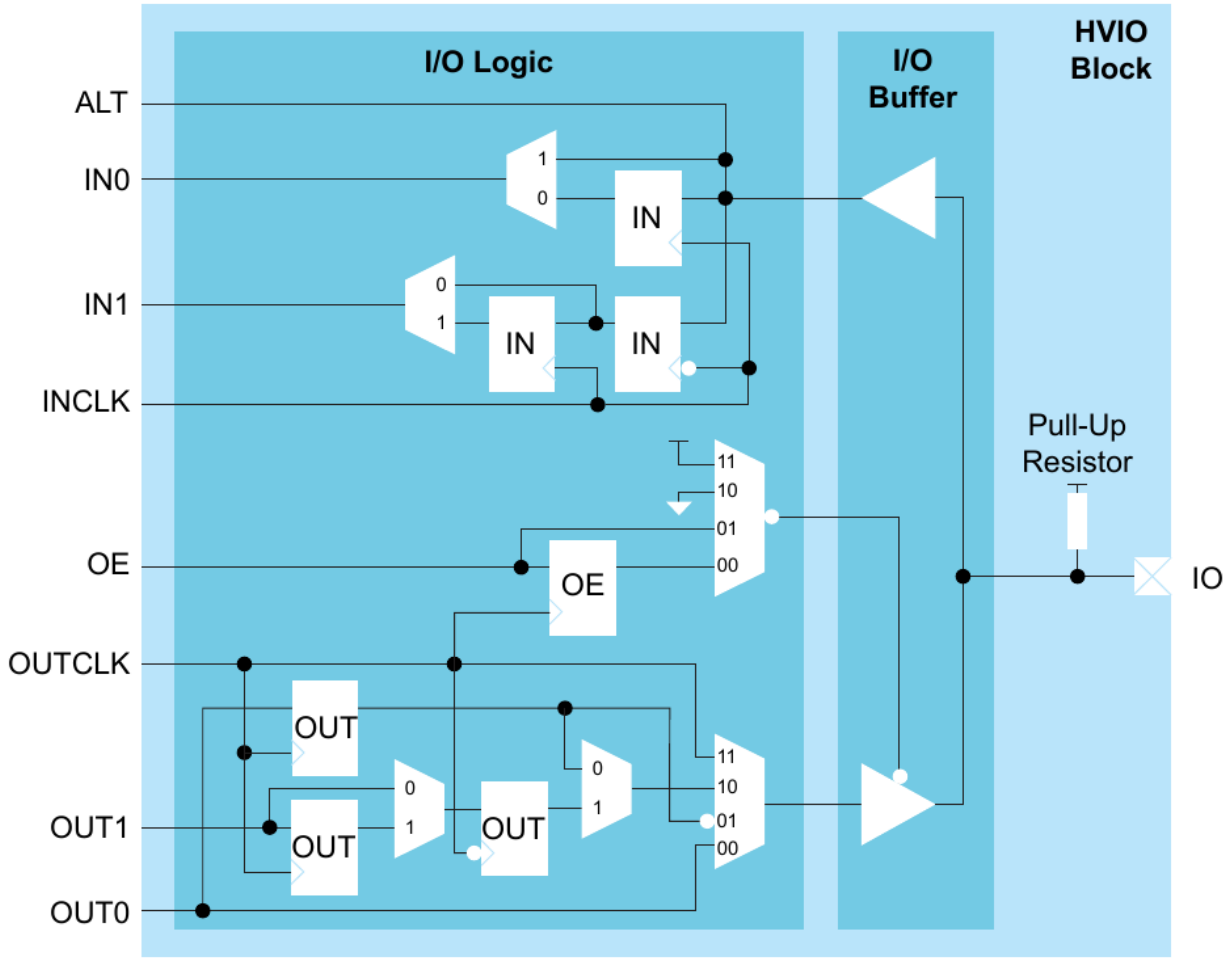
GPIO

Feature	HVIO	HSIO Configured as GPIO
Double-data I/O (DDIO)	✓	✓
Dynamic pull-up	–	✓
Pull-up/Pull-down	✓	✓
Slew-Rate Control	–	✓
Variable Drive Strength	✓	✓
Schmitt Trigger	✓	✓
1:4 Serializer/Deserializer (Full rate mode only)	–	✓
Programmable Bus Hold	–	✓
Static Programmable Delay Chains	✓	✓
Dynamic Programmable Delay Chains	–	✓

HVIO(High-voltage I/O)

Standard	VCCIO33 (V)	When Configured As
LVTTL 3.3 V	3.3	GPIO
LVTTL 3.0 V	3.0	GPIO
LVCMOS 3.3 V	3.3	GPIO
LVCMOS 3.0 V	3.0	GPIO
LVCMOS 2.5 V(5)	2.5	GPIO
LVCMOS 1.8 V	1.8	GPIO

HVIO(High-voltage I/O)



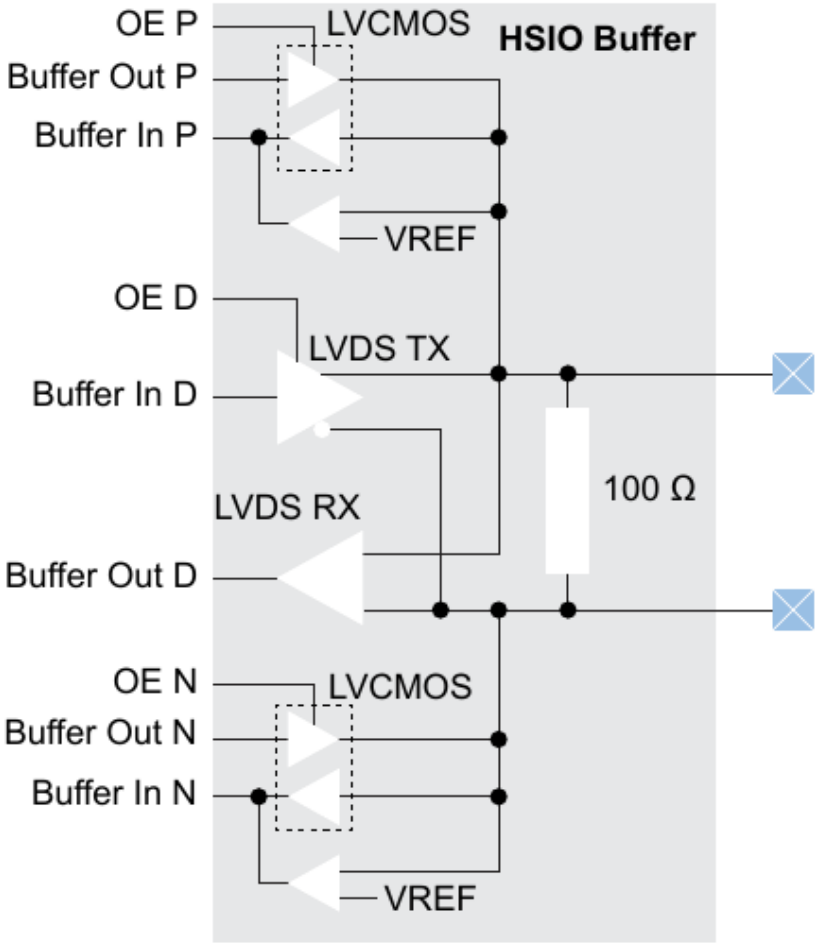
HSIO(High-speed I/O)

Standard	VCCIO (V)		VCCAUX (V)	VREF (V)	When Configured As
	TX	RX			
LVCMOS 1.8 V	1.8	1.8	1.8	–	GPIO
LVCMOS 1.5 V	1.5	1.5	1.8	–	GPIO
LVCMOS 1.2 V	1.2	1.2	1.8	–	GPIO
HSTL/Differential HSTL 1.8 V SSTL/Differential SSTL 1.8 V	1.8	1.8	1.8	0.9	GPIO
HSTL/Differential HSTL 1.5 V SSTL/Differential SSTL 1.5 V	1.5	1.5, 1.8	1.8	0.75	GPIO
HSTL/Differential HSTL 1.2 V SSTL/Differential SSTL 1.2 V	1.2	1.2, 1.5, 1.8	1.8	0.6	GPIO
LVDS/RSDS/mini-LVDS	1.8	1.8	1.8	–	LVDS
Sub-LVDS	1.8	1.5, 1.8	1.8	–	LVDS
MIPI D-PHY Lane I/O /SLVS	1.2	1.2	1.8	–	MIPI D-PHY

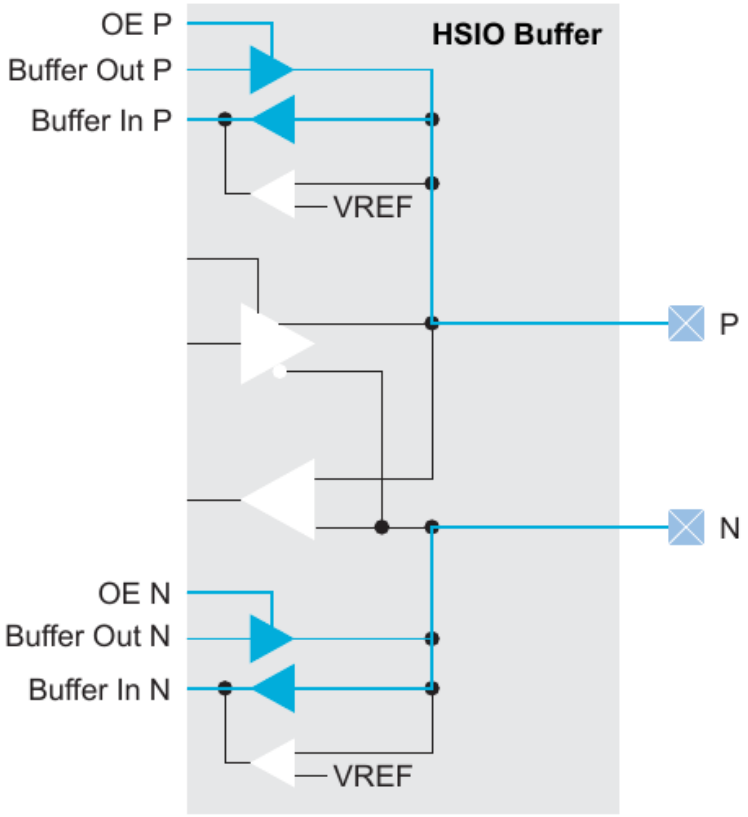
HSIO(High-speed I/O)

- Single-ended HSIO—Two single-ended I/O pins (LVCMOS, SSTL, HSTL)
- Differential HSIO—One differential I/O pins
  - Differential SSTL and HSTL
  - LVDS—Receiver (RX), transmitter (TX), or bidirectional (RX/TX)
  - MIPI D-PHY lane I/O—Receiver (RX) or transmitter (TX)
- The HSIO configured as GPIO supports programmable delay chain. You can use static and dynamic delays at the same time.
  - Static—16 steps with approximately 60ps of delay per step, both input and output paths.
  - Dynamic—64 steps with approximately 25ps of delay per step, input only. Only available on input (RX) delay; available only on P input of the HSIO pin pair.

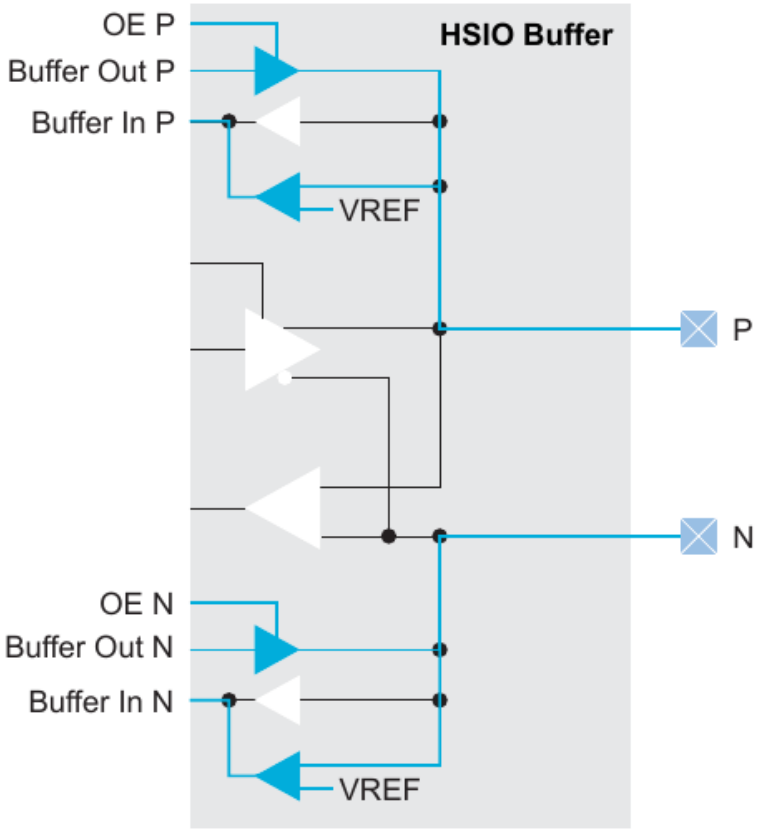
HSIO(High-speed I/O)-IO buffer



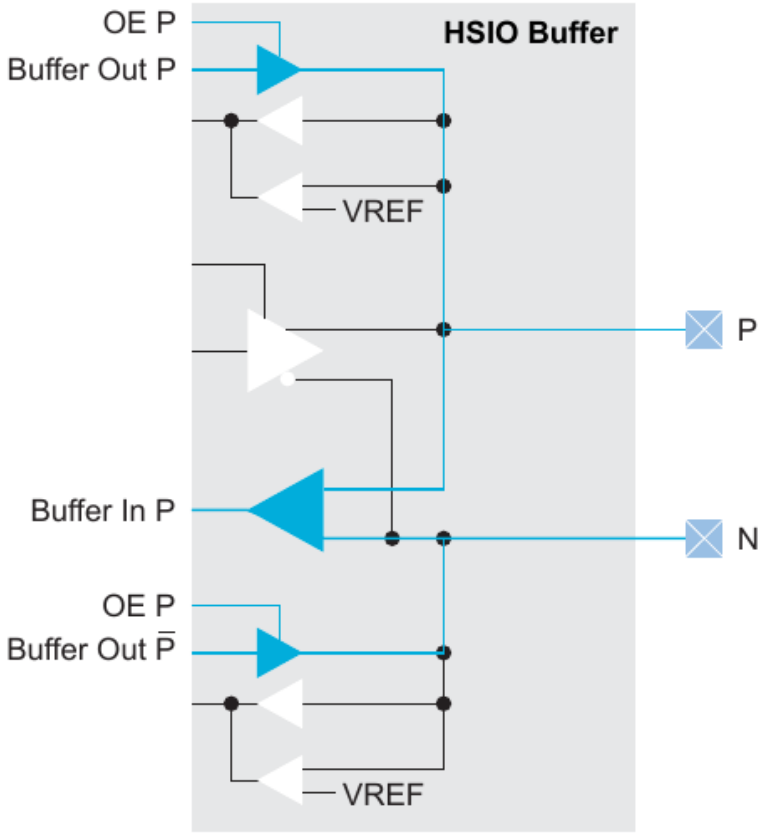
HSIO(High-speed I/O)-IO buffer



LVCMOS/LVTTL

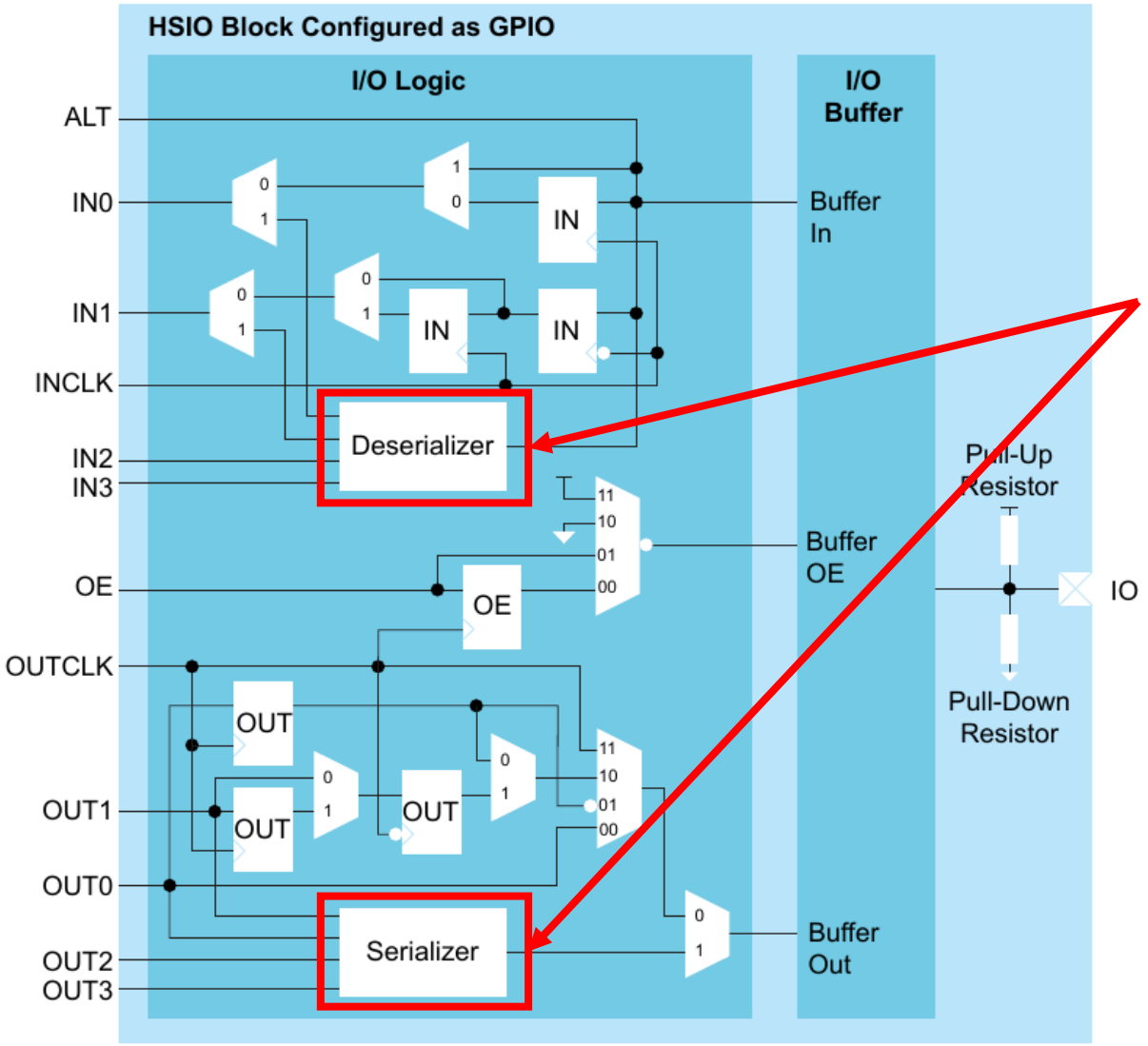


单端HSTL/SSTL



差分HSTL/SSTL

HSIO(High-speed I/O)-I/O Logic



支持串并1:4/并串变换4:1
(Full rate mode only)

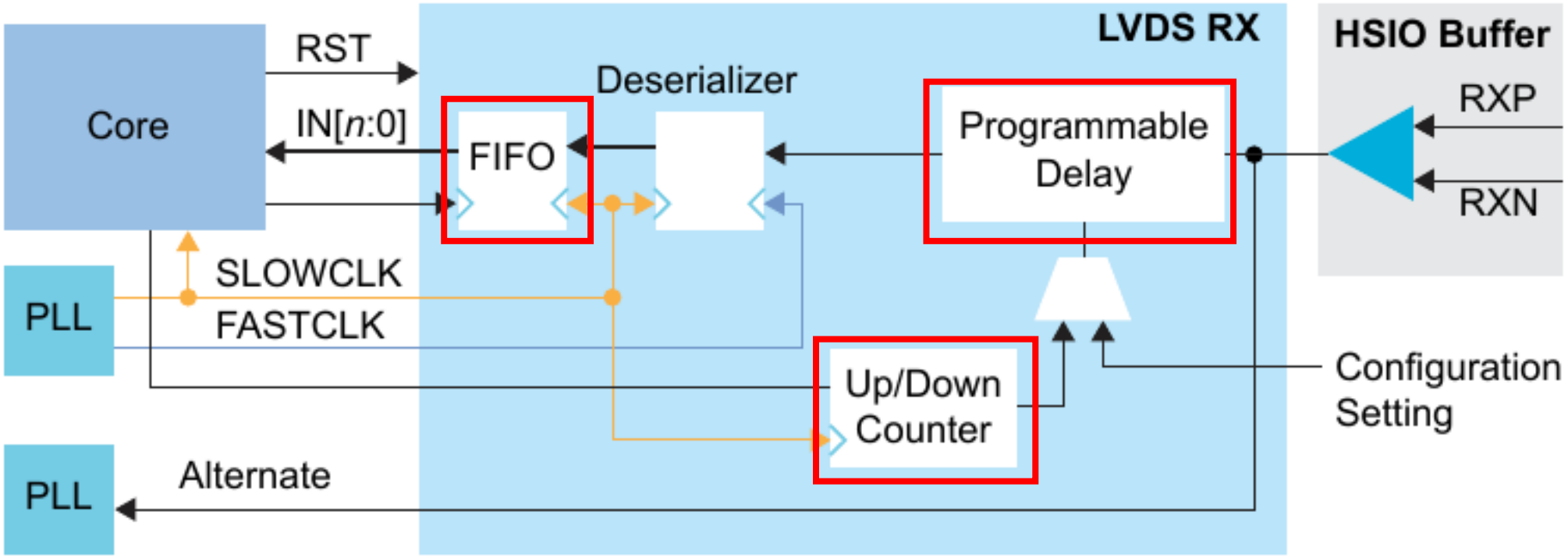
HSIO(High-speed I/O)-LVDS

- Programmable VOD, depending on the I/O standard used.
- Programmable output common mode (1.2 V for LVDS and 0.9 V for sub-LVDS) or with an external VREF. The shared VREF for the I/O bank provides the VREF.
- Programmable pre-emphasis.
- Programmable 100 Ω termination to save power (you can enable or disable it at runtime).
- LVDS input enable to dynamically enable/disable the LVDS input.
- Support for full rate or half rate serialization.
- Up to 10-bit serialization to support protocols such as 8b10b encoding.
- Programmable delay chains.
- Optional 8-word FIFO for crossing from the parallel (slow) clock to the user's core clock to help close timing (RX only).

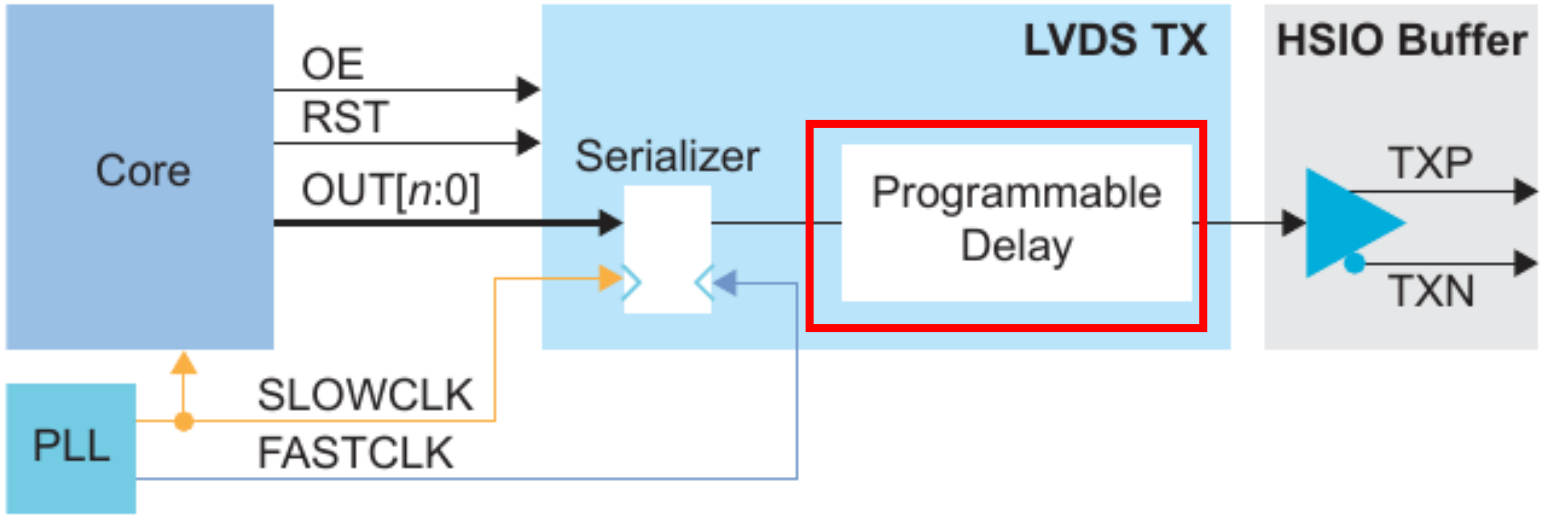
HSIO(High-speed I/O)-LVDS

Mode	Description	Example
Full rate clock	In full rate mode, the fast clock runs at the same frequency as the data and captures data on the positive clock edge.	Data rate: 800 Mbps Serialization/Deserialization factor: 8 Slow clock frequency: 100 Mhz (800 Mbps / 8) Fast clock frequency: 800 Mhz
Half rate clock	In half rate mode, the fast clock runs at half the speed of the data and captures data on both clock edges.	Data rate: 800 Mbps Serialization / Deserialization factor: 8 Slow clock frequency: 100 Mhz (800 Mbps / 8) Fast clock frequency: 400 Mhz (800 / 2)

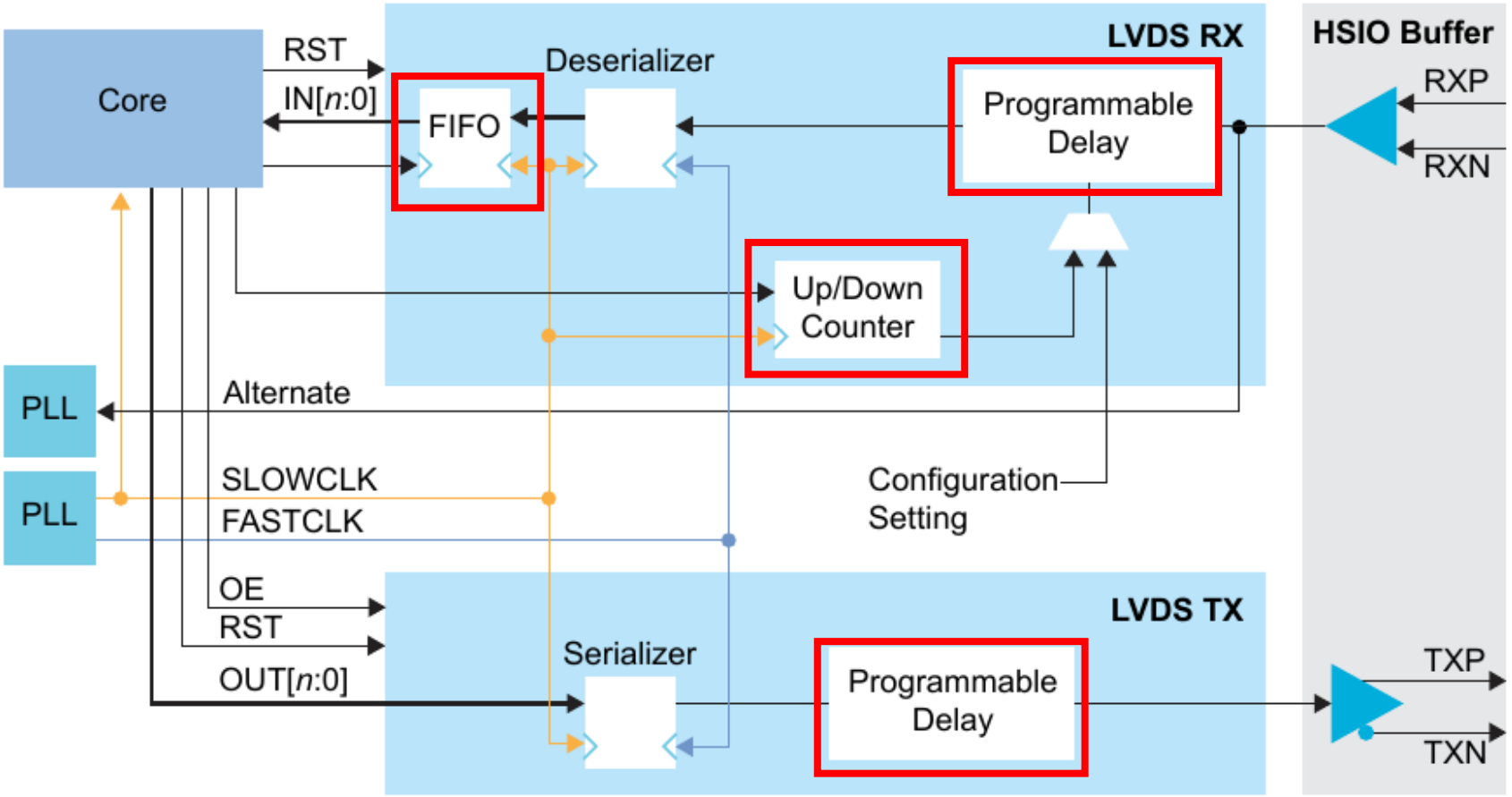
HSIO(High-speed I/O)-LVDS RX



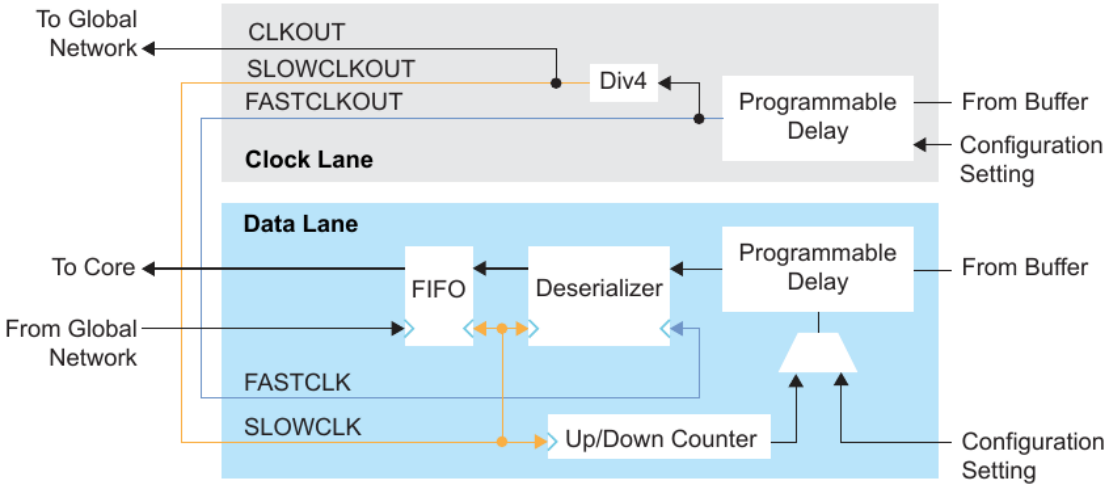
HSIO(High-speed I/O)-LVDS TX

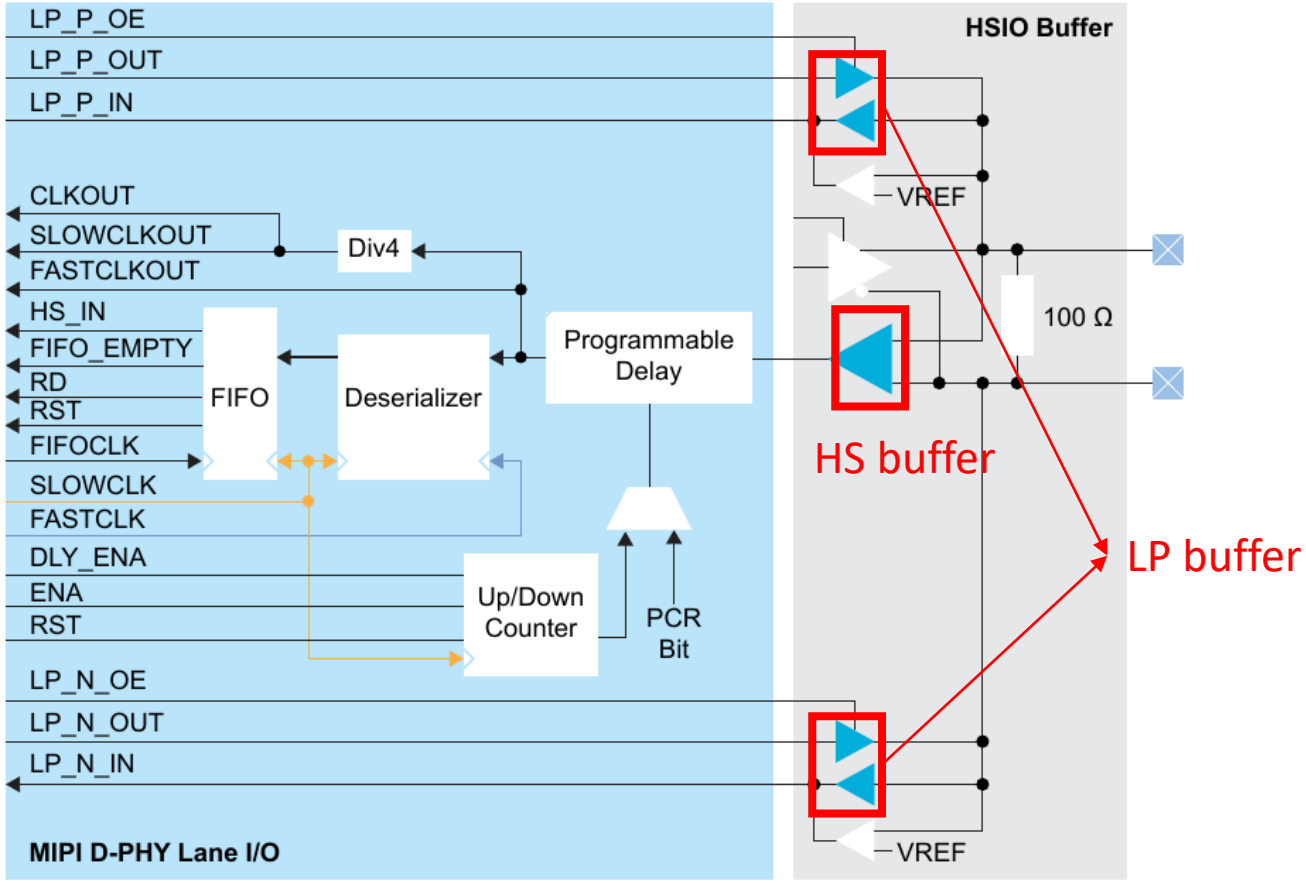


HSIO(High-speed I/O)-LVDS Bidirectional

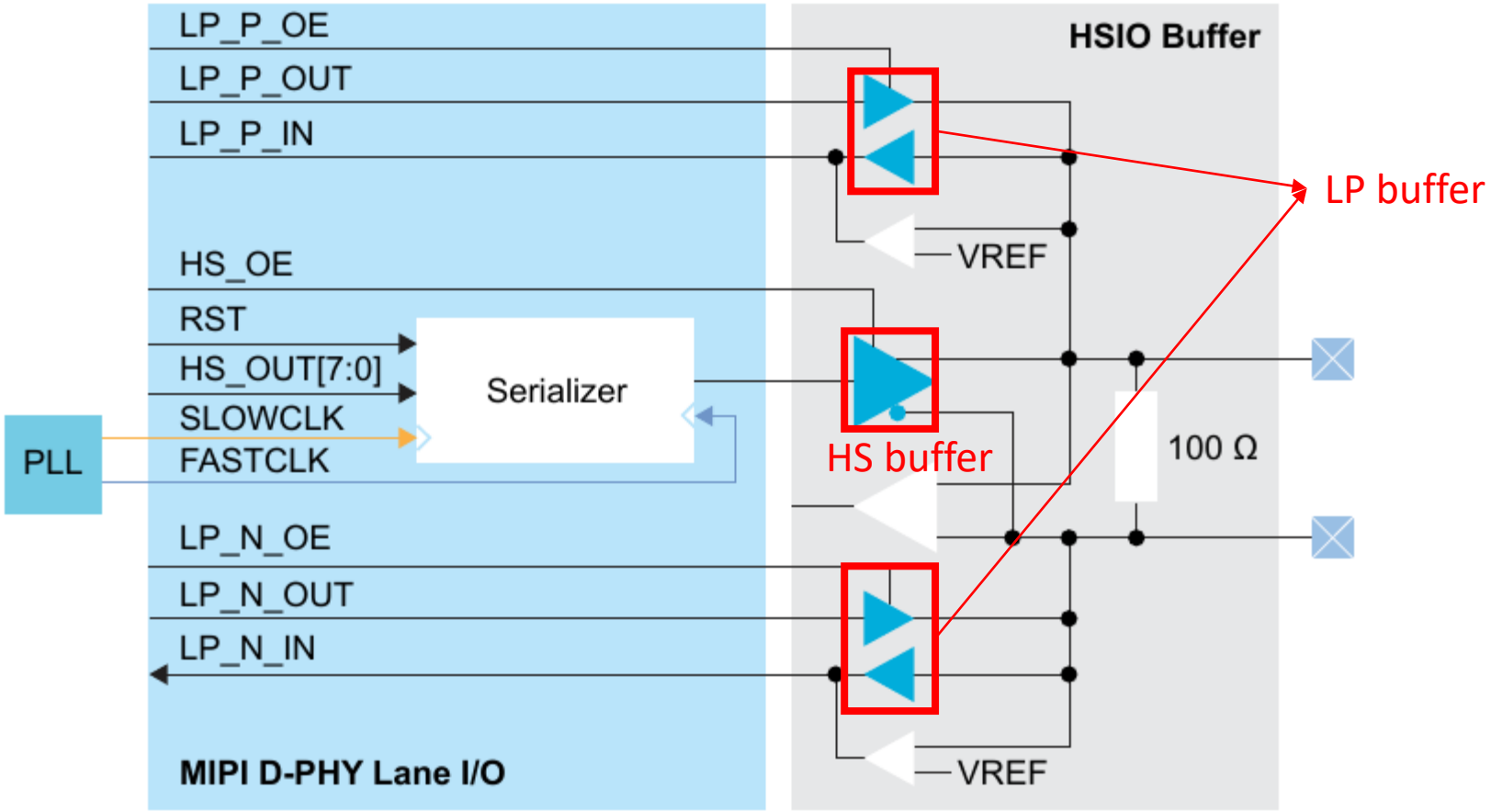


HSIO(High-speed I/O)- MIPI D-PHY RX Lane



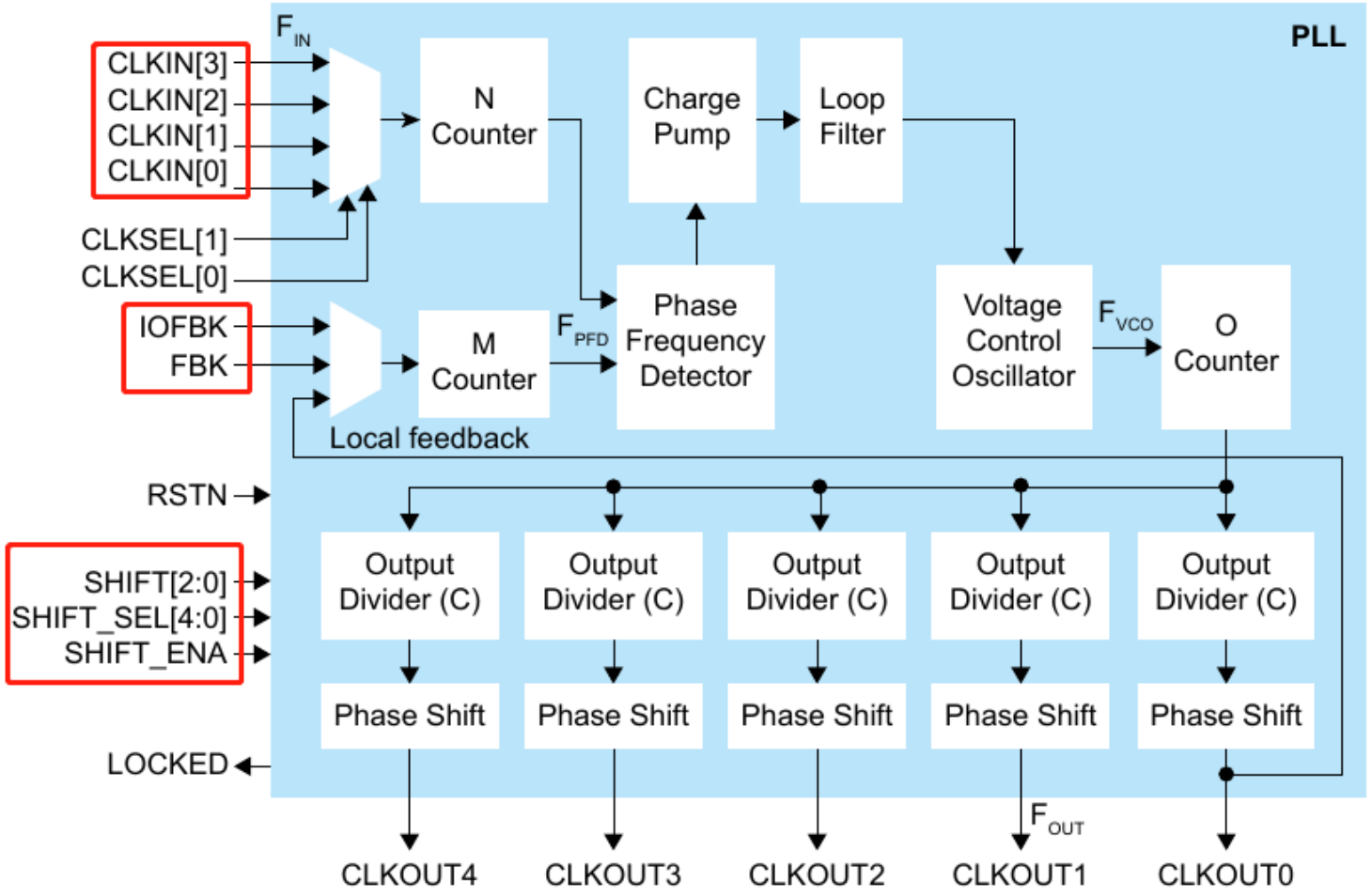


HSIO(High-speed I/O)- MIPI D-PHY TX Lane



Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller



PLL

- Ti60/Ti35最多支持4个锁相环
  - F225：4
  - F100：3
  - W64：2
- 支持内部反馈，外部反馈和IO反馈
- 每个锁相环支持4个参考时钟输入，并且支持动态切换
- 钛金系列 FPGA每个锁相环支持5路输出，支持输出时钟动态相位调整

PLL

Symbol	Parameter	Min	Typ	Max	Units
F_{IN}	Input clock frequency.	16	-	800	MHz
F_{OUT}	Output clock frequency.	-	-	1,000	MHz
F_{VCO}	PLL VCO frequency.	2,200	-	5,500	MHz
F_{PFD}	Phase frequency detector input frequency.	16	-	800	MHz

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

- Ti60/Ti35有一个为低功耗应用量身定制的片上低频振荡器。
- 输出可配置为10, 20, 40, 80 MHz.
- 可在超低功耗设计中执行always-on功能。
- 时钟输出到core逻辑

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
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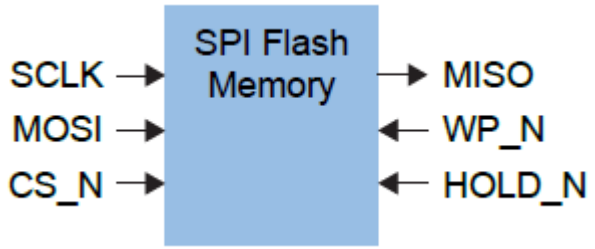


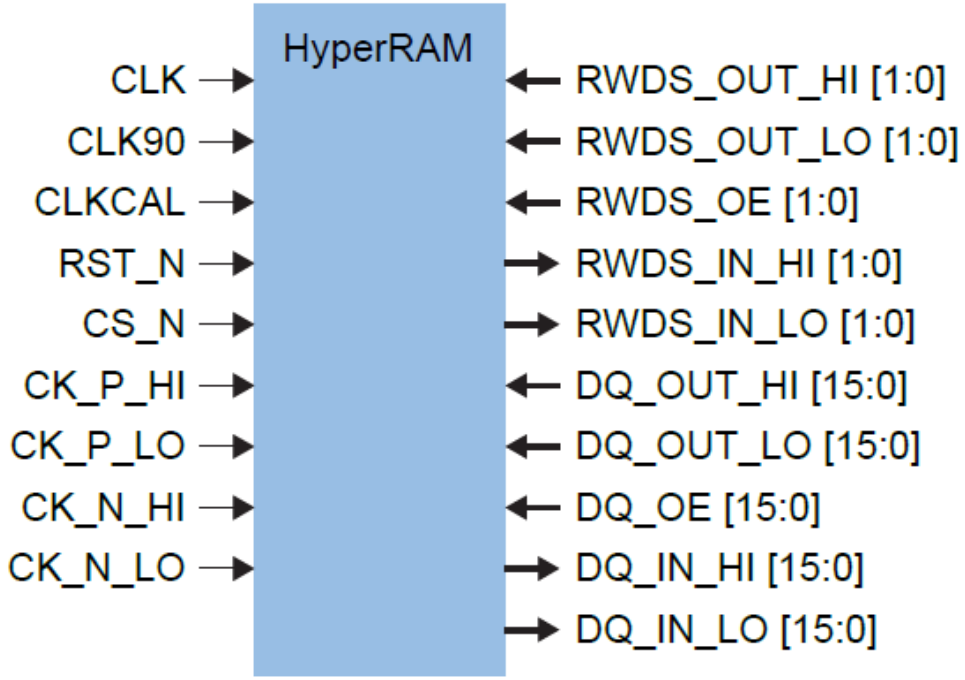
Signal	Direction	Description
SCLK	Input	Clock output to SPI flash memory.
MOSI	Input	Data output to SPI flash memory.
CS_N	Input	Active-low SPI flash memory chip select.
WP_N	Input	Active-low write protect signal.
HOLD_N	Input	Active-low hold signal.
MISO	Output	Data input from SPI flash memory.

- 只有FBGA100 支持片内 SPI FLASH
- FLASH容量：16Mbits
- 采用Bitstream压缩，最多可支持两个镜像
- 最大工作频率85Mhz
- 通过JTAG Bridge模式烧写FLASH

易 灵 思

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller



- 只有FBGA100 支持片内HyperRAM
- HyperRAM容量256Mbit
- 16位数据位宽
- 总带宽16X400Mbps=6.4Gbps

易 灵 思

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

- 单粒子翻转(SEU) 检测功能
- Auto mode—控制模块自动周期性的检查SEU错误，如果检查到错误，输出错误标志。检测时间间隔可配置
- Manual mode—用户控制是否检测，何时检测
- 当SEU检测模块输出错误标志以后，由用户逻辑决定是否重新配置FPGA

Interface Function

- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

易 灵 思

- 内部重配置功能
- 同Trion

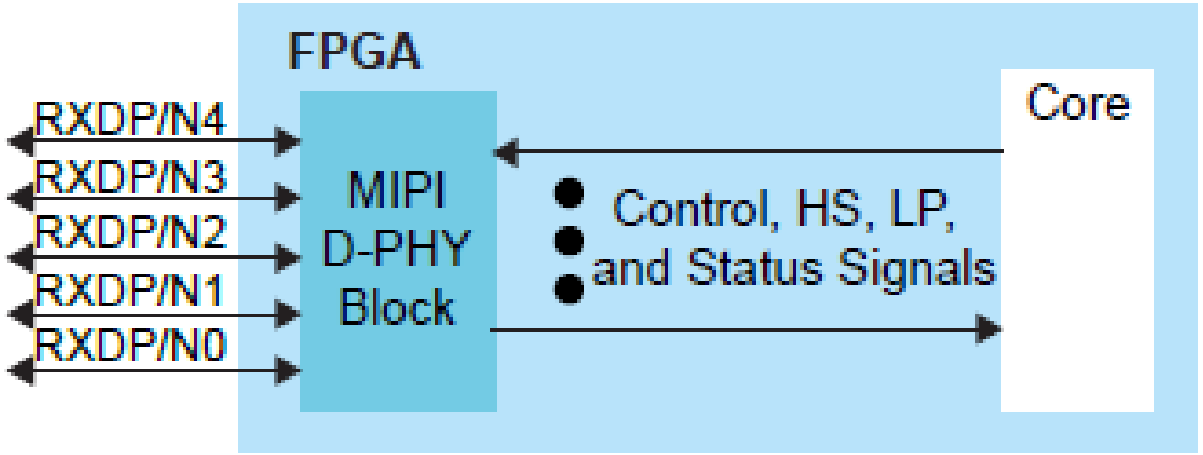
Interface Function

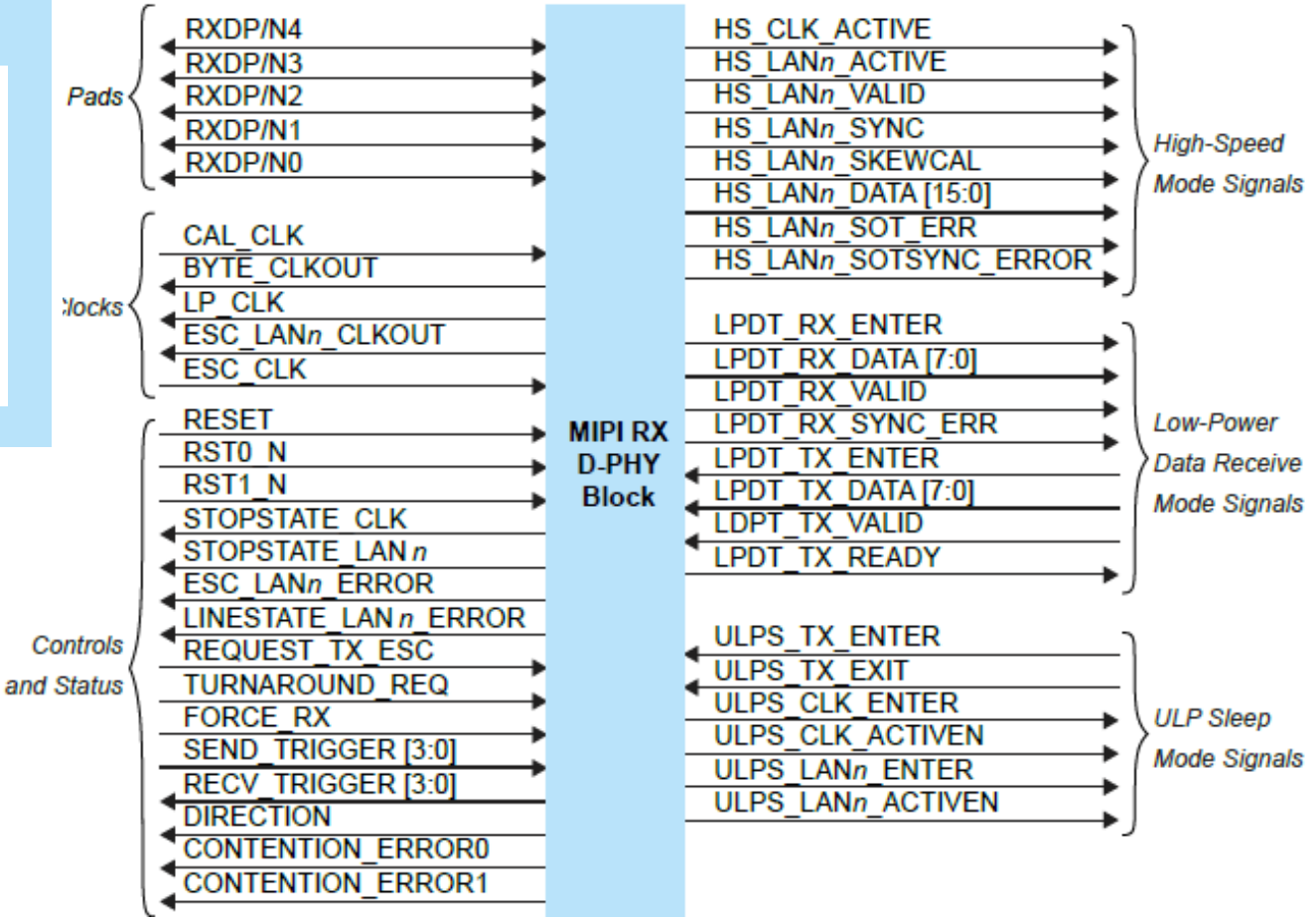
- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

易 灵 思

- Programmable data lane configuration supporting up to 4 lanes
- High-speed mode supports up to 2.5 Gbps data rates per lane
- Operates in continuous and non-continuous clock modes
- Supports Ultra-Low Power State (ULPS)

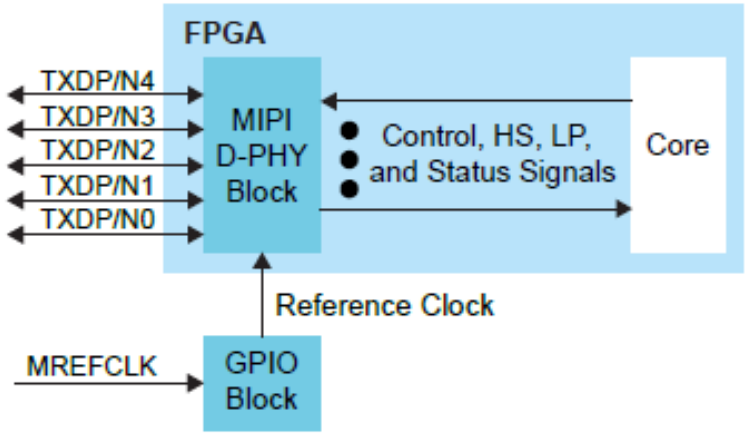
MIPI RX D-PHY



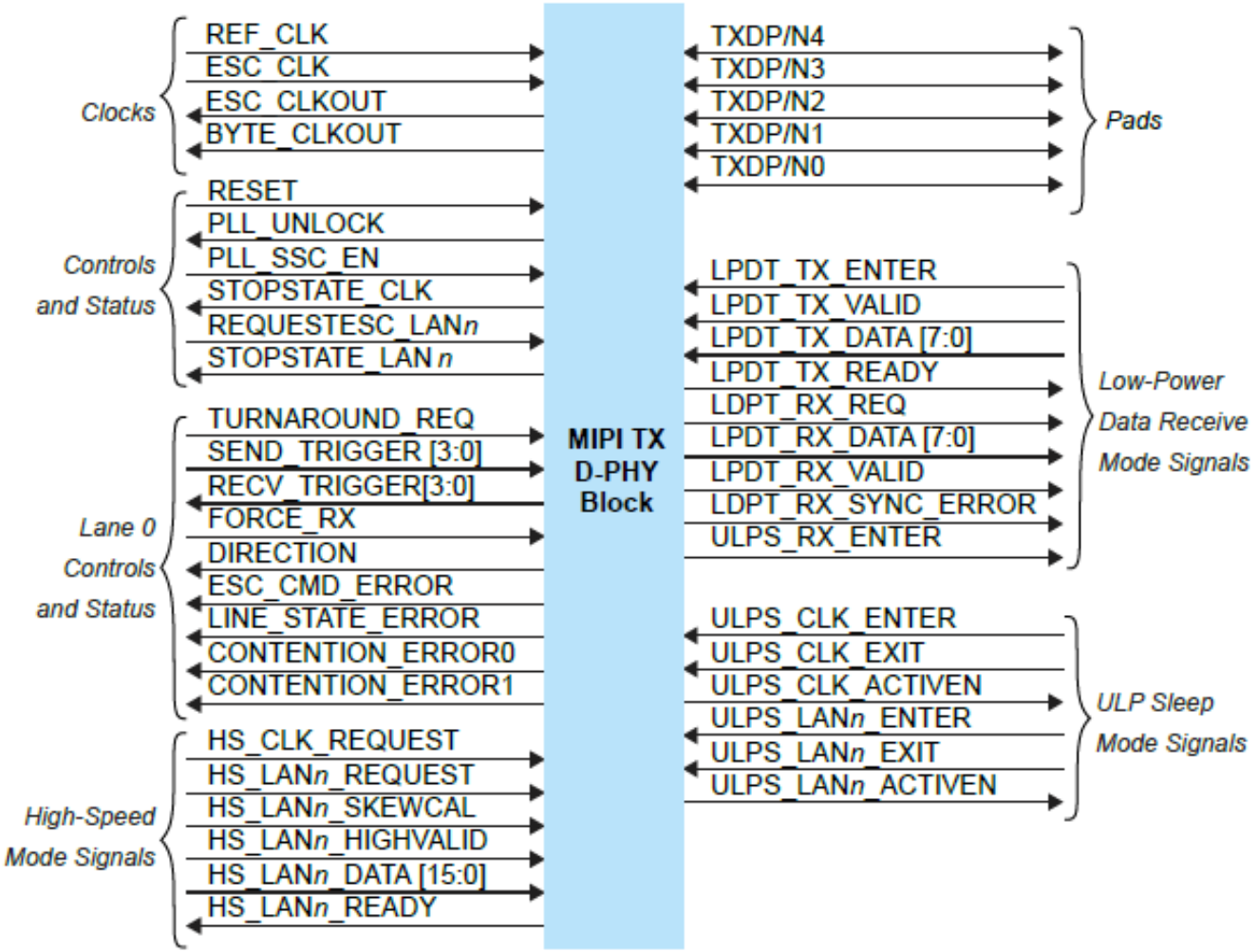


- 钛金系列的2.5G RX MIPI-DPHY的IO是MIPI RX专用管脚，不可用作普通GPIO
- 每个通道4个RX data lane+1个RX clock lane，支持Lane之间线线序交换
- 独立的RX D-PHY功能，和core逻辑的CSI/DSI RX控制器IP可构建高达2.5G的高速MIPI RX接口
- 同TRION FPGA不同，不再同协议部分（CSI控制器）绑定，更加灵活，可根据需要用逻辑资源灵活构建各种基于MIPI RX-DPHY的控制器。

MIPI TX D-PHY



- 钛金系列的2.5G TX MIPI-DPHY的IO是MIPI TX专用管脚，不可用作普通GPIO
- 每个通道4个TX data lane+1个TX clock lane，支持Lane之间线下交换
- 独立的TX D-PHY功能，和core逻辑的CSI/DSI TX控制器IP可构建高达2.5G的高速MIPI TX接口
- 同TRION FPGA不同，不再同协议部分（CSI控制器）绑定，更加灵活，可根据需要用逻辑资源灵活构建各种基于MIPI TX-DPHY的控制器。
  - 可构建MIPI DSI TX接口，驱动OLED显示屏。



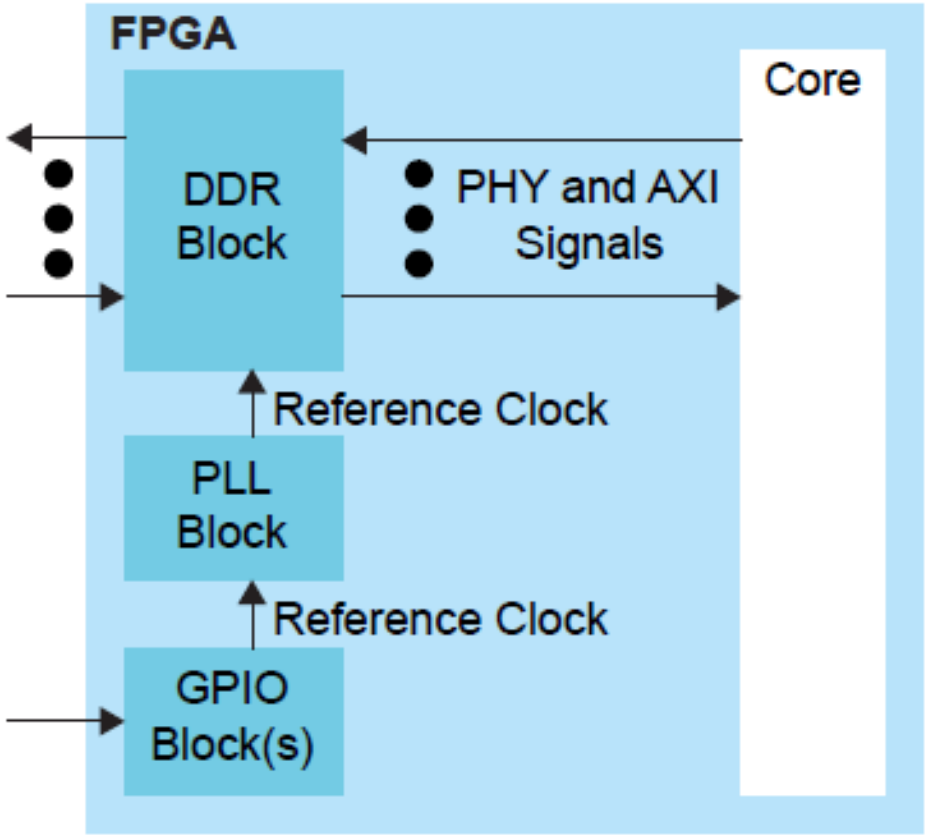
Interface Function

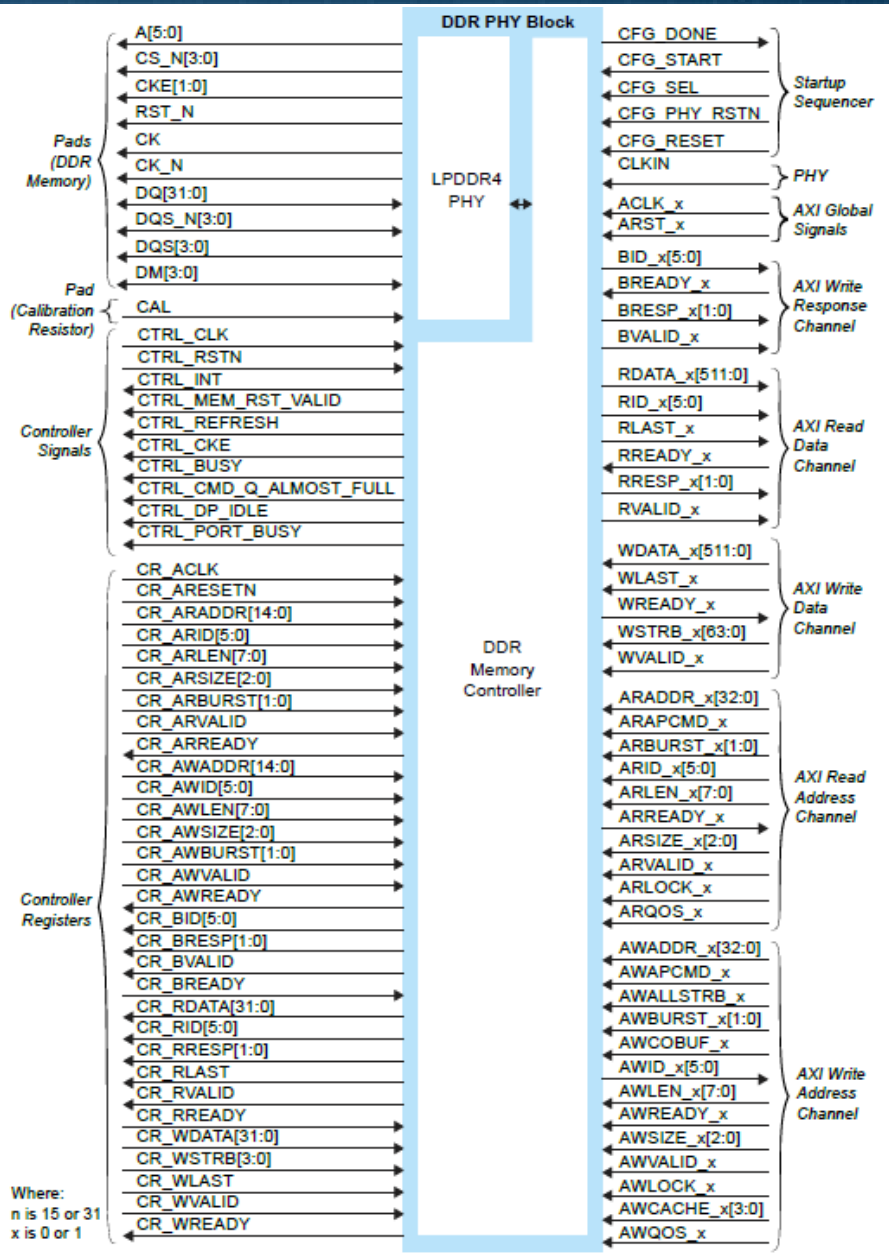
- GPIO
- PLL
- Oscillator
- SPI FLASH
- HyperRAM
- SEU detection
- Internal Reconfiguration Block
- MIPI DPHY
- LPDDR4/4X Controller

易灵思

- 全硬核
- LPDDR4/LPDDR4x
- 2个面向Core逻辑的，独立的AXI4全双工接口
- X16/X32 DQ位宽
- ~4266Mbps（理想最大速率，实际TBD）
- ~136Gbps（最大理想带宽，实际TBD）

LPDDR4/4X Controller





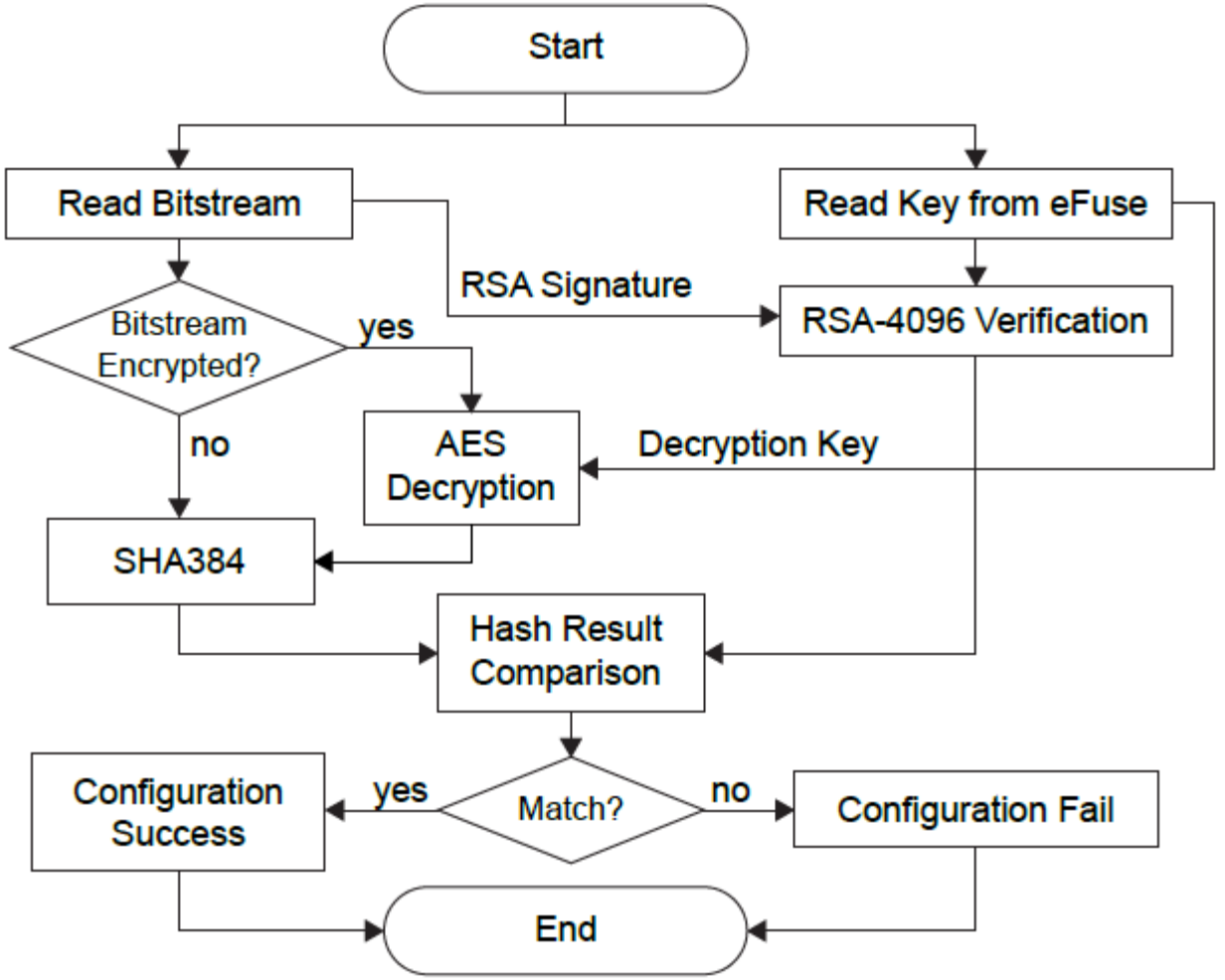
易 灵 思

Security Feature

- 位流加密
- 对称和非对称位流认证
- AES-GCM
- RSA-4096
- 位流加密不能和位流压缩同时使用
- JTAG Disable功能
  - 一旦Disable无法恢复
  - 只能读取IDCODE，或者使用JTAG Bypass模式进行边界扫描

易 灵 思

解密流程



The End