易灵思

# Trion® Packaging User Guide

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# Introduction

易灵思 offers Trion® FPGAs in packages that are designed for the devices' maximum number of user's I/O pins. This document describes the Trion® FPGAs' pin and package specifications as well as solder reflow guidelines.

**Learn more:** Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

## Available Package Options

**Table 1: Available Packages**

| Package | Dimensions (mm x mm) | Pitch (mm) |
|---|---|---|
| **T4/T8 FPGAs** | | |
| 49-ball FBGA[1] | 3 x 3 | 0.4 |
| 81-ball FBGA | 5 x 5 | 0.5 |
| **T20 FPGAs** | | |
| 80-ball WLCSP | 4.5 x 3.6 | 0.4 |
| **T8/T20 FPGAs** | | |
| 144-pin LQFP | 20 x 20 | 0.5 |
| **T13/T20 FPGAs** | | |
| 100-pin LQFP | 14 x 14 | 0.5 |
| 169-ball FBGA | 9 x 9 | 0.65 |
| 256-ball FBGA | 13 x 13 | 0.8 |
| **T20/T35 FPGAs** | | |
| 324-ball FBGA | 12 x 12 | 0.65 |
| 400-ball FBGA | 16 x 16 | 0.8 |
| **T55/T85/T120 FPGAs** | | |
| 324-ball FBGA | 12 x 12 | 0.65 |
| 484-ball FBGA | 18 x 18 | 0.80 |
| 576-ball FBGA | 16 x 16 | 0.65 |

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

[1] This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

## Device Pinout File

易灵思 provides pinout files for Trion® FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

# Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

**Table 2: General Pinouts**

| Function | Group | Direction | Description |
|---|---|---|---|
| VCC | Power | – | Core power supply. |
| VCCA_xx | Power | – | PLL analog power supply. xx indicates the location. |
| VCCIOxx | Power | – | I/O pin power supply. xx indicates the bank location. |
| VCCIOxx_yy_zz | Power | – | I/O pin power supply.<br>Power for I/O banks that are shorted together. xx, yy, and zz are the bank locations. |
| GND | Ground | – | Ground. |
| CLKn | Alternate | Input | Global clock network input. n is the number. The number of inputs is package dependent. |
| CTRLn | Alternate | Input | Global network input used for high fanout and global reset. n is the number. The number of inputs is package dependent. |
| PLLIN | Alternate | Input | PLL reference clock. |
| GNDA_PLL | Ground | – | PLL ground pin. |
| MREFCLK | Alternate | Input | MIPI PLL reference clock source. |
| GPIOx_n | GPIO | I/O | General-purpose I/O for user function. User I/O pins are single-ended.<br>x: Indicates the bank (L or R)<br>n: Indicates the GPIO number. |
| GPIOx_n_yyy<br>GPIOx_n_yyy_zzz<br>GPIOx_zzzn | GPIO<br>Multi-Function | I/O | Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins.<br>x: (T4) Indicates the bank; left (L) or right (R).<br>x: (T13/T20) Indicates the bank; left (L), right (R), or bottom (B).<br>n: Indicates the GPIO number.<br>yyy, yyy_zzz: Indicates the alternate function.<br>zzzn: Indicates LVDS TX or RX and number. |
| TXNn, TXPn | LVDS | I/O | LVDS transmitter (TX). n: Indicates the number. |
| RXNn, RXPn | LVDS | I/O | LVDS receiver (RX). n: Indicates the number. |
| CLKNn, CLKPn | LVDS | I/O | Dedicated LVDS receiver clock input. n: Indicates the number. |
| RXNn_EXTFBn<br>RXPn_EXTFBn | LVDS | I/O | LVDS PLL external feedback. n: Indicates the number. |
| REF_RES | – | – | REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating. |

### Table 3: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

| Pins | Direction | Description | Use External Weak Pull-Up |
|---|---|---|---|
| CDONE | I/O | Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete. If you hold CDONE low, the device will not enter user mode. | ✓ |
| CRESET_N | Input | Initiates FPGA re-configuration (active low). Pulse CRESET_N low for a duration of $t_{creset_N}$ before asserting CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset. | ✓ |
| TCK | Input | JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin. | ✓ |
| TMS | Input | JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1. | Recommended |
| TDI | Input | JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1. | Recommended |
| TDO | Output | JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance). | ✓ |

**Note:** All dedicated configuration pins have Schmitt Trigger buffer. Refer to the respective Trion FPGAs datasheet for the Schmitt Trigger buffer specifications in **Single Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer** table.

### Table 4: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

| Pins | Direction | Description | Use External Weak Pull-Up |
|---|---|---|---|
| CBUS[2:0] | Input | Configuration bus width select. CBUS has an internal weak pull-up. However, 易灵思 recommends that you use an external pull-up accordingly. See Selecting the Configuration Mode in AN 006: Configuring Trion FPGAs | ✓[2] |
| CBSEL[1:0] | Input | Optional multi-image selection input (if external multi-image configuration mode is enabled). | ✓[3] |
| CCK | I/O | Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up. | Optional[4] |
| CDIn | I/O | n is a number from 0 to 31 depending on the SPI configuration.<br>0: Passive serial data input or active serial output.<br>1: Passive serial data output or active serial input.<br>n: Parallel I/O.<br>In multi-bit daisy chain connection, the CDIn (31:0) connects to the data bus in parallel. | Optional[4] |
| CSI | Input | Chip select.<br>0: The FPGA is not selected or enabled and will not be configured.<br>1: Selects the FPGA for configuration (SPI and JTAG configuration). | ✓ |
| CSO | Output | Chip select output. Selects the next device for cascading configuration. | N/A |
| NSTATUS | Output | Status (active low).<br>Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.<br>For Trion® T4, T8 BGA49, and T8 BGA81 FPGAs, logic low indicates a configuration error due to ID mismatch. | N/A |
| SS_N | Input | SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode.<br>The FPGA senses the value of SS_N when it comes out of reset (pulse CRESET_N low to high).<br>0: Passive mode<br>1: Active mode | Optional[4] |
| TEST_N | Input | Active-low test mode enable signal. Set to 1 to disable test mode.<br>During configuration, rely on the external weak pull-up or drive this pin high. | ✓ |
| RESERVED_OUT | Output | Reserved pin during user configuration. This pin drives high during user configuration.<br>BGA49 and BGA81 packages only. | N/A |

(2) Optional for x1 mode.
(3) Not applicable to single-image or remote update.
(4) Optional unless pull-up is required by external load.

### Table 5: MIPI Pinouts (Dedicated)

n Indicates the number. L indicates the lane

| Function | Group | Direction | Description |
|---|---|---|---|
| VCC25A_MIPI0<br>VCC25A_MIPI1 | Power | – | MIPI 2.5 V analog power supply. |
| VCC12A_MIPI0_TX<br>VCC12A_MIPI1_TX | Power | – | MIPI 1.2 V TX analog power supply. |
| VCC12A_MIPI0_RX<br>VCC12A_MIPI1_RX | Power | – | MIPI 1.2 V RX analog power supply. |
| GNDA_MIPI | Ground | – | Ground for MIPI analog power supply. |
| MIPIn_TXDPL<br>MIPIn_TXDNL | MIPI | I/O | MIPI differential transmit data lane. |
| MIPIn_RXDPL<br>MIPIn_RXDNL | MIPI | I/O | MIPI differential receive data lane. |
| MREFCLK | Clock | Input | MIPI PLL reference clock source. |

### Table 6: DDR Pinouts (Dedicated)

n indicates the number.

| Function | Direction | Description |
|---|---|---|
| VCCIO_DDR | – | DDR power supply. |
| DDR_A[n] | Output | Address signals to the memories. |
| DDR_BA[n] | Output | Bank signals to the memories. |
| DDR_CAS_N | Output | Active-low column address strobe signal to the memories. |
| DDR_CKE | Output | Active-high clock enable signals to the memories. |
| DDR_CK<br>DDR_CK_N | Output | Differential clock output pins to the memories. |
| DDR_CS_N | Output | Active-low chip select signals to the memories. |
| DDR_DQ[n] | I/O | Data bus to/from the memories. |
| DDR_DM[n] | Output | Active-high data-mask signals to the memories. |
| DDR_DQS_N[n] | I/O | Differential data strobes to/from the memories. |
| DDR_DQS[n] | I/O | Differential data strobes to/from the memories. |
| DDR_ODT | Output | ODT signal to the memories. |
| DDR_RAS_N | Output | Active-low row address strobe signal to the memories. |
| DDR_RST_N | Output | Active-low reset signals to the memories. |
| DDR_WE_N | Output | Active-low write enable strobe signal to the memories. |
| DDR_VREF | I/O | Reference voltage. |
| DDR_ZQ | I/O | ZQ calibration pin. |

### Table 7: SPI Flash Memory Pin

| Function | Direction | Description |
|---|---|---|
| SPI_CS_N | Input | Internal SPI flash memory chip select. Available in QFP100F3 packages only. |

# 49-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

**Figure 1: 49-Ball FBGA Pinout Diagram**

## Figure 2: 49-Ball FBGA I/O Bank Diagram

## Figure 3: 49-Ball FPGA Package Marking

## Figure 4: 49-Ball FBGA Package Outline

1. All dimensions and tolerances confirm to ASME Y14.5-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AWW SPEC # 001-2234: Packing Operation Procedure
   B. AWW SPEC # 001-2062: Marking

# 80-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

### Figure 5: 80-Ball WLCSP Pinout Diagram

## Figure 6: 80-Ball WLCSP I/O Bank Diagram

## Figure 7: 80-Ball WLCSP Package Marking

## Figure 8: 80-Ball WLCSP Package Outline

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.4 | 0.455 | 0.51 |
| STAND OFF | | A1 | 0.125 | --- | 0.185 |
| WAFER THICKNESS | | A2 | 0.275 | 0.3 | 0.325 |
| FILM THICKNESS | | A3 | --- | --- | --- |
| BODY SIZE | Y | D | 4.4567 | | |
| | X | E | 3.5569 | | |
| BALL/BUMP PITCH | Y | SD | 0.2 | | BSC |
| | X | SE | 0.2 | | BSC |
| EDGE BALL CENTER TO CENTER | Y | D1 | 3.6 | | BSC |
| | X | E1 | 2.8 | | BSC |
| PITCH | | e | 0.4 | | BSC |
| BALL DIAMETER (SIZE) | | | 0.2 | | |
| BALL/BUMP WIDTH | | b | 0.19 | --- | 0.25 |
| BALL/BUMP COUNT | | n | 80 | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.03 | | |
| WAFER FLATNESS | | bbb | 0.06 | | |
| COPLANARITY | | ccc | 0.03 | | |
| BALL/BUMP OFFSET (PACKAGE) | | ddd | 0.015 | | |

# 81-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

**Figure 9: 81-Ball FBGA Pinout Diagram**

## Figure 10: 81-Ball FBGA I/O Bank Diagram

## Figure 11: 81-Ball FPGA Package Marking

## Figure 12: 81-Ball FBGA Package Outline

1. All dimensions and tolerances confirm to ASME Y14.5-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are define by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AWW SPEC # 001-2234: Packing Operation Procedure
   B. AWW SPEC # 001-2062: Marking

# 100-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

### Figure 13: 100-Lead LQFP Pinout Diagram

## Figure 14: 100-Lead LQFP I/O Bank Diagram

## Figure 15: 100-Lead LQFP FPGA Package Marking

## Figure 16: 100-Lead LQFP FPGA Package Outline

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.17 | 0.2 | 0.27 |
| LEAD WIDTH | | b1 | 0.17 | --- | 0.23 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| | X | D | 16 BSC | | |
| | Y | E | 16 BSC | | |
| BODY SIZE | X | D1 | 14 BSC | | |
| | Y | E1 | 14 BSC | | |
| LEAD PITCH | | e | 0.5 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.08 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

# 144-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

### Figure 17: 144-Lead LQFP Pinout Diagram

## Figure 18: 144-Lead LQFP I/O Bank Diagram

## Figure 19: 144-Lead LQFP FPGA Package Marking

## Figure 20: 144-Lead LQFP FPGA Package Outline

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.17 | 0.22 | 0.27 |
| LEAD WIDTH | | b1 | 0.17 | 0.2 | 0.23 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| BODY SIZE | X | D | 22 BSC | | |
| | Y | E | 22 BSC | | |
| | X | D1 | 20 BSC | | |
| | Y | E1 | 20 BSC | | |
| LEAD PITCH | | e | 0.5 BSC | | |
| FOOTPRINT | | L | 0.45 | 0.6 | 0.75 |
| | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.08 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

# 169-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

## Figure 21: 169-Ball FBGA Pinout Diagram

Note (1) In this package, this pin is not used for configuration functions.

## Figure 22: 169-Ball FBGA I/O Bank Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | MIPI0_ TXDP0 | MIPI0_ TXDP2 | MIPI0_ TXDP4 | MIPI0_ RXDN0 | MIPI0_ RXDN2 | MIPI0_ RXDN4 | MIPI1_ TXDN0 | MIPI1_ TXDP2 | MIPI1_ TXDP4 | MIPI1_ RXDN0 | MIPI1_ RXDN2 | GND | A |
| B | GPIOL_75 _PLLIN1 | MIPI0_ TXDN0 | MIPI0_ TXDN2 | MIPI_0 TXDN4 | MIPI0_ RXDP0 | MIPI0_ RXDP2 | MIPI0_ RXDP4 | MIPI1_ TXDP0 | MIPI1_ TXDN2 | MIPI1_ TXDN4 | MIPI1_ RXDP0 | MIPI1_ RXDP2 | MIPI1_ RXDN4 | B |
| C | GPIOL_73 _EXTFB1 _CDI15 | GPIOL_71 NSTATUS | VCC12A_ MIPI0__TX | MIPI0_ TXDP1 | MIPI0_ TXDP3 | MIPI0_ RXDP1 | MIPI0_ RXDP3 | MIPI1_ TXDP1 | MIPI1_ TXDP3 | MIPI1_ RXDP1 | GNDA_MIPI | MIPI1_ RXDP3 | MIPI1_ RXDP4 | C |
| D | GPIOL_69 _CBSEL1 | GPIOL_70 _CBSEL0 | GNDA_MIPI | MIPI0_ TXDN1 | MIPI0_ TXDN3 | MIPI0_ RXDN1 | MIPI0_ RXDN3 | MIPI1_ TXDN1 | MIPI1_ TXDN3 | MIPI1_ RXDN1 | GNDA_MIPI | MIPI1_ RXDN3 | GPIOR_76 _PLLIN0 | D |
| E | GPIOL_20 _CTRL0 _CDI4 | GND | GPIOL_74 _PLLIN0 | VCC | GNDA_MIPI | VCC12A_ MIPI0__RX | VCC25A_ MIPI0_ | VCC12A_ MIPI1__TX | VCC25A_ MIPI1_ | VCC12A_ MIPI1__RX | GPIOR_85 | GND | GPIOR_78 _EXTFB0 _CDI31 | E |
| F | GPIOL_12 _CDI2 | GPIOL_21 _CTRL1 _CDI5 | GPIOL_72 _EXTFB0 _CDI14 | VCCIO1E | GND | GND | VCC | GND | VCC | VCCIO3A_3B | GPIOR_81 _MREFCLK | GPIOR_77 _PLLIN1 | GPIOR_119 _CTRL12 | F |
| G | TDO | GPIOL_13 _CDI3 | GPIOL_25 _CLK1 | VCCA_TL | VCC | GND | GND | VCC | VCC | VCCA_TR | GPIOR_88 _CDI28 | GPIOR_120 _CLK15 | GPIOR_150 _CBUS1 | G |
| H | TCK | TMS | GPIOL_24 _CLK0 | VCCIO1B_ 1C_1D | VCCIO4B | VCC | VCCIO4A | VCCIO4A | VCCIO4A | VCCIO3C_ 3D_3E | GPIOR_121 _CLK14 | GPIOR_158 _TESTN | GPIOR_155 | H |
| J | GPIOL_08 _CDI0 | GPIOL_09 _CDI1 | TDI | VCCIO1A | VCCIO4B | VCC | GND | GND | VCCIO4A | VCCA_BR | GPIOR_151 _CBUS0 | GPIOR_157 _PLLIN | GPIOB_ RXP12_ EXTFB0 | J |
| K | GPIOL_01 _CCK | GND | CRESET_N | GPIOB_ TXP03 | GPIOB_ TXP06 | GPIOB_ TXP09 | GPIOB_ RXN00 | GPIOB_ RXN02 | GPIOB_ RXP04 | GPIOB_ RXP06 | GPIOB_ RXP08 | GND | GPIOB_ RXN12_ EXTFB0 | K |
| L | GPIOL_00 _SS | CONDONE | GPIOB_ TXN02 | GPIOB_ TXN03 | GPIOB_ TXN06 | GPIOB_ TXN09 | GPIOB_ RXP00 | GPIOB_ RXP02 | GPIOB_ RXN04 | GPIOB_ RXN06 | GPIOB_ RXN08 | GND | GPIOB_ CLKN0 | L |
| M | GPIOB_ TXN01 | GPIOB_ TXP01 | GPIOB_ TXP02 | GND | GPIOB_ TXN05 | GPIOB_ TXN08 | GPIOB_ RXN01 | GPIOB_ RXP03 | GPIOB_ RXP05 | GPIOB_ RXN07 | GPIOB_ RXP09 | GPIOB_ RXN09 | GPIOB_ CLKP0 | M |
| N | GND | GPIOB_ TXN00 | GPIOB_ TXP00 | REF_RES | GPIOB_ TXP05 | GPIOB_ TXP08 | GPIOB_ RXP01 | GPIOB_ RXN03 | GPIOB_ RXN05 | GPIOB_ RXP07 | GPIOB_ RXP10 | GPIOB_ RXN10 | GND | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

Bank 1A
Bank 1A VCCIO
Bank 2A
Bank 3A
Bank 3A_3B VCCIO
Bank 4A
Bank 4A VCCIO
Bank 1B
Bank 1B_1C_1D VCCIO
Bank 2B
Bank 3C
Bank 3C_3D_3E VCCIO
Bank 4B
Bank 4B VCCIO
Bank 1E
Bank 1E VCCIO
Other Dedicated Power and Ground

## Figure 23: 169-Ball FPGA Package Marking

## Figure 24: 169-Ball FBGA Package Outline

1. All dimensions and tolerances confirm to ASME Y14.5M-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AAWW SPEC # 001-2234: Packing Operation Procedure
   B. AAWW SPEC # 001-v2062: Marking

# 256-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

## Figure 25: 256-Ball FBGA Pinout Diagram

## Figure 26: 256-Ball FBGA I/O Bank Diagram

## Figure 27: 256-Ball FPGA Package Marking

## Figure 28: 256-Ball FBGA Package Outline

1. All dimensions and tolerances confirm to ASME Y14.5M-1994
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AAWW SPEC # 001-0531-2234: Packing Operation Procedure
   B. AAWW SPEC # 0010519--2062: Marking

# 324-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package.

**Note:** Some pin names and I/O banks differ between T20/T35 and T55/T85/T120 FPGAs; however, you can still migrate between FPGAs in this package.

# T20 and T35 FPGAs

## Pinout and I/O Banks

### Figure 29: 324-Ball FBGA Pinout Diagram (T20 and T35)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | MIPI1 TXDN1 | MIPI1 TXDN0 | MIPI0 TXDP4 | MIPI0 TXDP3 | MIPI0 TXDN0 | MIPI0 TXDP1 | MIPI0 TXDN2 | GPIOT RXN25 CLKN2 | GPIOT RXP24 EXTFB2 | GPIOT RXP23 | GPIOT RXP22 | GPIOT RXN21 | GPIOT RXN20 | GPIOT RXN19 | GPIOT RXN18 | GPIOT_RXP17 CLKP1 | GND | A |
| B | MIPI1 TXDN2 | MIPI1 TXDP1 | MIPI1 TXDP0 | MIPI0 TXDN4 | MIPI TXDN3 | MIPI0 TXDP0 | MIPI0 TXDN1 | MIPI0 TXDP2 | GPIOT RXP25 CLKP2 | GPIOT RXN24 EXTFB2 | GPIOT RXN23 | GPIOT RXN22 | GPIOT RXP21 | GPIOT RXP20 | GPIOT RXP19 | GPIOT RXP18 | GPIOT RXN17 CLKN1 | GPIOT RXP16 EXTFB1 | B |
| C | MIPI1 TXDP2 | VCC12A MIPI1_TX | GNDA_MIPI | VCC25A MIPI1 | VCC12A MIPI0_RX | VCC12A MIPI0_TX | GNDA_MIPI | GNDA_MIPI | GPIOR_118 PLLIN0 | VCCIO2C | GPIOT RXN02 | GND | GPIOT RXN00 | VCCIO2C | GND | GPIOT RXP01 | VCCIO2B | GPIOT RXN16 EXTFB1 | C |
| D | MIPI1 TXDN4 | MIPI1 TXDP3 | MIPI1 RXDP4 | MIPI1 RXDP0 | MIPI0 RXDN0 | MIPI0 RXDN3 | VCC25A MIPI0 | MIPI0 RXDN1 | GPIOR_119 PLLIN1 | GND | GPIOT RXP02 | GPIOT RXN05 | GPIOT RXP00 | GPIOT RXP04 | GPIOT RXP03 | GPIOT RXN01 | GPIOT RXP13 | GPIOT RXP14 | D |
| E | MIPI1 TXDP4 | MIPI1 TXDN3 | MIPI1 RXDN4 | MIPI1 RXDN0 | MIPI0 RXDP0 | MIPI0 RXDP3 | MIPI0 RXDP4 | MIPI0 RXDP1 | GPIOR_120 PLLIN2 | VCCIO2A | GPIOT RXP07 EXTFB0 | GPIOT RXP05 | GPIOT RXP06 | GPIOT RXN04 | GPIOT RXN03 | GPIOT RXP08 CLKP0 | GPIOT RXN13 | GPIOT RXN14 | E |
| F | MIPI1 RXDN2 | GNDA_MIPI | MIPI1 RXDP1 | GND | MIPI0 RXDN2 | MIPI0 RXDP2 | MIPI0 RXDN4 | VCCA_TR | VCCA_TR | GPIOR_121 MREFCLK | GPIOT RXN07 EXTFB0 | VCCA_BL | GPIOT RXN06 | GPIOT RXN12 | VCCIO2A | GPIOT RXN08 CLKN0 | GND | VCCIO2B | F |
| G | MIPI1 RXDP2 | MIPI1 RXDN3 | MIPI1 RXDN1 | DDR_DQ[15] | GPIOR_125 CTRL12 | GPIOR_126 CLK15 | GND | VCC | GND | VCC | GND | VCC | GPIOL_75 CTRL5 | GPIOT RXP12 | GPIOT RXP11 | GPIOT RXP10 | GPIOT RXP09 | GPIOT RXN15 | G |
| H | GND | MIPI1 RXDP3 | VCC12A MIPI1_RX | DDR_DQ[13] | DDR_DM[1] | GPIOR_130 CLK11 | VCC | GND | VCC | GND | VCC | GND | GPIOL_73 CLK7 | GPIOL_72 CLK6 | GPIOT RXN11 | GPIOT RXN10 | GPIOT RXN09 | GPIOT RXP15 | H |
| J | DDR_DQ[8] | VCCIO _DDR | DDR_DQ[10] | DDR _DQ[12] | DDR_DQ[14] | VCCIO 3C_TR_BR | GND | VCC | GND | VCC | GND | VCC | VCCIO 1D_1E | GPIOL_102 NSTATUS | GPIOL_103 TEST_N | GND | GPIOL_108 CBSEL0 | GPIOL_109 CBSEL1 | J |
| K | DDR_DQ[6] | DDR_DQ[9] | DDR_DQ[11] | VCCIO _DDR | DDR_DQS[1] | GPIOR_135 CTRL10 | VCC | GND | VCC | GND | VCC | GND | VCCIO1B_1C | GPIOL_14 CDI2 | GPIOL_63 CTRL1 | GPIOL_62 CTRL0 | GPIOL_66 CLK0 | GPIOL_16 CDI3 | K |
| L | DDR_DM[0] | VCCIO _DDR | DDR_DQ[5] | DDR_ DQ[7] | DDR_ DQS_N[1] | VCCIO _DDR | GND | VCC | GND | VCC | GND | VCC | VCCIO1A | GPIOL_15 PLLIN0 | GPIOL_17 EXTFB0 | GPIOL_22 CDI6 | GPIOL_24 CDI7 | GPIOL_20 CDI5 | L |
| M | GND | DDR_DQ[3] | DDR_DQS[0] | DDR_DQ[4] | GND | DDR_VREF | VCC | GND | VCC | GND | VCC | GND | GPIOL_08 CDI0 | GPIOL_11 CBUS0 | GPIOL_05 CSO | GPIOL_12 CBUS1 | GPIOL_13 CBUS2 | GPIOL_18 CDI4 | M |
| N | DDR_DQ[2] | DDR_ DQ[1] | DDR_ DQS_N[0] | DDR_DQ[0] | DDR_ZQ | DDR_CS_N | DDR_CKE | VCCA_BR | GPIOB TXP16 CDI13 | GPIOB_TXP14 EXTFB1 CDI17 | GPIOB TXP13 CDI19 | GPIOB TXN12 | GPIOL_01 CCK | GPIOL_09 CDI1 | GPIOL_04 CSI | GND | CRESET_N | CDONE | N |
| P | DDR_CK | VCCIO _DDR | DDR_A[0] | DDR_A[1] | VCCIO _DDR | DDR_A[3] | GND | VCCA_BR | GPIOB TXN16 CDI12 | GPIOB TXN14 CDI16 | GPIOB TXN13 CDI18 | GPIOB TXP12 | GPIOB TXP09 CLK0 | GPIOB TXP07 CDI23 | GPIOL_00 SS_N | TMS | TDO | GPIOB TXN02 | P |
| R | DDR_CK_N | GND | DDR_A[5] | GND | DDR_BA[2] | DDR_A[2] | DDR_A[6] | GPIOR_140 PLLIN2 | GPIOB TXN19 | GND | VCCIO4A | GPIOB TXP11 | GPIOB TXN09 | GPIOB TXN07 CDI22 | GPIOB TXN05 CDI26 | TDI | GPIOB TXN00 | GPIOB TXP02 | R |
| T | DDR_A[4] | DDR_RST_N | DDR_A[9] | DDR_A[8] | DDR_BA[0] | DDR_A[13] | VCCIO _DDR | GPIOR_139 PLLIN1 | GPIOB TXP19 CLK2 | VCCIO4A | GPIOB TXN18 CDI8 | GPIOB TXN11 | GND | VCCIO4B | GPIOB TXP05 CDI27 | TCK | GPIOB TXP00 | GPIOB TXN01 | T |
| U | DDR_ODT | VCCIO _DDR | DDR_BA[1] | DDR_WE_N | VCCIO _DDR | DDR_A[12] | DDR_A[11] | GPIOR_138 PLLIN0 | GPIOB TXN17 CDI10 | GPIOB_TXP15 CLK1 CDI15 | GPIOB TXP18 EXTFB2_CDI9 | GPIOB TXN10 | GPIOB TXN08 CDI20 | GPIOB TXN06 CDI24 | GPIOB TXP04 CDI29 | GPIOB TXP03 CDI31 | VCCIO4B | GPIOB TXP01 | U |
| V | GND | DDR_ CAS_N | DDR_RAS_N | GND | DDR_A[15] | DDR_A[14] | DDR_A[10] | DDR_A[7] | GPIOB TXP17 CDI11 | GPIOB TXN15 CDI14 | REF_RES_4A | GPIOB TXP10 | GPIOB_TXP08 EXTFB0 CDI21 | GPIOB TXP06 CDI25 | GPIOB TXN04 CDI28 | GPIOB TXN03 CDI30 | REF_RES_4B | GND | V |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

Configuration or GPIO
Dedicated Configuration
Dedicated JTAG
Multi-Function or GPIO
Multi-Function, Configuration, or GPIO
MIPI
Dedicated Power
Dedicated Ground
GPIO
LVDS or GPIO
Multi-Function, LVDS, or GPIO
LVDS Reference Resistor Pin
Configuration, LVDS, or GPIO
DDR

## Figure 30: 324-Ball FBGA I/O Bank Diagram (T20 and T35)

# Package Outline and Marking

## Figure 31: 324-Ball FBGA Package Outline (T20 and T35)

**Figure 32: 324-Ball FPGA Package Marking (T20 and T35)**

# T55, T85, and T120 FPGAs

## Pinout and I/O Banks

### Figure 33: 324-Ball FBGA Pinout Diagram (T55, T85, and T120)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | MIPI1 TXDN1 | MIPI1 TXDN0 | MIPI0 TXDP4 | MIPI0 TXDP3 | MIPI0 TXDN0 | MIPI0 TXDP1 | MIPI0 TXDN2 | GPIOT RXN29 CLKN2 | GPIOT RXP28 EXTFB2 | GPIOT RXP27 | GPIOT RXP24 | GPIOT RXN23 | GPIOT RXN22 | GPIOT RXN21 | GPIOT RXN20 | GPIOT RXP19 CLKP1 | GND | A |
| B | MIPI1 TXDN2 | MIPI1 TXDP1 | MIPI1 TXDP0 | MIPI0 TXDN4 | MIPI TXDN3 | MIPI0 TXDP0 | MIPI0 TXDN1 | MIPI0 TXDP2 | GPIOT RXP29 CLKP2 | GPIOT RXN28 EXTFB2 | GPIOT RXN27 | GPIOT RXN24 | GPIOT RXP23 | GPIOT RXP22 | GPIOT RXP21 | GPIOT RXP20 | GPIOT RXN19 CLKN1 | GPIOT RXP18 EXTFB1 | B |
| C | MIPI1 TXDP2 | VCC12A MIPI1_TX | GNDA_MIPI | VCC25A MIPI1 | VCC12A MIPI0_RX | VCC12A MIPI0_TX | GNDA_MIPI | GNDA_MIPI | GPIOR_166 PLLIN0 | VCCIO2F | GPIOT RXN03 | GND | GPIOT RXN01 | VCCIO2F | GND | GPIOT RXP02 | VCCIO2E | GPIOT RXN18 EXTFB1 | C |
| D | MIPI1 TXDN4 | MIPI1 TXDP3 | MIPI1 RXDP4 | MIPI1 RXDP0 | MIPI0 RXDN0 | MIPI0 RXDN3 | VCC25A MIPI0 | MIPI0 RXDN1 | GPIOR_167 PLLIN1 | GND | GPIOT RXP03 | GPIOT RXN06 | GPIOT RXP01 | GPIOT RXP05 | GPIOT RXP04 | GPIOT RXN02 | GPIOT RXP15 | GPIOT RXP16 | D |
| E | MIPI1 TXDP4 | MIPI1 TXDN3 | MIPI1 RXDN4 | MIPI1 RXDN0 | MIPI0 RXDP0 | MIPI0 RXDP3 | MIPI0 RXDP4 | MIPI0 RXDP1 | GPIOR_168 PLLIN2 | VCCIO2D | GPIOT RXP08 EXTFB0 | GPIOT RXP06 | GPIOT RXP07 | GPIOT RXN05 | GPIOT RXN04 | GPIOT RXP09 CLKP0 | GPIOT RXN15 | GPIOT RXN16 | E |
| F | MIPI1 RXDN2 | GNDA_MIPI | MIPI1 RXDP1 | GND | MIPI0 RXDN2 | MIPI0 RXDP2 | MIPI0 RXDN4 | VCCA_TR | VCCA_TR | GPIOR_169 MREFCLK | GPIO RXN08 EXTFB0 | VCCA_BL | GPIOT RXN07 | GPIOT RXN14 | VCCIO2D | GPIOT RXN09 CLKN0 | GND | VCCIO2E | F |
| G | MIPI1 RXDP2 | MIPI1 RXDN3 | MIPI1 RXDN1 | DDR_DQ[15] | GPIOR_173 CTRL12 | GPIOR_174 CLK15 | GND | VCC | GND | VCC | GND | VCC | GPIOL_75 CTRL5 | GPIOT RXP14 | GPIOT RXP13 | GPIOT RXP12 | GPIOT RXP11 | GPIOT RXN17 | G |
| H | GND | MIPI1 RXDP3 | VCC12A MIPI1_RX | DDR_DQ[13] | DDR_DM[1] | GPIOR_178 CLK11 | VCC | GND | VCC | GND | VCC | GND | GPIOL_73 CLK7 | GPIOL_72 CLK6 | GPIOT RXN13 | GPIOT RXN12 | GPIOT RXN11 | GPIOT RXP17 | H |
| J | DDR_DQ[8] | VCCIO _DDR | DDR_DQ[10] | DDR_ DQ[12] | DDR_DQ[14] | VCCIO 3D_TR_BR | GND | VCC | GND | VCC | GND | VCC | VCCIO1D_ 1E_1F_1G | GPIOL_150 NSTATUS | GPIOL_151 TEST_N | GND | GPIOL_156 CBSEL0 | GPIOL_157 CBSEL1 | J |
| K | DDR_DQ[6] | DDR_DQ[9] | DDR_DQ[11] | VCCIO _DDR | DDR_ DQS[1] | GPIOR_183 CTRL10 | VCC | GND | VCC | GND | VCC | GND | VCCIO1B_1C | GPIOL_14 CDI2 | GPIOL_63 CTRL1 | GPIOL_62 CTRL0 | GPIOL_66 CLK0 | GPIOL_16 CDI3 | K |
| L | DDR_DM[0] | VCCIO _DDR | DDR_DQ[5] | DDR_ DQ[7] | DDR_ DQS_N[1] | VCCIO _DDR | GND | VCC | GND | VCC | GND | VCC | VCCIO1A | GPIOL_15 PLLIN0 | GPIOL_17 EXTFB0 | GPIOL_22 CDI6 | GPIOL_24 CDI7 | GPIOL_20 CDI5 | L |
| M | GND | DDR_DQ[3] | DDR_DQS[0] | DDR_DQ[4] | GND | DDR_VREF | VCC | GND | VCC | GND | VCC | GND | GPIOL_08 CDI0 | GPIOL_11 CBUS0 | GPIOL_05 CSO | GPIOL_12 CBUS1 | GPIOL_13 CBUS2 | GPIOL_18 CDI4 | M |
| N | DDR_DQ[2] | DDR_DQ[1] | DDR_DQS _N[0] | DDR_DQ[0] | DDR_ZQ | DDR_CS_N | DDR_CKE | VCCA_BR | GPIOB TXP16 CDI13 | GPIOB TXP14 CDI17 | GPIOB TXP13 CDI19 | GPIOB TXN12 | GPIOL_01 CCK | GPIOL_09 CDI1 | GPIOL_04 CSI | GND | CRESET_N | CDONE | N |
| P | DDR_CK | VCCIO _DDR | DDR_A[0] | DDR_A[1] | VCCIO _DDR | DDR_A[3] | GND | VCCA_BR | GPIOB TXN16 CDI12 | GPIOB TXN14 CDI16 | GPIOB TXN13 CDI18 | GPIOB TXP12 | GPIOB TXP09 | GPIOB TXP07 CDI23 | GPIOL_00 SS_N | TMS | TDO | GPIOB TXN02 | P |
| R | DDR_CK_N | GND | DDR_A[5] | GND | DDR_BA[2] | DDR_A[2] | DDR_A[6] | GPIOR_188 PLLIN2 | GPIOB TXN19 | GND | VCCIO4E | GPIOB TXP11 | GPIOB TXN09 | GPIOB TXN07 CDI22 | GPIOB TXN05 CDI26 | TDI | GPIOB TXN00 | GPIOB TXP02 | R |
| T | DDR_A[4] | DDR_RST_N | DDR_A[9] | DDR_A[8] | DDR_BA[0] | DDR_A[13] | VCCIO _DDR | GPIOR_187 PLLIN1 | GPIOB TXP19 | VCCIO4E | GPIOB TXN18 CDI8 | GPIOB TXN11 | GND | VCCIO4F | GPIOB TXP05 CDI27 | TCK | GPIOB TXP00 | GPIOB TXN01 | T |
| U | DDR_ODT | VCCIO _DDR | DDR_BA[1] | DDR_WE_N | VCCIO _DDR | DDR_A[12] | DDR_A[11] | GPIOR_186 PLLIN0 | GPIOB TXN17 CDI10 | GPIOB TXP15 CDI15 | GPIOB TXP18 CDI9 | GPIOB TXN10 | GPIOB TXN08 CDI20 | GPIOB TXN06 CDI24 | GPIOB TXP04 CDI29 | GPIOB TXP03 CDI31 | VCCIO4F | GPIOB TXP01 | U |
| V | GND | DDR_ CAS_N | DDR_ RAS_N | GND | DDR_A[15] | DDR_A[14] | DDR_A[10] | DDR_A[7] | GPIOB TXP17 CDI11 | GPIOB TXN15 CDI14 | REF_RES_4E | GPIOB TXP10 | GPIOB TXP08 CDI21 | GPIOB TXP06 CDI25 | GPIOB TXN04 CDI28 | GPIOB TXN03 CDI30 | REF_RES_4F | GND | V |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

Configuration or GPIO
Multi-Function or GPIO
Dedicated Power
LVDS or GPIO
Configuration, LVDS, or GPIO
Dedicated Configuration
Multi-Function, Configuration, or GPIO
Dedicated Ground
Multi-Function, LVDS, or GPIO
DDR
Dedicated JTAG
MIPI
GPIO
LVDS Reference Resistor Pin

## Figure 34: 324-Ball FBGA I/O Bank Diagram (T55, T85, and T120)

# Package Outline and Marking

## Figure 35: 324-Ball FBGA Package Outline (T55, T85, and T120)

**Figure 36: 324-Ball FPGA Package Marking (T55, T85, and T120)**

# 400-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

## Figure 37: 400-Ball FBGA Pinout Diagram

## Figure 38: 400-Ball FBGA I/O Bank Diagram

## Figure 39: 400-Ball FBGA Package Outline

## Figure 40: 400-Ball FPGA Package Marking

# 484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

## Figure 41: 484-Ball FBGA Pinout Diagram

## Figure 42: 484-Ball FBGA I/O Bank Diagram

## Figure 43: 484-Ball FBGA Package Outline

## Figure 44: 484-Ball FPGA Package Marking

# 576-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

## Figure 45: 576-Ball FBGA Pinout Diagram

## Figure 46: 576-Ball FBGA I/O Bank Diagram

## Figure 47: 576-Ball FBGA Package Outline

## Figure 48: 576-Ball FPGA Package Marking

# Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for 易灵思® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its profile, which depends upon the board design and the reflow equipment used. You must characterize each PCB to find a reliable profile.

## Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

## Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

## BGA Reballing

易灵思 does not recommend BGA reballing. Reballed BGA packages void the original 易灵思® specifications.

## Peak Reflow Temperatures

**Table 8: Peak Reflow Temperature ($T_p$) by Package**

| Package | Number of Leads/Balls | Moisture Sensitivity Level | Peak Reflow Temperature (+0/-5 °C) |
|---|---|---|---|
| FBGA | 49 | 3 | 260 |
| WLCSP | 80 | 1 | 260 |
| FBGA | 81 | 3 | 260 |
| LQFP | 100 | 3 | 260 |
| FBGA | 169 | 3 | 260 |
| FBGA | 256 | 3 | 260 |
| FBGA | 324 | 3 | 260 |
| FBGA | 400 | 3 | 260 |
| FBGA | 484 | 3 | 260 |
| FBGA | 576 | 3 | 260 |
| LQFP | 144 | 3 | 260 |

**Note:** These packages are "green" and RoHS compliant.

# Reflow Profile for SMT Packages

The reflow process usually includes four phases:

1. **Preheat Phase**—The preheat phase brings the assembly from 25 °C to $T_S$. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
   - **Solder Ball Spattering**—Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
   - **Bridging**—Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase**—As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase**—The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase**—Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

**Table 9: Peak Reflow Temperature ($T_P$) Parameters**

| Parameter | Description | Specification (Lead and Halogen Free Packages) |
|---|---|---|
| Ramp up | Average ramp-up rate ($T_{SMAX}$ to $T_P$) | 3 °C/second maximum |
| $T_{SMIN}$ | Preheat peak minimum temperature | 150 °C |
| $T_{SMAX}$ | Preheat peak maximum temperature | 200 °C |
| $t_s$ | Time between $T_{SMIN}$ and $T_{SMAX}$ | 60 - 120 seconds |
| $T_L$ | Solder melting point | 217 °C |
| $t_L$ | Time maintained above $T_L$ | 60 - 150 seconds |
| $t_P$ | Time within 5 °C of peak temperature | 30 seconds |
| Ramp down | Ramp-down rate | 6 °C/second maximum |
| $t_{25C}$ to $T_p$ | Time from 25 °C to peak temperature | 8 minutes maximum |

**Figure 49: Thermal Reflow Profile**

# Thermal Resistance

Thermal management is an important consideration when designing your system. 易灵思® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, the proximity of other devices, and user applications. Because of this, 易灵思 FPGAs do not come with preset thermal solutions.

**Table 10: Device/Package Thermal Resistance**

| Device | Package | Dimensions (mm) | $\Theta_{JA}$/W Still Air | $\Theta_{JA}$ (200 LFM)/W | $\Theta_{JA}$ (500 LFM)/W | $\Theta_{JB}$/W | $\Theta_{JC}$/W |
|---|---|---|---|---|---|---|---|
| T4, T8 | FBGA49 | 3 x 3 | 90.446 | 84.782 | 81.797 | 56.464 | 46.431 |
| | FBGA81 | 5 x 5 | 80.476 | 75.363 | 72.797 | 55.352 | 32.583 |
| T8, T20 | LQFP144 | 20 x 20 | 42.82 | 37.68 | 35.50 | 31.12 | 10.51 |
| T13, T20 | LQFP100 | 14 x 14 | 51.29 | 45.64 | 43.40 | 37.70 | 15.21 |
| | FBGA169 | 9 x 9 | 38.25 | 33.33 | 31.60 | 23.64 | 12.39 |
| | FBGA256 | 13 x 13 | 24.24 | 20.52 | 17.59 | 31.57 | 11.85 |
| T20 | WLCSP80 | 4.5 x 3.5 | 44.94 | 39.35 | 37.54 | 18.91 | 0.12 |
| T20, T35 | FBGA324 | 12 x 12 | 20.69 | 17.89 | 16.89 | 10.12 | 2.59 |
| | FBGA400 | 16 x 16 | 18.70 | 16.95 | 15.92 | 12.45 | 11.10 |
| T55, T85,T120 | FBGA324 | 12 x 12 | 16.9 | 14.4 | 13.5 | 8.04 | 2.01 |
| | FBGA484 | 18 x 18 | 15.85 | 12.83 | 11.99 | 6.10 | 4.10 |
| | FBGA576 | 16 x 16 | 15.376 | 13.648 | 12.568 | 6.601 | 1.712 |

Where:

- $\Theta_{JA}$ is the junction-to-ambient thermal resistance
- $\Theta_{JB}$ is the junction-to-board thermal resistance
- $\Theta_{JC}$ is the junction-to-case thermal resistance

# PCB Guidelines for BGA Packages

## PCB Solder Pad Guidelines

易灵思 provides solder mask defined (SMD) and non-solder mask defined (NSMD) diameter information. Use this data when creating your board landing pads.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better "grip" area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball.

**Figure 50: SMD and Non-SMD Pad Specification**

**Legend:**

A: BGA package solder mask opening
B: Optimum PCB solder mask opening
C: Optimum PCB pad size
D: Solder ball diameter

### Table 11: PCB Solder Pad Recommendations

| Package | Pitch (mm) | A BGA Package Solder Mask Opening (mm) | SMD | | Non-SMD | | D Solder Ball Diameter (mm) |
|---|---|---|---|---|---|---|---|
| | | | B Optimum PCB Solder Mask Opening (mm) | C Optimum PCB Pad Size (mm) | B Optimum PCB Solder Mask Opening (mm) | C Optimum PCB Pad Size (mm) | |
| F49 | 0.4 | 0.2 | 0.2 | 0.275 | 0.3 | 0.2 | 0.25 |
| W80 | 0.4 | N.A. | 0.175 | 0.225 | 0.25 | 0.175 | 0.2 |
| F81 | 0.5 | 0.245 | 0.245 | 0.325 | 0.4 | 0.2 | 0.25 |
| F169 | 0.65 | 0.25 | 0.25 | 0.35 | 0.4 | 0.2 | 0.25 |
| F256 | 0.8 | 0.37 | 0.37 | 0.5 | 0.5 | 0.35 | 0.4 |
| F324 (T20, T35 | 0.65 | 0.275 | 0.275 | 0.335 | 0.4 | 0.25 | 0.3 |
| F324 (T55, T85, T120 | 0.65 | 0.275 | 0.275 | 0.38 | 0.4 | 0.25 | 0.3 |
| F400 | 0.8 | 0.275 | 0.275 | 0.38 | 0.4 | 0.25 | 0.3 |
| F484 | 0.8 | 0.35 | 0.35 | 0.45 | 0.5 | 0.35 | 0.4 |
| F576 | 0.65 | 0.275 | 0.275 | 0.38 | 0.4 | 0.25 | 0.3 |

# Routing between Pads on the Top Layer

You can route signal trace between solder pads on the top layer of the PCB while meeting the clearance requirement.

**Figure 51: Routing Traces between Pads on the Top Layer**

**Table 12: Routing Measurements**

| Measure-ment | Description | Ball Count | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | F49 | W80 | F81 | F169 | F256 | F324 (T20, T35) | F324 (T55, T85, T120) | F400 | F484 | F576 | |
| A | Ball pitch. | 0.4 | 0.4 | 0.5 | 0.65 | 0.8 | 0.65 | 0.65 | 0.8 | 0.8 | 0.65 | mm |
| | Ball #. | 0.25 | 0.2 | 0.25 | 0.25 | 0.4 | 0.3 | 0.3 | 0.3 | 0.4 | 0.3 | mm |
| B | Width of the solder landing pad # (SMD) | 0.275 | 0.225 | 0.325 | 0.35 | 0.5 | 0.335 | 0.38 | 0.38 | 0.45 | 0.38 | mm |
| | Width of the solder landing pad # (NSMD) | 0.2 | 0.175 | 0.2 | 0.2 | 0.35 | 0.25 | 0.25 | 0.25 | 0.35 | 0.25 | mm |
| H (min.) | Minimum space between the trace and the landing pad (SMD) | (5) | (5) | 0.05 | 0.08 | 0.08 | 0.1 | 0.08 | 0.1 | 0.1 | 0.08 | mm |
| | Minimum space between the trace and the landing pad (NSMD) | (5) | (5) | 0.08 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | mm |

(5) The via is under the pad, no traces between landing pads.

# Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an "offset via," is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

**Figure 52: Via Dimensions**

**Table 13: Via Measurements**

| Measure-ment | Description | Ball Count | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | F49 | W80 | F81 | F169 | F256 | F324 (T20, T35) | F324 (T55, T85, T120) | F400 | F484 | F576 | |
| D | Via capture pad width. | 0.16 | 0.16 | 0.22 | 0.3 | 0.4 | 0.3 | 0.3 | 0.3 | 0.4 | 0.3 | mm |
| E | Finished via #. | 0.1 | 0.1 | 0.13 | 0.15 | 0.25 | 0.15 | 0.2 | 0.2 | 0.25 | 0.2 | mm |
| F (min.) | Space between the landing pad and via. | (6) | (6) | 0.08 | 0.12 | 0.11 | 0.14 | 0.11 | 0.14 | 0.12 | 0.11 | mm |

(6) The via is under the pad, no traces between landing pads.

# Routing through Different PCB Layers

You can route a trace between two solder pads, at the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

**Figure 53: BGA Trace Routing for Top and Second Layers**

**Table 14: Routing Measurements**

| Measure-ment | Description | Ball Count | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | F49 | W80 | F81 | F169 | F256 | F324 (T20, T35) | F324 (T55, T85, T120) | F400 | F484 | F576 | |
| G (min.) | Minimum space required between via trace and spacing. | 0.08 | 0.08 | 0.085 | 0.01 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | mm |

# PCB Guidelines for QFP Packages

## PCB Solder Pad (LQFP Packages)

易灵思 provides LQFP lead dimension information. Use this data when creating your board layout so that the board pads match the landing pads.

**Figure 54: Recommended PCB Landing Pad Guideline**

| Package | L | B | e |
|---|---|---|---|
| LQFP 144-pin | 1.35 mm | 0.29 mm | 0.5 BSC |
| LQFP 100-pin | 1.35 mm | 0.29 mm | 0.5 BSC |

**Figure 55: LQFP Lead Dimensions**

| | Symbol | Min | Nom | Max |
|---|---|---|---|---|
| Total thickness | A | – | – | 1.6 |
| Stand-off | A1 | 0.05 | – | 0.15 |
| Mold thickness | A2 | 1.35 | 1.4 | 1.45 |
| Lead width | b | 0.17 | 0.22 | 0.27 |
| L/F thickness | c | 0.09 | – | 0.2 |
| | L | 0.45 | 0.6 | 0.75 |

# Green Packaging

易灵思 FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. 易灵思 refers to these products as "green" packaging.

# Tape and Reel Packaging

易灵思 offers BGA and WLCSP devices in tape and reel packaging.

### Table 15: Tape and Reel Packaging

| Package | Carrier Width (mm) | Cover Width (mm) | Pitch (mm) | Reel Size (in) | Maximum Quantity per Reel |
|---|---|---|---|---|---|
| FBGA49 | 12 | 9.3 | 8 | 13 | 5,000 |
| | 12 | 9.3 | 8 | 7 | 1,500 |
| FBGA81 | 12 | 9.3 | 8 | 13 | 5,000 |
| | 12 | 9.3 | 8 | 7 | 1,500 |
| WLCSP80 | 12 | 9.5 | 8 | 13 | 2,500 |

### Figure 56: Pin 1 Location (BGA49 and BGA81 Packages)

### Figure 57: Tape Outline (BGA49 Packages)

Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Camber not to exceed 1 mm in 250 mm.
3. Material is black, conductive polystyrene.
4. Measured on a plane 0.3 mm above the bottom of the pocket.
5. Measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be the same position.

## Figure 58: Tape Outline (BGA81 Packages)

Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Camber not to exceed 1 mm in 250 mm.
3. Material is black, conductive polystyrene.
4. Measured on a plane 0.3 mm above the bottom of the pocket.
5. Measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be the same position.

### Figure 59: Pin 1 Location (WLCSP80 Packages)

### Figure 60: Tape Outline (WLCSP80 Packages)

Unit: mm

| Symbol | Ao | Bo | Ko | Po | P1 | P2 | T |
|---|---|---|---|---|---|---|---|
| Spec | 3.76±0.05 | 4.66±0.05 | 0.66±0.05 | 4.00±0.10 | 8.00±0.10 | 2.00±0.05 | 0.25±0.03 |
| Symbol | E | F | Do | D1 | W | 10Po | |
| Spec | 1.75±0.10 | 5.50±0.05 | $1.50^{+0.10}_{-0}$ | 1.00±0.05 | 12.0±0.30 | 40.0±0.20 | |

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity $\geq 1.0*10^{5}$ & $\leq 1.0*10^{8}$ ohm/sq.

# Tray Packaging

易灵思 offers BGA and LQFP devices in tray packaging.

**Table 16: Tray Packaging**

| Package | Quantity per Tray | Tray Matrix | Tray Stack | Minimum Quantity per Stack |
|---|---|---|---|---|
| FBGA256 | 119 | 7 x 17 | 10 + 1 | 1,190 |
| FBGA169 | 260 | 10 x 26 | 10 + 1 | 2,600 |
| LQFP100 | 90 | 6 x 15 | 10 + 1 | 900 |
| LQFP144 | 60 | 12 x 5 | 10 + 1 | 600 |
| FBGA324 | 168 | 21 x 8 | 10 + 1 | 1,680 |
| FBGA400 | 84 | 14 x 6 | 10 + 1 | 840 |
| FBGA484 | 84 | 14 x 6 | 10 + 1 | 840 |
| FBGA576 | 84 | 14 x 6 | 10 + 1 | 840 |

# Revision History

**Table 17: Revision History**

| Date | Version | Description |
|---|---|---|
| August 2023 | 4.8 | Updated package outline for 49-Ball and 576-Ball FBGA Package Specifications. Added in package thickness of 1.07mm for 324-Ball Package Specifications. (ADV-2307-001) (DOC-1350) |
| June 2023 | 4.7 | Updated Trion T13/T20 Q100F3. (DOC-1164) |
| February 2023 | 4.6 | Corrected side view dimensions for F256 package. (DOC-813)<br>Corrected routing and via dimensions for the F169 package. (DOC-804)<br>Added 1,500 quantity tape and reel information for T4 and T8 FPGAs in BGA49 and BGA81 packages.<br>Added PCB data for F400 packages. (DOC-928)<br>Updated routing measurements. (DOC-928) |
| April 2022 | 4.5 | Corrected typo for pin A9 in BGA400 package pinout and I/O banks. (DOC-784) |
| March 2022 | 4.4 | Corrected typos for pins G6 and H15 in BGA400 package pinout and I/O banks. (DOC-756)<br>Noted that BGA324, BGA400, and BGA576 are flip-chip packages. (DOC-756) |
| March 2022 | 4.3 | Removed thermal pad from LQFP144 Recommended PCB Landing Pad Guideline; this package does not have a thermal pad. (DOC-751) |
| February 2022 | 4.2 | Fixed typo in LQFP144 package pinout and I/O banks. Pin 31 was incorrectly marked as 34. |
| February 2022 | 4.1 | Added recommended PCB landing pad guideline for LQFP packages.<br>Corrected color coding for VCCIO4A in the BGA169 I/O bank diagram. (DOC-719)<br>Correct the F (min.) via measurement for the BGA484 and BGA256 packages. (DOC-710) |
| December 2021 | 4.0 | Fix incorrect pin names for T55/T85/T120 FPGAs in the BGA324 package. (DOC-671) |
| November 2021 | 3.9 | Fixed incorrect color coding for I/O banks VCCIO_1F_1G in the BGA484 package. (DOC-639) |
| November 2021 | 3.8 | Corrected symbols for pins L19 and R15 for the 400 BGA package. (DOC-564) |
| August 2021 | 3.7 | Corrected pin numbering for the WLCSP80 package. (DOC-504)<br>Corrected pitch for F576 in the PCB Solder Pad Recommendations table. (DOC-504)<br>Updated PCB solder pad recommendations (DOC-504)<br>Corrected pin A9 for F256 package pinout. (DOC-493) |
| July 2021 | 3.6 | Rotated package outline, pinout, and I/O banks figures for the WLCSP80 to make it easier to identify pin 1. |
| June 2021 | 3.5 | Added thermal resistance data for WLCSP80 package. (DOC-439)<br>Added tape and reel information for WLCSP80. (DOC-439)<br>Added peak reflow temperature for WLCSP80.<br>Corrected typos in BGA256 pinout and fixed mislabeled banks in BGA256 I/O banks. (DOC-452) |
| December 2020 | 3.4 | Added WLCSP80 package information. |
| August 2020 | 3.3 | Updated routing measurements and via measurements. |
| July 2020 | 3.2 | Corrected the BGA169 pinout. |
| July 2020 | 3.1 | Updated solder ball co-planarity limit from 0.1 to 0.15.<br>Updated 81-ball FPGA package marking. |
| May 2020 | 3.0 | Added guidelines for traces, pads, and vias for PCB design.<br>Added BGA400 package information.<br>Updated side view BGA576 package dimensions. |

| Date | Version | Description |
|---|---|---|
| February 2020 | 2.1 | Fixed typos in BGA576 pinout and I/O bank diagrams. |
| January 2020 | 2.0 | Added BGA324, BGA484, and BGA576 package information. |
| October 2019 | 1.6 | Added LQFP144 package information. |
| August 2019 | 1.5 | Updated BGA169 and BGA256 package marking. |
| June 2019 | 1.4 | Added 169 ball FBGA package information. |
| February 2019 | 1.3 | Added Thermal resistance, solder pad dimensions, and peak reflow data for the 256 BGA package.<br>Aded information on tray packaging.<br>Clarified PLL ground pin in the 81 ball BGA diagram and pinout.<br>Updated 256 ball FBGA package marking. |
| November 2018 | 1.2 | Added 256 ball FBGA package information. |
| August 2018 | 1.1 | Updated BGA81 pin figure. |
| July 2018 | 1.0 | Initial release. |