易灵思®

White Paper

Unplug with Low-Power FPGA Solutions

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Introduction

Today, design engineers and architects are expected to juggle conflicting system requirements during product development. Product mobility and non-traditional end product locations in the "real world" continue to affect design decisions as IoT and other data driven needs push data gathering and edge analytics out and away from the safety of an AC wall plug.

These new use cases create challenges for the overall size of the product and put pressure on the intertwined power subsystem and the actual product functions themselves.

Reducing power can be a daunting challenge

Further design complications come from these small, unique products placed in non-traditional locations with little infrastructure, while mobile devices seem to be converging towards a desired size of "zero." As more space is needed for power delivery functions for longer life, it negatively affects the size constraints of the remaining design, further pushing for smaller footprint and more power efficient devices. In addition to the size constraints, the overall power efficiency is important to regulate the heat of these fan-less products for high reliability through a variety of environmental conditions.

In this white paper, we highlight 易灵思's leadership in low power, specifically some very low power FPGAs with extremely small footprints.

Power Consumption in FPGAs

Two components of the actual power in a system are static and dynamic power. Static power is defined as the product of the power supply voltage and static current, which itself has two further components: leakage current and through current. Leakage currents are due to parasitic effects inherent in the transistors. Through currents occur in normal operation

Factors to consider when choosing the right low-power FPGA:

- Is it fabricated on a low-power process?
- Was it designed with a low-power architecture?
- Are the FPGA's hard IP blocks low power?
- What is the supply voltage?

and are due to transistors being continuously operated in their saturation region. The predominant cause of static power consumption in a system is leakage, which is highly dependent on the process used to fabricate the FPGA.

Dynamic power has two components: the capacitive load power and the cell power. The cell power is consumed internally by the cell primitives. This component accounts for the power that is required to charge and discharge the internal cell capacitance. The capacitive load power represents the currents required to charge the external loads driven by each cell.

Dynamic power can vary depending on the supply voltage, switching frequency, and load capacitance. Essentially, dynamic power consumption comes from the outputs changing state. The dynamic power is used to charge the load

capacitance when the output transitions from 0 to 1. This charge is then drained when the output transitions back to 0. Therefore, the number and frequency of transitions in an end application strongly affects power consumption.

Ultimately, dynamic power is tied to frequency, as CMOS power is primarily driven as logic level switching occurs.

Ultra-Low-Power Trion FPGAs

易灵思® Trion® T4 and the T8 in 81-ball BGA and 49-ball BGA packages are the leaders in power, form factor, and price optimization.

These devices have tiny footprints of 5 x 5 mm and 3 x 3 mm, respectively, so using them in a dense, size constrained design means that you have more space for other necessary devices. Compared to other low-power devices on the market, the Trion T8 FPGAs have the lowest static and dynamic power in the industry. They are great choices if you have a small footprint need for I/O expansion, bridging, translation, and even some processing. The largest T8 can even accommodate an 易灵思 Opal RISC-V SoC and other functions needed for your design.

The reason that Trion T4 and T8 FPGAs excel on low power is twofold:

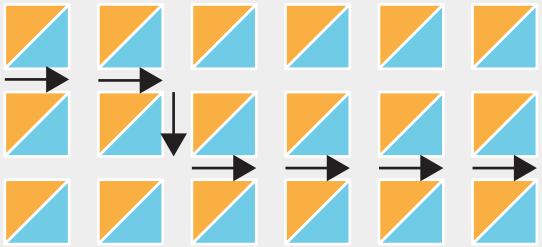
- First, the process fabrication node 易灵思 chose is a low-power process that is optimized for the lowest leakage with a V_{CC} of 1.1 V.
- Second, the Quantum architecture, which is the basic technology underlying our FPGAs, drives the smallest die size and provides power advantages for of all our Trion FPGAs.

Static current, though typically less significant compared to dynamic current, becomes important for battery-operated or power sensitive systems. Reducing the static current is beneficial especially when the device is powered-up but not active. Trion static power is extremely low, and that is the essential foundation on which to build an overall low-power device.

All Trion FPGAs are built on the Quantum architecture, which is a fabric consisting of eXchangeable Logic and Routing, or XLR, tiles. These tiles can function as either "routing or "logic", depending on what your specific design needs. This groundbreaking architecture gives you the flexibility to optimize your design into the smallest device needed, while also allowing for very high utilization levels of the available logic elements in each FPGA.

XLR Equals Low Power:

- Trion FPGAs are a "sea" of XLR tiles
- Logic is a 4-input LUT
- Routing is a short wire
- Architecture is low power by design



As discussed previously, in FPGAs the overall system power can be highly affected by I/O usage. Trion FPGAs provide significant advantages for I/O power. As your design requires more I/O pins, Trion FPGA's lead in power savings only increases. Obviously, all designs are unique and different, so you need to test out your own use cases to confirm the effect in your specific design. If power and size is a challenge you are currently facing, you should take a serious look at the Trion devices, specifically the T8 and T4 devices. Table 1 provides power consumption data for several typical designs.

The T4 and T8 FPGAs are not just slimmed down devices. These FPGAs have many features and capabilities that are not always included in other small FPGA solutions, such as 18 x 18 multiplier blocks, embedded block memory, and on-chip oscillators. The 49-ball and 81-ball BGA packages have 33 and 55 I/O pins, respectively, can support multiple I/O

Table 1 Comparing T8 Power

	T8 FPGA (mW)	Similar-Sized Competitor (mW)	Notes
Static power	0.168	0.478	
UART	2	3.6	Uses about 4K LEs. opencores.org/projects/uart16550
AES	1.65	6.48	Uses about 1K LEs and lots of I/O pins.
PWM	1.5	3.27	Uses about 200 LEs.
Keyboard controller	6.14	32	Uses about 500 LEs for an I/O intensive, faster design. opencores.org/projects/keyboardcontroller

voltages, and have four banks of I/O pins. These FPGAs are also available in both industrial and commercial temperature grades. In all, these small, low-power, and price optimized FPGAs support a lot of flexibility.

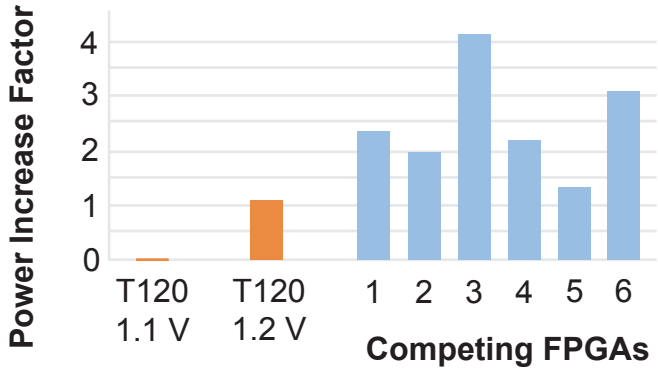
Higher Density Trion FPGAs

The Quantum architecture die size advantage and our fabrication node helps our larger FPGAs also lead the competition as the lowest power FPGAs in the market. Although these FPGAs do not use the T4 and T8's specialized transistors to achieve ultra low power, Trion FPGAs from the T13 up to the T120 deliver lower power compared to similar size devices. Using hardened blocks for MIPI/CSI-2 and DDR3 DRAM controllers also drive lower power compared to similar-sized competitive devices. A dedicated function block inherently achieves lower power than using logic elements to create a similar function.

To illustrate how the Quantum architecture results in lower power for the larger Trion FPGAs, 易灵思 performed an analysis for a range of designs (see Table 2). The comparison devices represent several other vendors with process nodes from 60 nm to 28 nm (see Table 3). All of the power numbers reflect the designs running at the same f_{MAX}. Several designs did not fit into the comparison FPGAs 5 and 6.

As the results in Figure 1 and Table 4 show, T120 FPGAs are lower power for nearly all designs with the average ratio ranging from a 3.5x to 1.3x power improvement.

Figure 1 Comparing T120 Power



Power ratio compared to T120 at 1.1 V core voltage.

Table 2 Designs Used for T120 Power Comparison

Design	Description	Origin
1	AES-128 pipelined cypher	opencores.org/projects/aes-128_pipelined_encryption
2	Floating point calculation (FPU)	opencores.org/projects/double_fpu
3	Gaussian noise generator	github.com/liuguangxi/gng
4	10 Gigabit Ethernet MAC	opencores.org/projects/xge_mac
5	Open RISC 1200 soft processor	github.com/juliusbaxter/mor1kx-dev-env/tree/master/boards
6	Reed–Solomon encoder/decoder	en.pudn.com/Download/item/id/1960919.html
7	Secure hash algorithm (SHA)	易灵思 design
8	Secure hash algorithm (SHA512)	易灵思 design
9	Viterbi decoder	易灵思 customer design, used with permission

Table 3 FPGAs Used for T120 Power Comparison

	T120	FPGA 1	FPGA 2	FPGA 3	FPGA 4	FPGA 5	FPGA 6
Process	40 nm	60 nm	28 nm	45 nm	28 nm	40 nm	28 nm
LE equivalents	112,000	114,000	149,500	147,400	101,000	84,000	100,000
Package Pins/GPIO	484	484	484	484	484	381	324
GPIO	256	280	240	338	285	205	210
Multipliers/DSP blocks	320	266	312	180	240	156	188
Memory (kbits)	5,407	3888	6860	4824	4860	3744	5148
Memory blocks	1056	432	686	268	135	208	286
Speed grade	C4	C7	C7	-3	-2	8	N/A

Table 4 T120 Power Comparison Data[1] [2]

Design	T120 1.1 V (mW)	T120 1.2 V		FPGA 1		FPGA 2		FPGA 3		FPGA 4		FPGA 5		FPGA 6	
		mW	Ratio	mW	Ratio	mW	Ratio	mW	Ratio	mW	Ratio	mW	Ratio	mW	Ratio
1	850	1016	1.2	No fit	–	603	0.7	1148	1.4	827	1.0	519	0.6	No fit	–
2	514	614	1.2	1319	2.6	1038	2.0	670	1.3	475	0.9	No fit	–	No fit	–
3	565	676	1.2	1410	2.5	1160	2.1	2351	4.2	1804	3.2	No fit	–	1655	2.9
4	573	685	1.2	1674	2.9	1206	2.1	2152	3.8	1461	2.6	No fit	–	No fit	–
5	305	365	1.2	1053	3.4	910	3.0	865	2.8	436	1.4	279	0.9	1411	4.6
6	373	446	1.2	1157	3.1	605	1.6	4964	13.3	2041	5.5	728	2.0	573	1.5
7	414	495	1.2	924	2.2	881	2.1	1328	3.2	746	1.8	716	1.7	1237	3.0
8	428	512	1.2	1039	2.4	898	2.1	1565	3.7	866	2.0	No fit	–	No fit	–
9	393	470	1.2	983	2.5	819	2.1	No fit	–	1024	2.6	1024	2.6	1333	3.4
Average			**1.2**		**2.7**		**2.0**		**4.2**		**2.3**		**1.6**		**3.1**

1. Power numbers are rounded to the nearest whole number.
2. All ratios are compared to the 1.1 V T120 power usage.

钛金系列 Power Advantage

With our 16 nm Trion 钛金系列 family, which has an enhanced Quantum compute fabric, 易灵思 provides a new class of devices balancing performance, power, and package size,letting you use 钛金系列 FPGAs in applications that would not be able to accommodate a traditional FPGA due to power and package size. This new family will extend 易灵思's power leadership by packing more compute and low power into tiny packages.

Software Support

All Trion and 钛金系列 devices are supported by our easy-to-use Efinity® integrated development environment. The Efinity software is a fully enabled tool, supporting VHDL, Verilog HDL, and System Verilog synthesis languages, along with timing-driven place and route, bitstream generation, debugging, and programming. The Efinity software is supported on Windows and Linux platforms and has both a graphical user interface and a command-line flow.

In Conclusion

If you are trying to the juggle requirements of a mobile or size-constrained design, you should add the Trion T8 and T4 FPGAs to your consideration list. These FPGAs lead in both static and dynamic power, and with packages as small as 3 x 3 mm, you will be challenged to find a better FPGA solution.

For larger designs, for example for video or sensor processing or aggregation, the T13 through T120 FPGAs offer hardened MIPI CSI-2 and DDR DRAM controller interfaces, enough logic for complex functions, and low power.

The value of FPGAs in general is in their flexibility, quick time to market, and "do anything" capability, so using FPGAs in your design can allow you to fix issues without needing to re-spin and redesign boards. This versatility can help you get to market quicker and maximize your engineering effort. Additionally, with Trion FPGAs, you get all of this flexibility at an affordable price, something for which FPGAs have not traditionally strived to accomplish or been known for.

Competing FPGAs can't take their heat.

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