易灵思®

钛金系列 Packaging User Guide

UG-TI-PKG-v2.0
February 2021
www.elitestek.com

Contents

Introduction

易灵思 offers 钛金系列 FPGAs in packages that are designed for the device's maximum number of user I/O pins. This document describes 钛金系列 FPGA pin and package specifications as well as solder reflow guidelines.

Learn more: Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

Available Package Options

Table 1: 钛金系列 Package Options

Package	Pitch (mm)	Size (mm)	Ti35	Ti60	Ti90	Ti120	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
64-ball WLCSP	0.4	3.5x3.4		✓								
100-ball FBGA	0.5	5.5x5.5	✓	✓								
225-ball FBGA	0.65	10x10	✓	✓	✓	✓	✓					
361-ball FBGA	0.65	13x13			✓	✓	✓					
484-ball FBGA	0.65	15x15			✓	✓	✓	✓	✓			
484-ball FBGA	0.8	18x18			✓	✓	✓					
529-ball FBGA	0.8	19x19			✓	✓	✓					
625-ball FBGA	0.65	17x17						✓	✓	✓	✓	
784-ball FBGA	0.8	23x23						✓	✓	✓	✓	✓
1,156-ball FBGA	1.0	35x35								✓	✓	✓

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

Device Pinout File

易灵思 provides pinout files for 钛金系列 FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Download: Download the pinout files from the Documentation page in the Support section of the 易灵思® web site (www.elitestek.com/support)

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: Power and Ground Pinouts

xx indicates the bank location.

Function	Description
VCC	Core power supply.
VCCA_*xx*	PLL analog power supply.
VCCAUX	1.8 V auxiliary power supply.
VCCIO33_*xx*	HVIO bank power supply.
VCCIO*xx*	HSIO bank power supply.
VCCIO*xx_yy_zz*	Power for HSIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C
GND	Ground.

Table 3: GPIO Pinouts

x indicates the location (T, B, L, or R); *xx* indicates the bank location; *n* indicates the number; *yyyy* indicates the function.

Function	Direction	Description
GPIO*x_n*	I/O	HVIO for user function. User I/O pins are single-ended.
GPIO*x_n_yyyy*	I/O	HVIO or multi-function pin.
GPIO*x*_N_*n* GPIO*x*_P_*n*	I/O	HSIO transmitter, receiver, or both.
GPIO*x*_N_*n_yyyy* GPIO*x*_P_*n_yyyy*	I/O	HSIO transmitter, receiver, both, or multi-function.
REF_RES_*xx*	–	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 10 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.

Table 4: Alternate Function Pinouts

n is the number.

Function	Direction	Description
CLK*n*	Input	Global clock and control network resource. The number of inputs is package dependent.
PLLIN*n*	Input	PLL reference clock resource. The number of reference clock resources is package dependent.

Table 5: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up During Configuration
CDONE[1]	Bidirectional	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode.	✓
CRESET_N[1]	Input	Initiates FPGA re-configuration (active low). Pulse CRESET_N low for a duration of t_{creset_N} before asserting CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	✓
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	✓
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

[1] CDONE and CRESET_N have a drive strength of 12 mA at 1.8 V.

Table 6: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up During Configuration
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	N/A
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock.	N/A
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI*n* (31:0) connects to the data bus in parallel.	N/A
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration (SPI and JTAG configuration).	✓
CSO	Output	Chip select output. Selects the next device for cascading configuration. (2)	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SSL_N	Input	Active-low configuration mode select. The FPGA senses the value of SSL_N when it comes out of reset (pulse CRESET_N low to high). 0: Passive mode 1: Active mode In active configuration mode, SSL_N serves as a chip select to the flash device 1 (CDI0 - CDI3).	✓
SSU_N	Input	In active configuration mode (dual quad mode), SSU_N serves as a chip select to the flash device 2 (CDI4 - CDI7).	✓
EXT_CONFIG_CLK	I/O	In active mode, EXT_CONFIG_CLK pin is connected from an external clock, to be used as a configuration clock.	N/A
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓

(2) Cascaded configuration is not supported in the F100S3F2 package.

64-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 64-Ball WLCSP Pinout Diagram

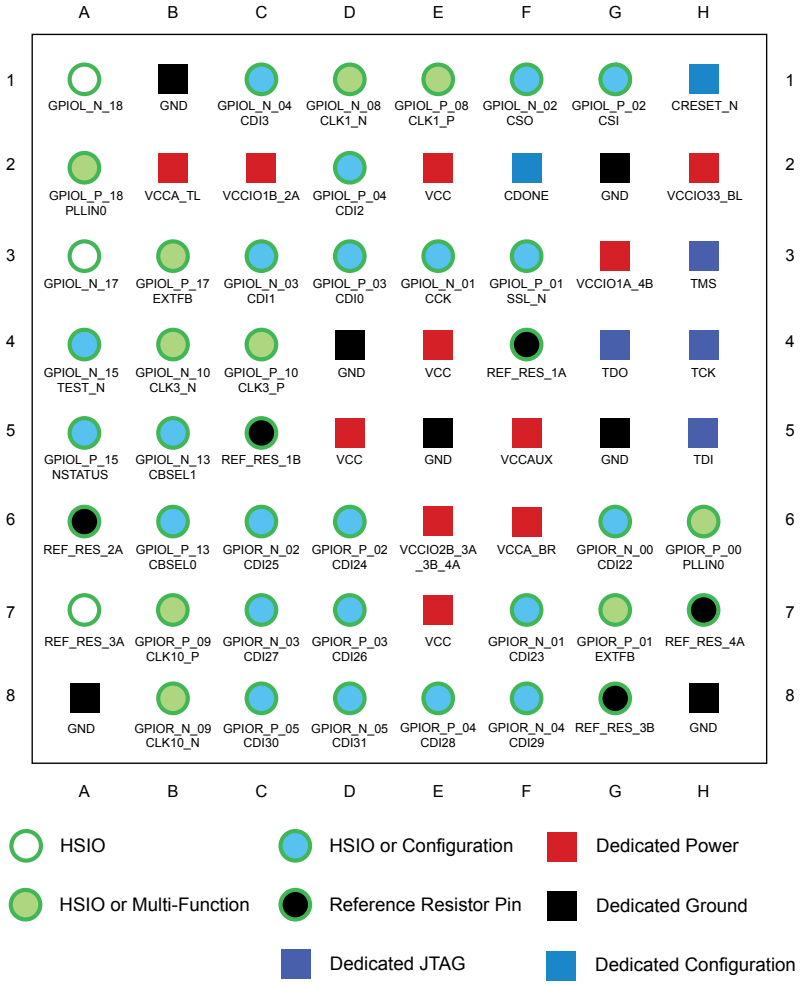


Figure 2: 64-Ball WLCSP I/O Bank Diagram

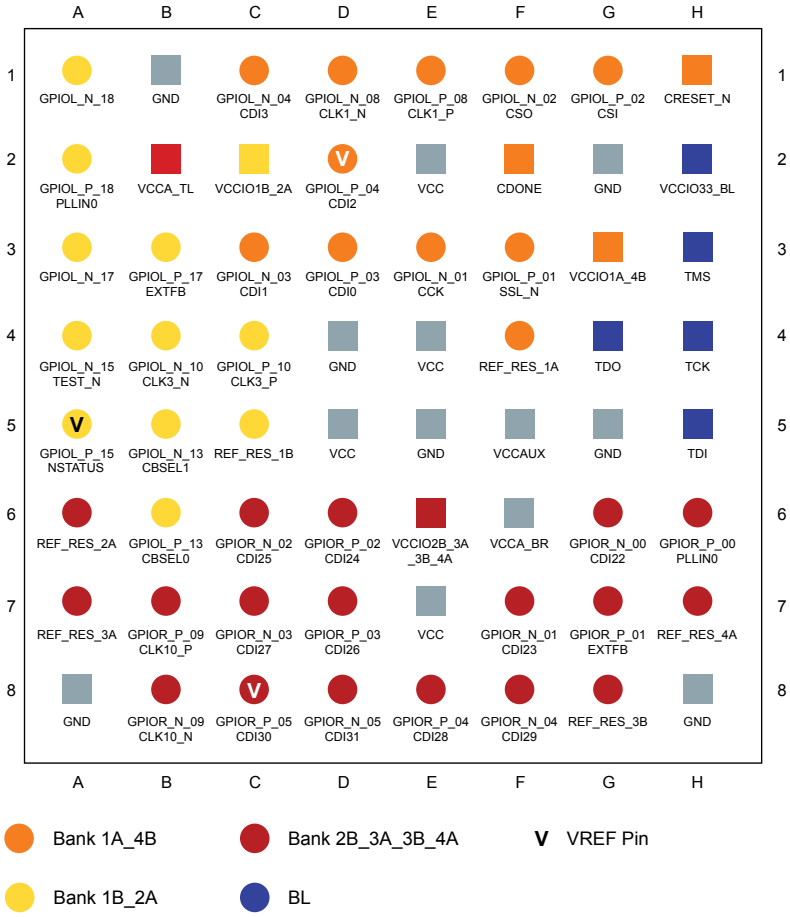


Figure 3: 64-Ball WLCSP MIPI RX Groups

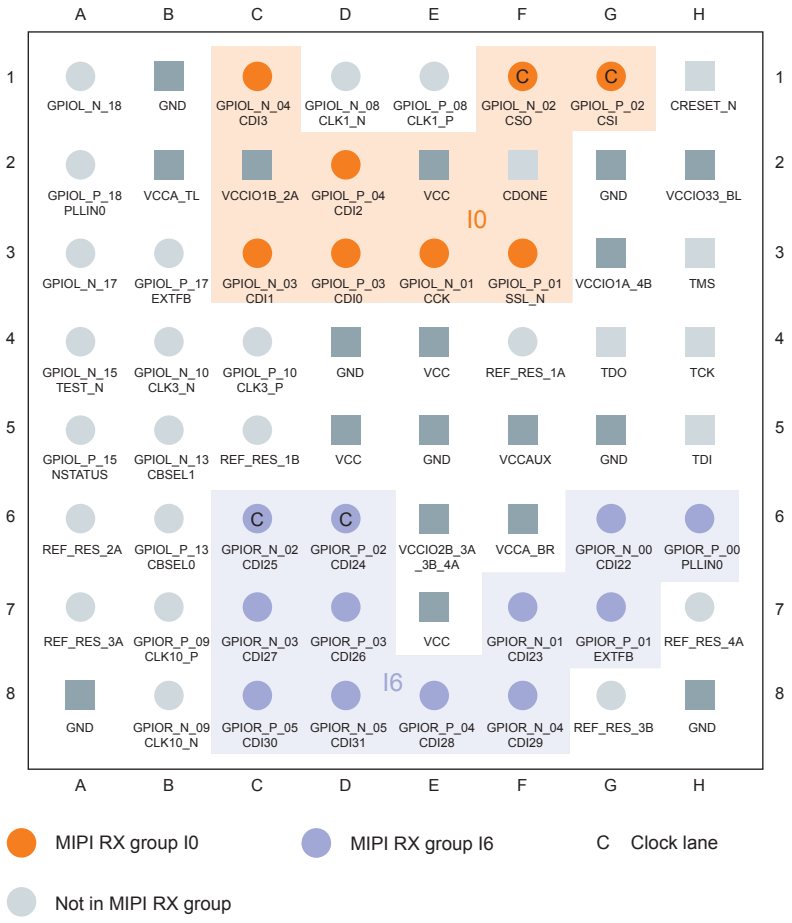


Figure 4: 64-Ball WLCSP Package Marking

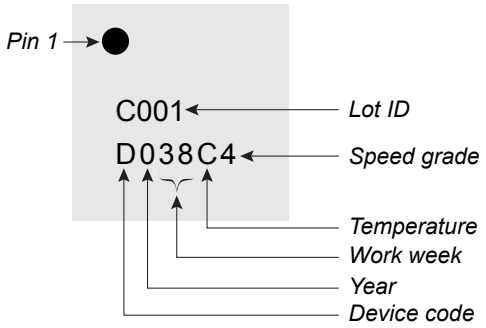
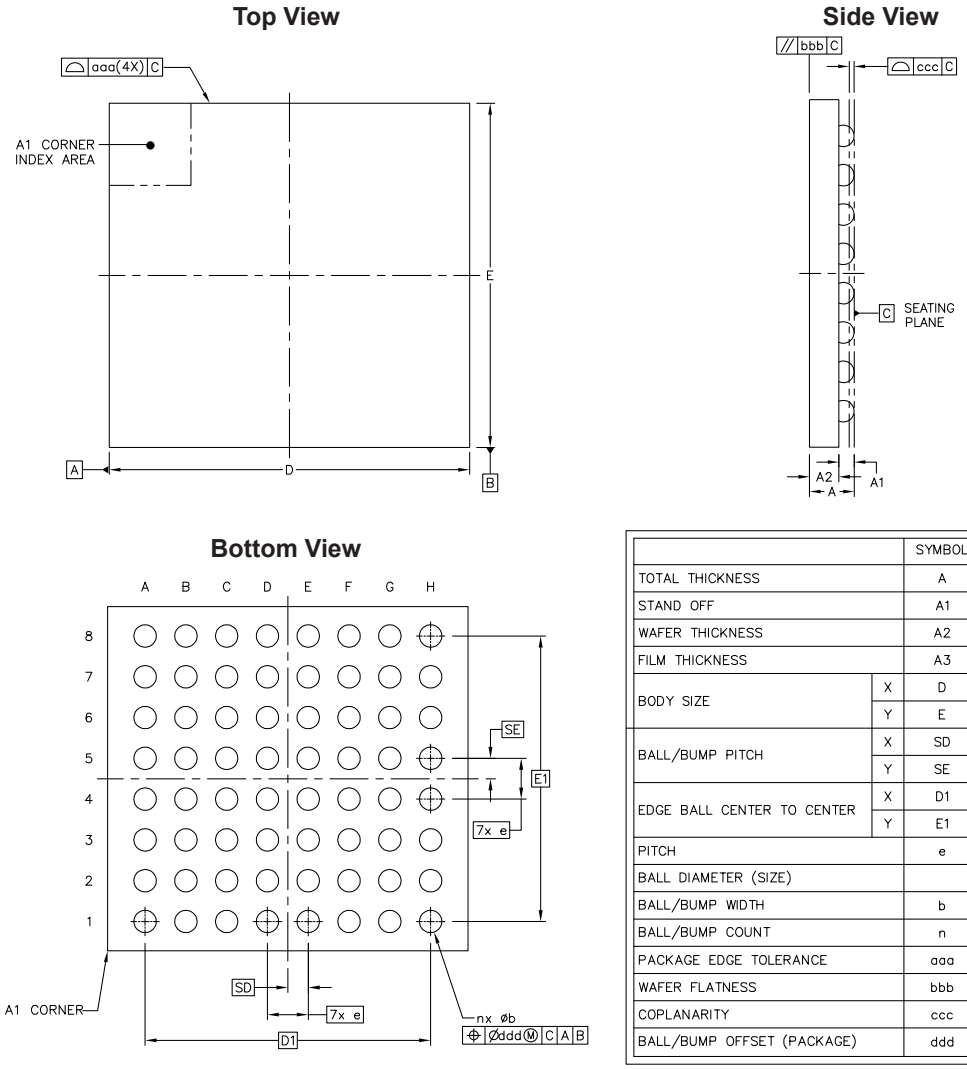


Figure 5: 64-Ball WLCSP Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.405	0.455	0.505
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.28	0.3	0.32
FILM THICKNESS		A3	---	---	---
BODY SIZE	X	D	3.5353		
	Y	E	3.3753		
BALL/BUMP PITCH	X	SD	0.2		BSC
	Y	SE	0.2		BSC
EDGE BALL CENTER TO CENTER	X	D1	2.8		BSC
	Y	E1	2.8		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	64		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.05		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

100-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 6: 100-Ball FBGA Pinout Diagram

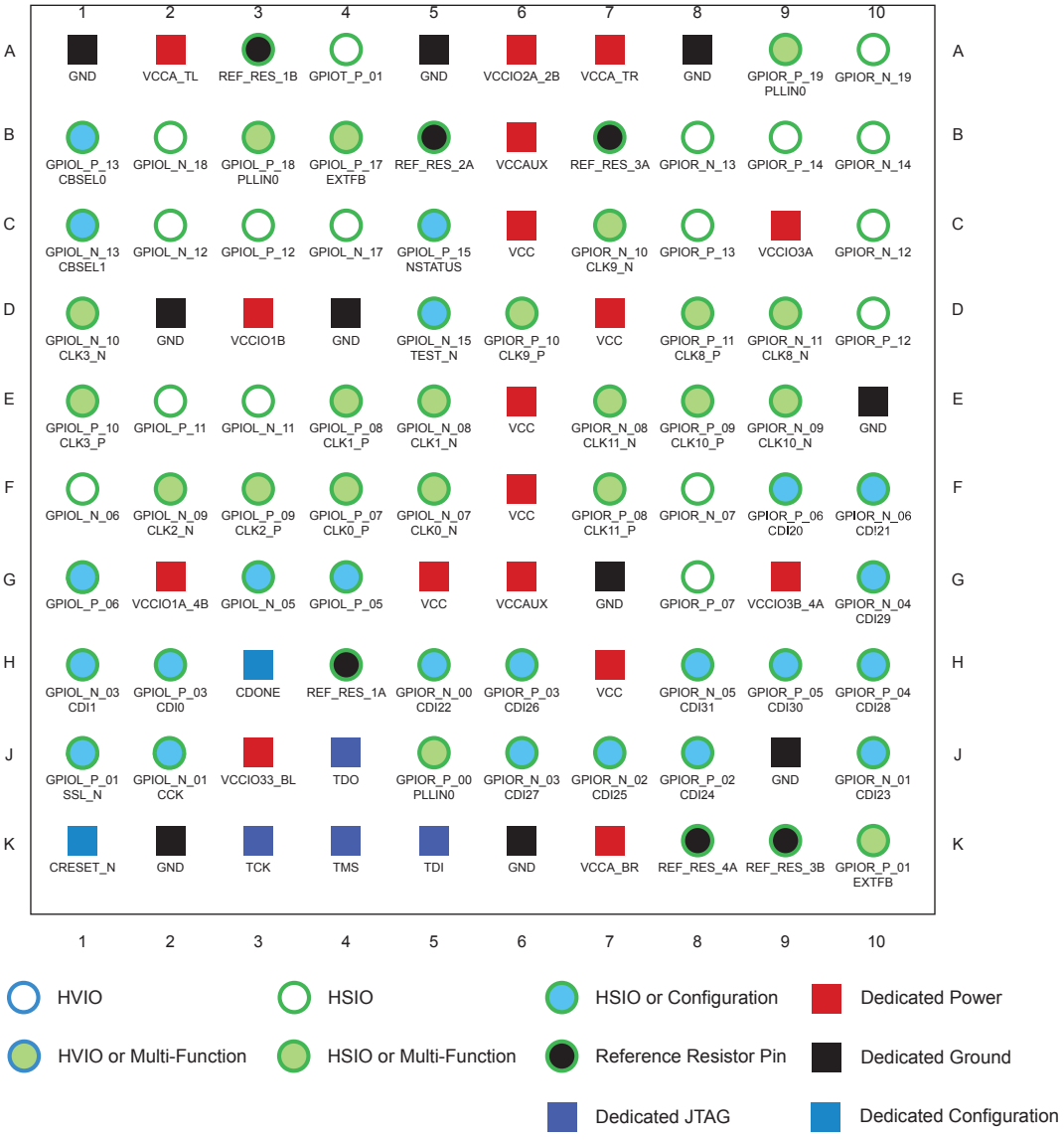
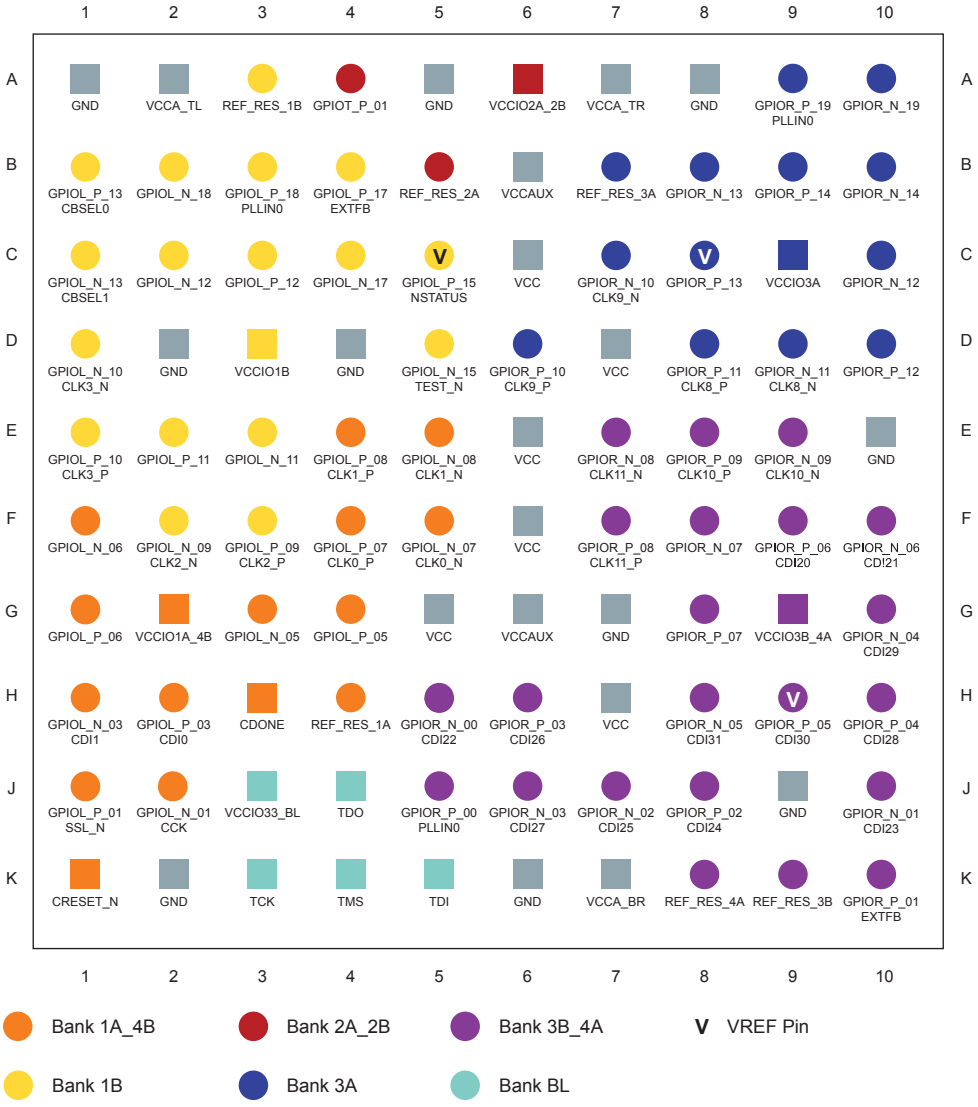


Figure 7: 100-Ball FBGA I/O Bank Diagram



Bank 1A_4B Bank 2A_2B Bank 3B_4A V VREF Pin

Bank 1B Bank 3A Bank BL

Figure 8: 100-Ball FBGA MIPI RX Groups

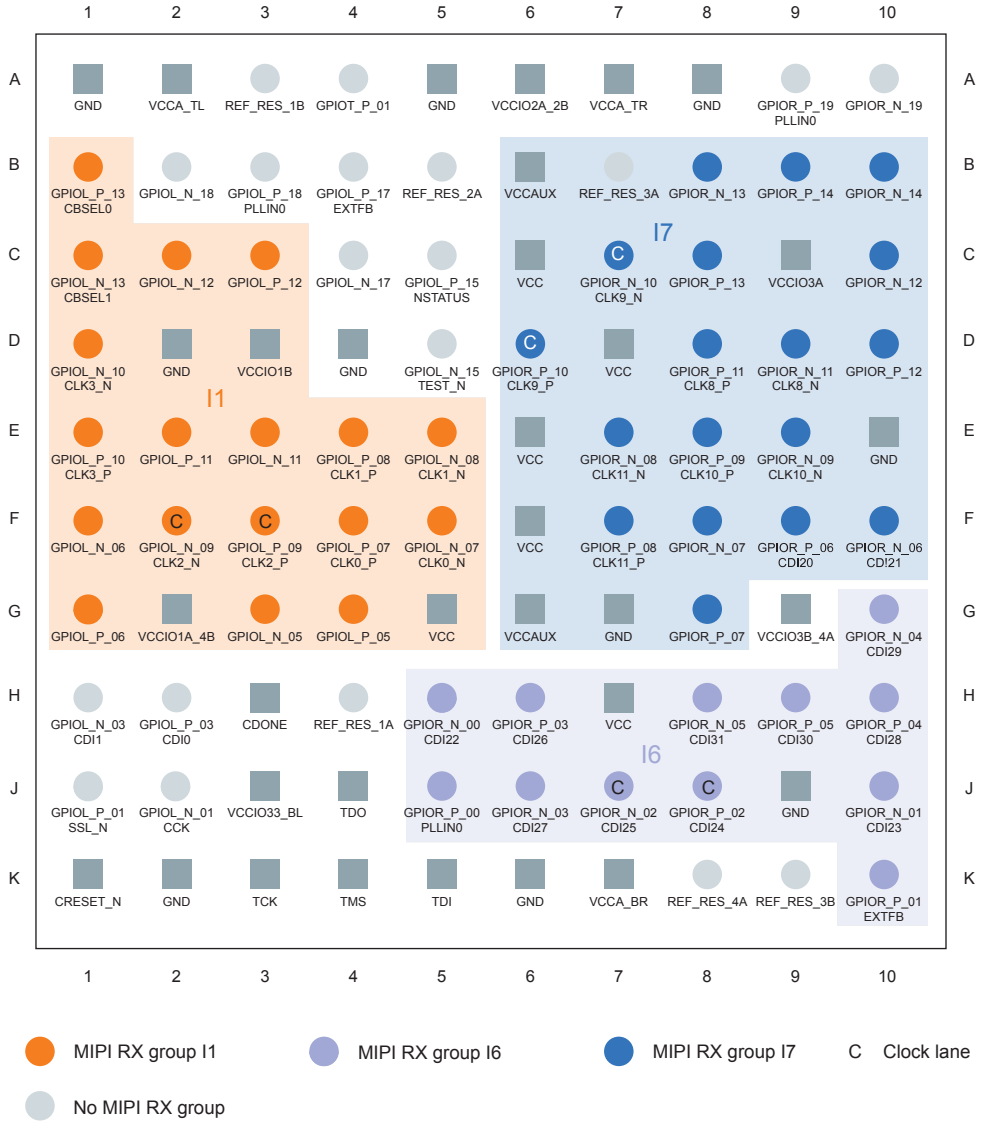


Figure 9: 100-Ball FPGA FBGA Package Marking

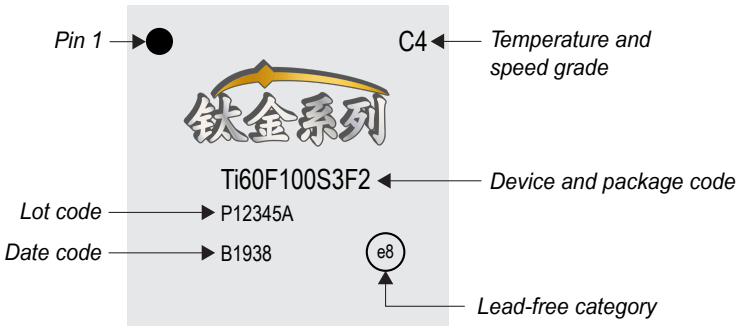
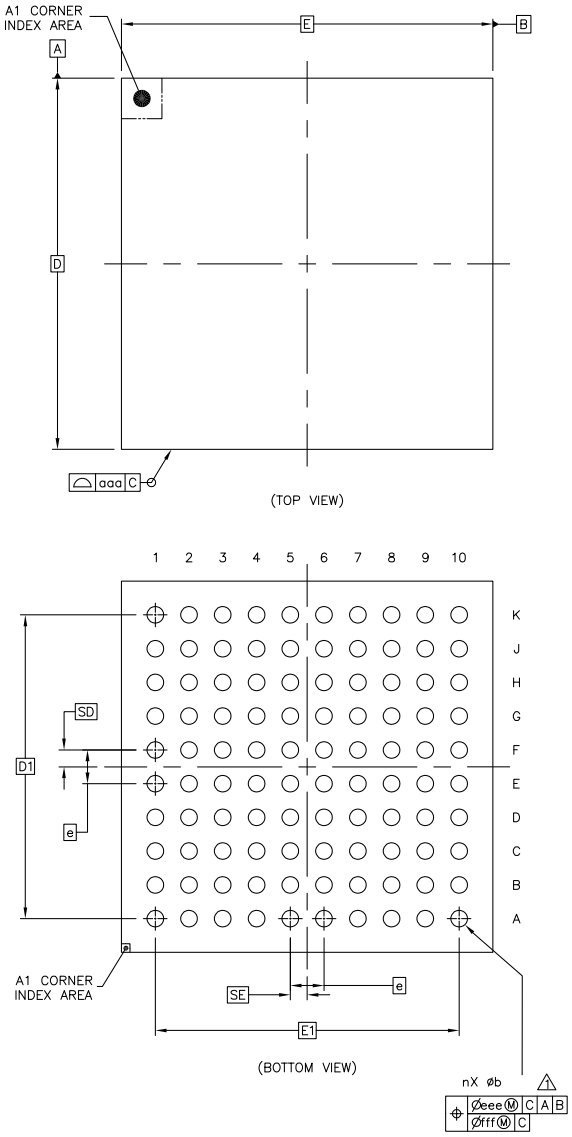


Figure 10: 100-Ball FBGA FBGA Package Outline



NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.105	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		5.5	BSC
	E		5.5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.5	BSC
BALL COUNT	n		100	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.25	BSC
	SE		0.25	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

225-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Note: Refer to the F225 Escape Routing on page 30 for escape routing example.

Figure 11: 225-Ball FBGA Pinout Diagram

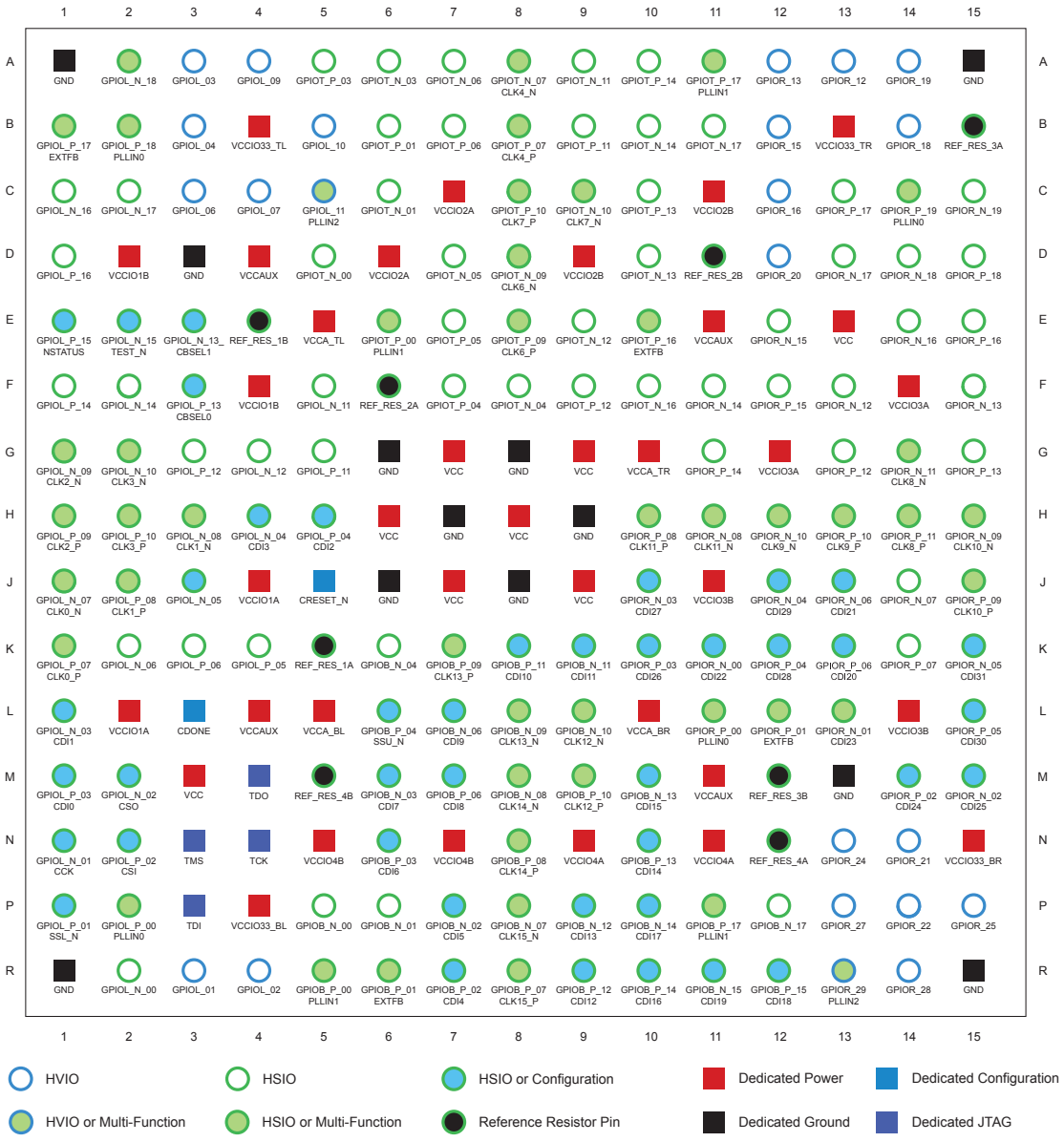


Figure 12: 225-Ball FBGA I/O Bank Diagram

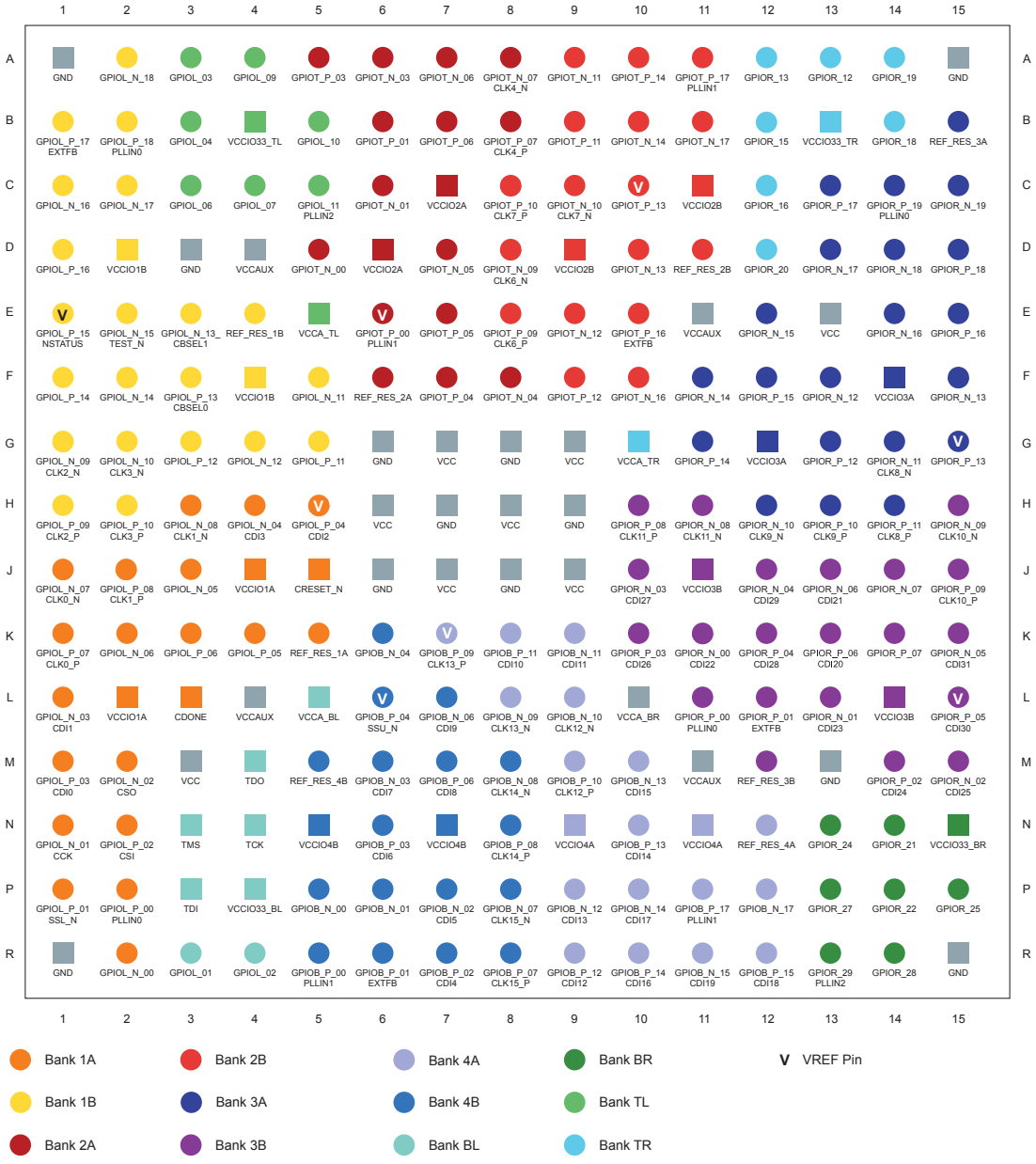


Figure 13: 225-Ball FBGA MIPI RX Groups

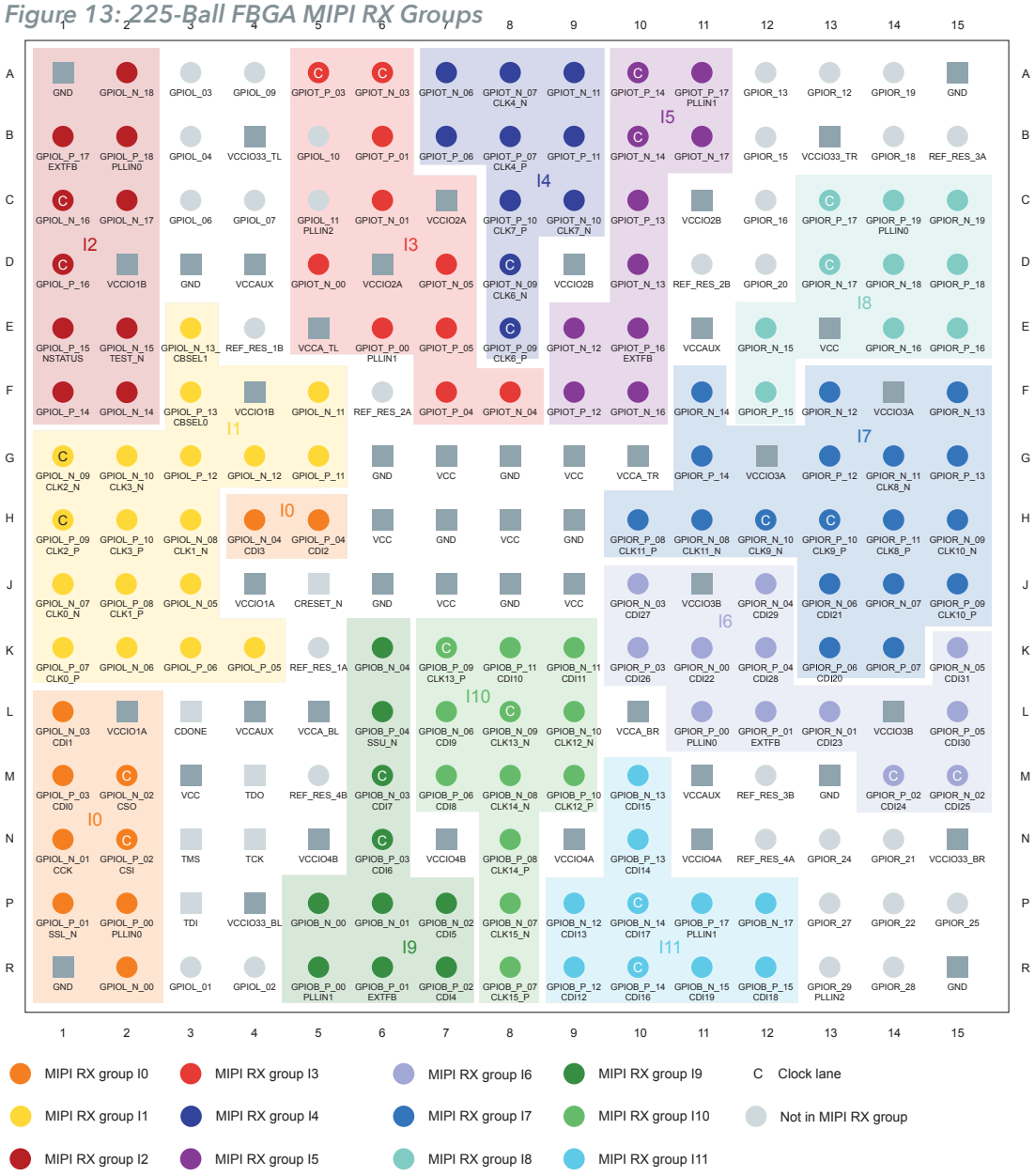


Figure 14: 225-Ball FPGA FBGA Package Marking

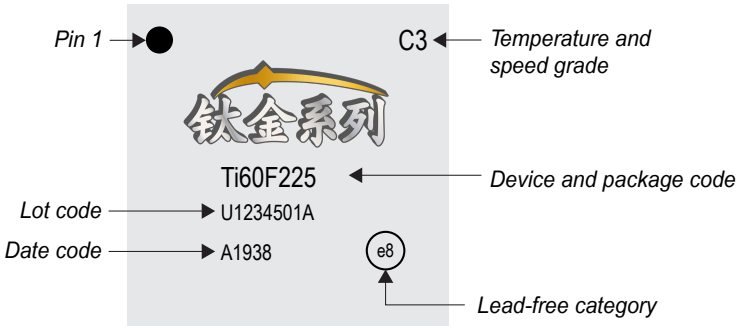
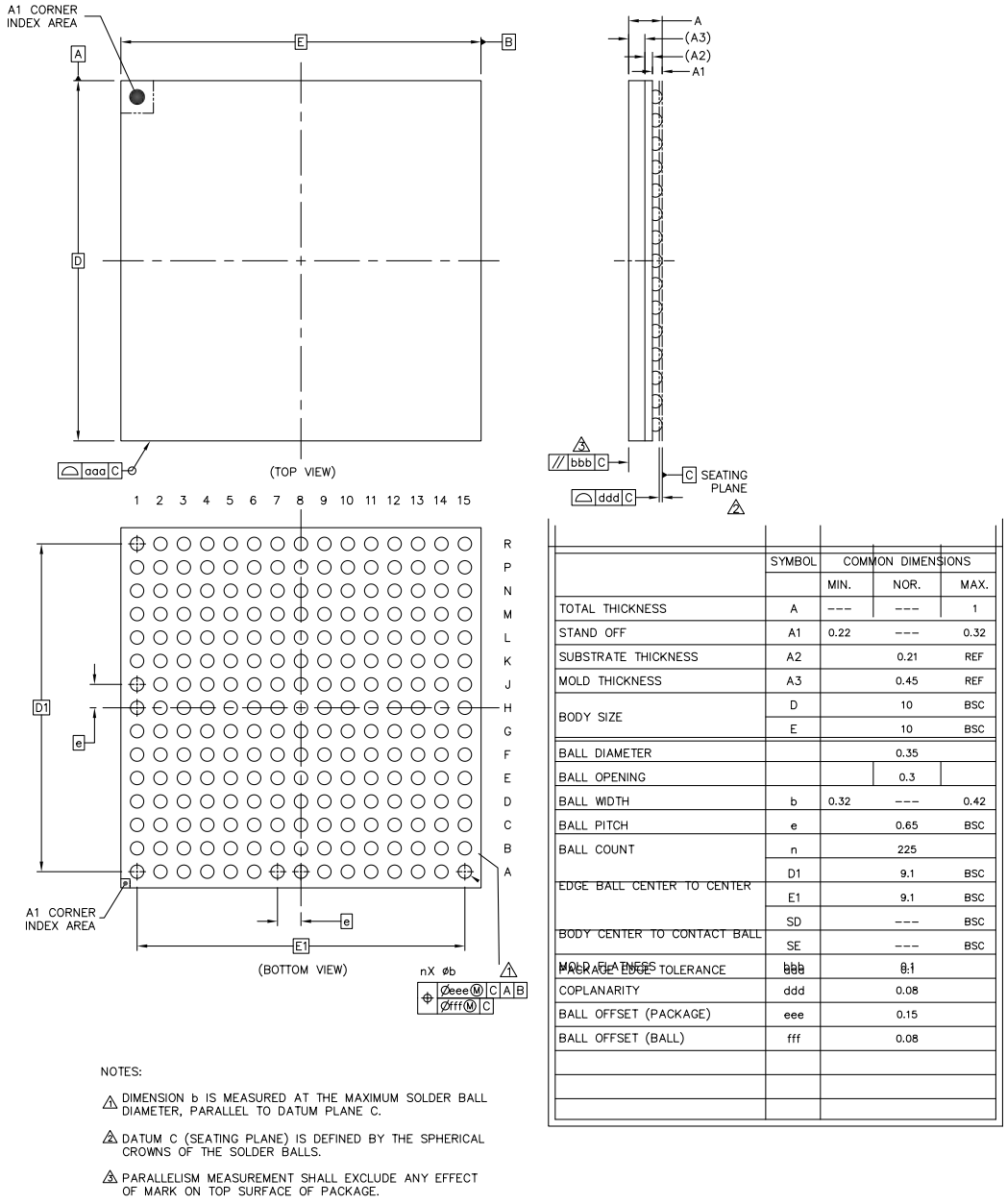


Figure 15: 225-Ball FBGA FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 16: 484-Ball Pitch FBGA Pinout Diagram

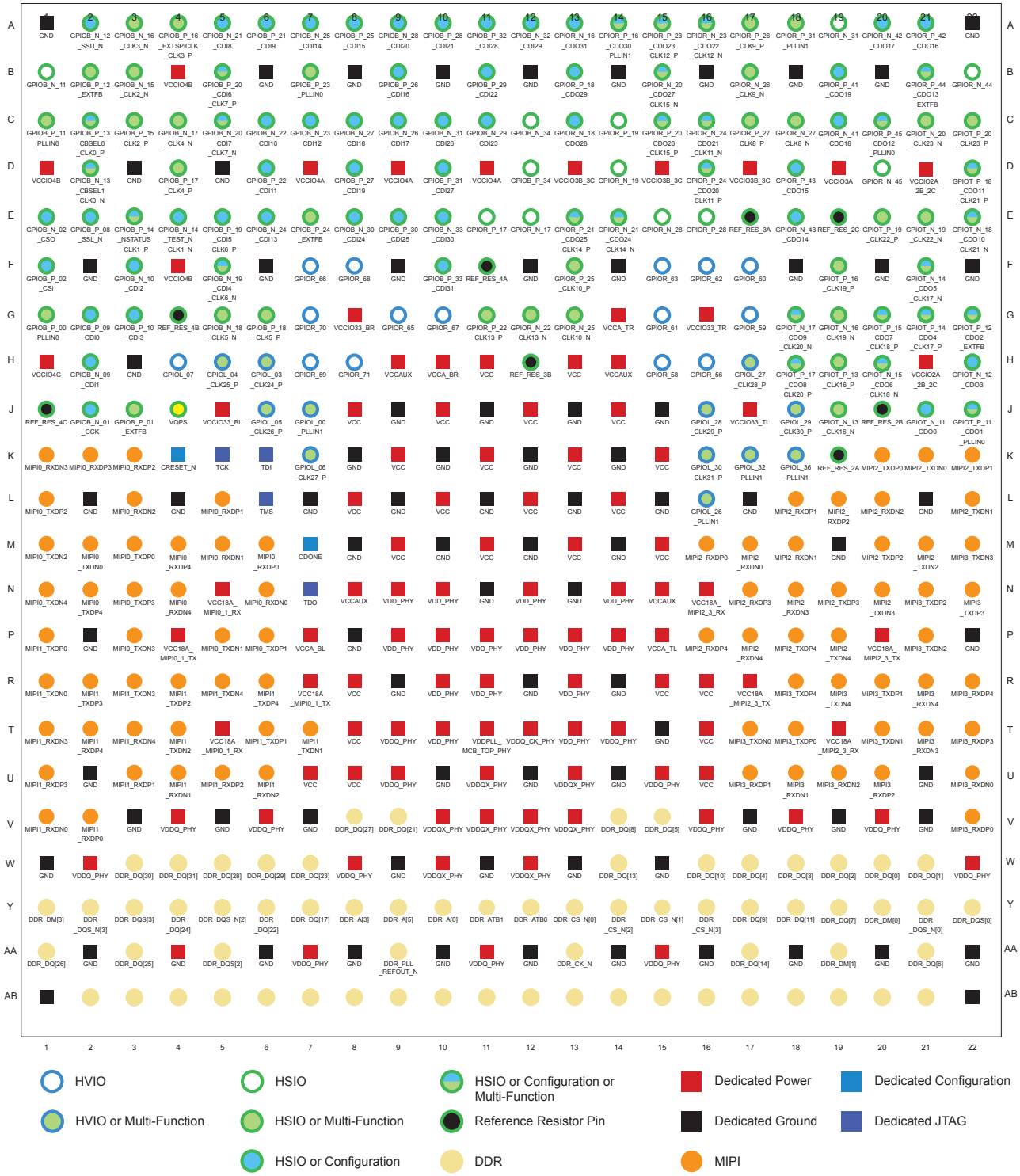


Figure 17: 484-Ball Pitch FBGA I/O Bank Diagram

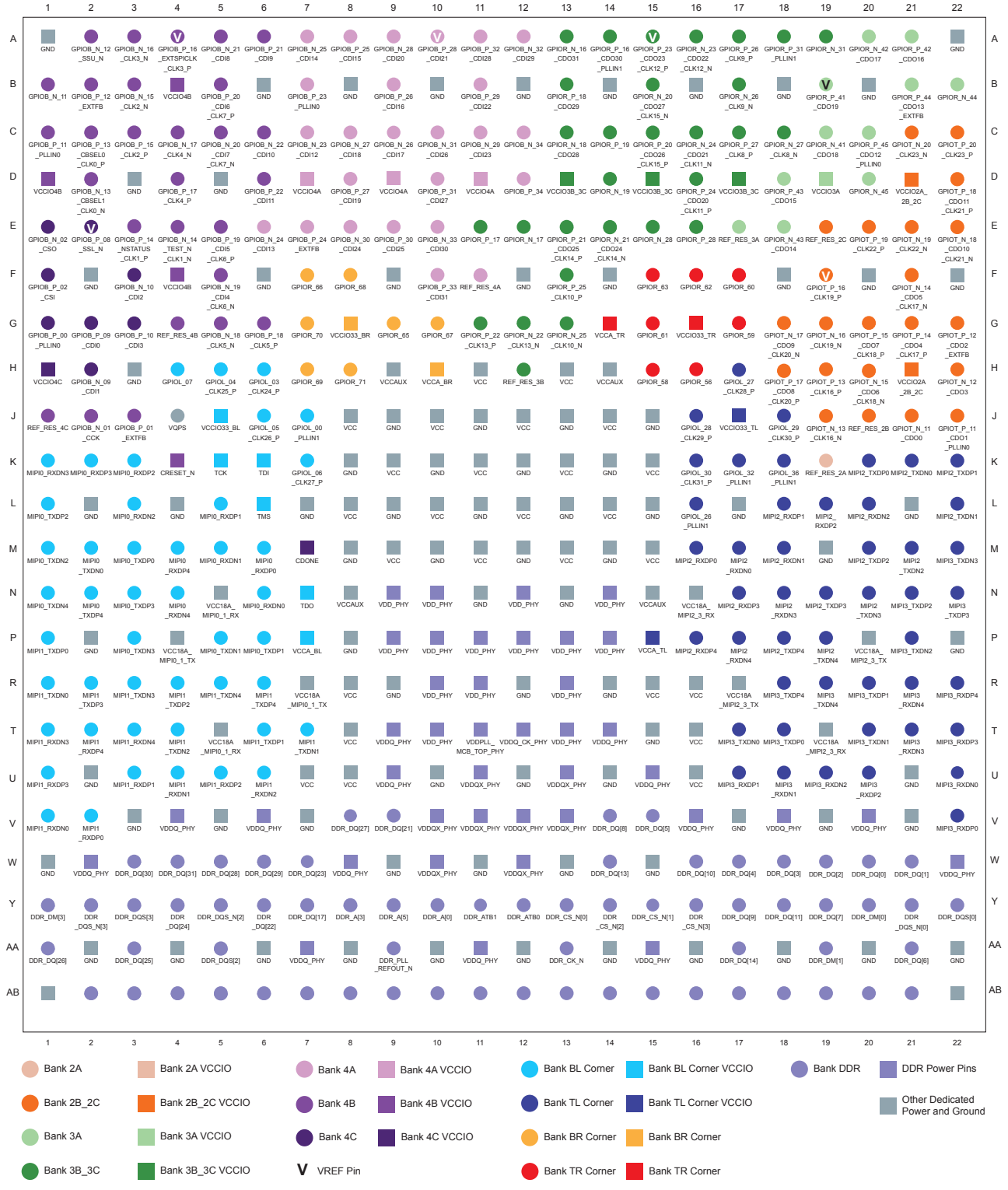


Figure 18: 484-Ball Pitch FBGA MIPI RX Groups

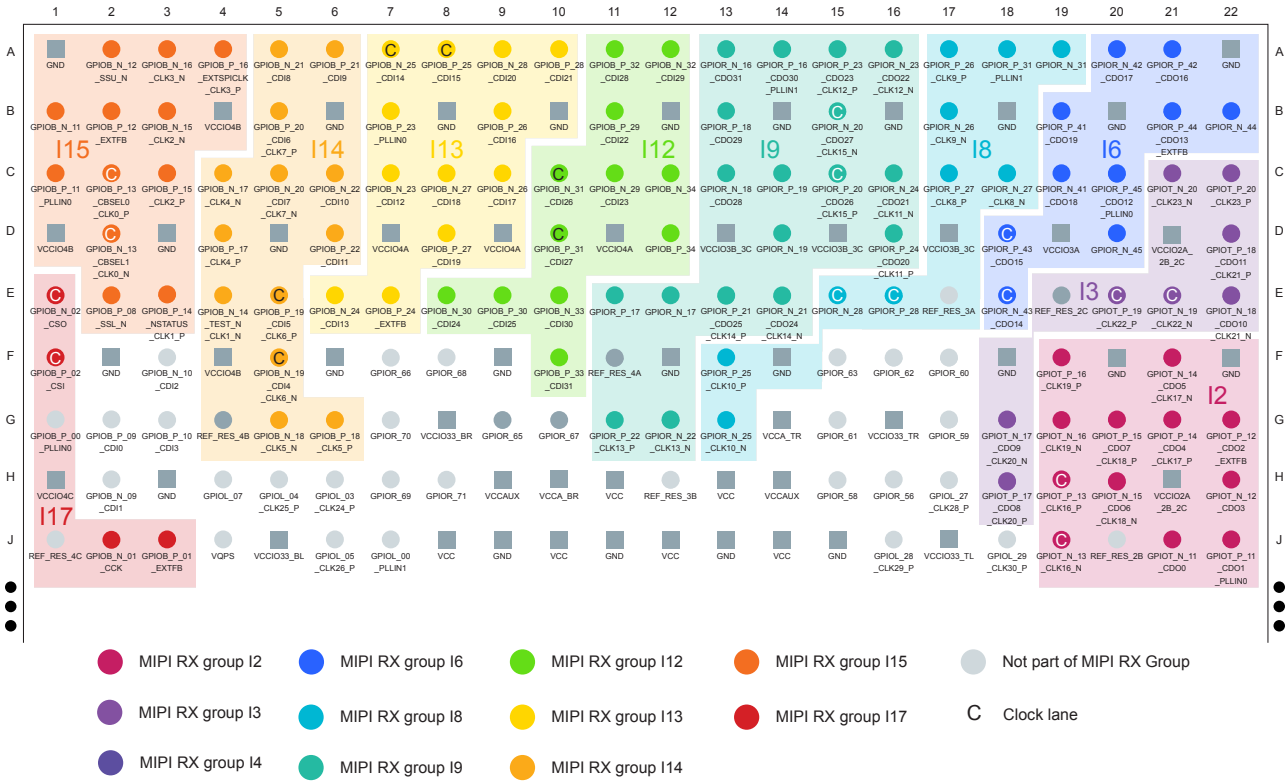


Figure 19: 484-Ball FPGA Pitch FBGA Package Marking

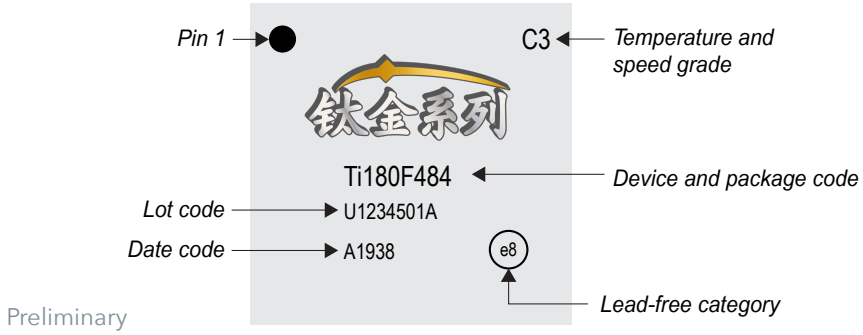
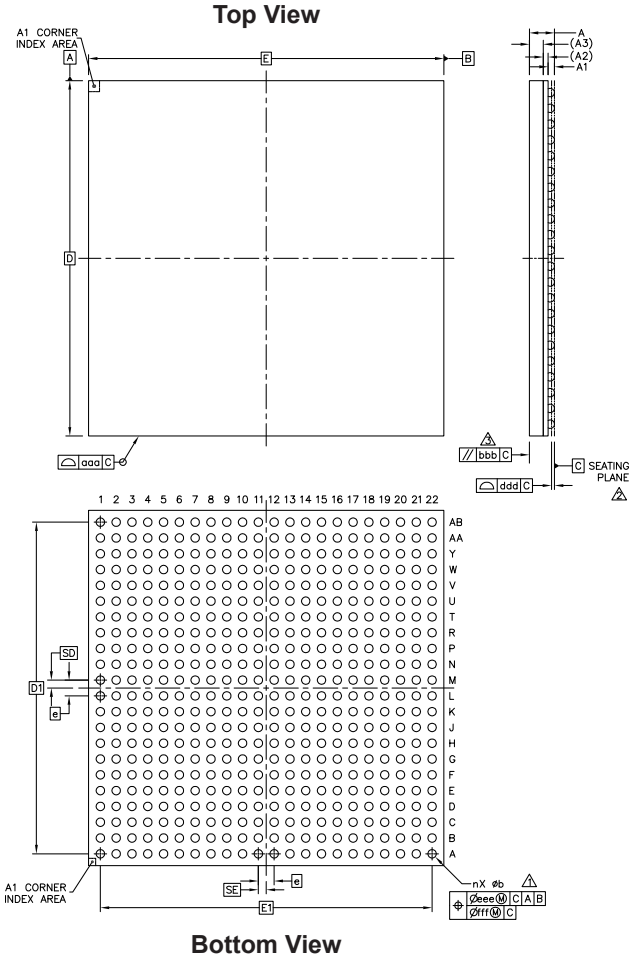


Figure 20: 484-Ball Pitch FBGA FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for 易灵思® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its own profile, which depends upon the reflow equipment used and the board design. You must characterize each PCB to find the profile that is reliable.

Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

易灵思 does not recommend BGA reballing. Reballed BGA packages void the original 易灵思® specifications.

Peak Reflow Temperatures

Table 7: Peak Reflow Temperature (Tp) by Package

Package	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
WLCSP	64	1	260
FBGA	100	3	260
FBGA	225	3	260
FBGA	484	(3)	(3)

Note: These packages are "green" and RoHS compliant.

(3) Pending characterization.

Reflow Profile for SMT Packages

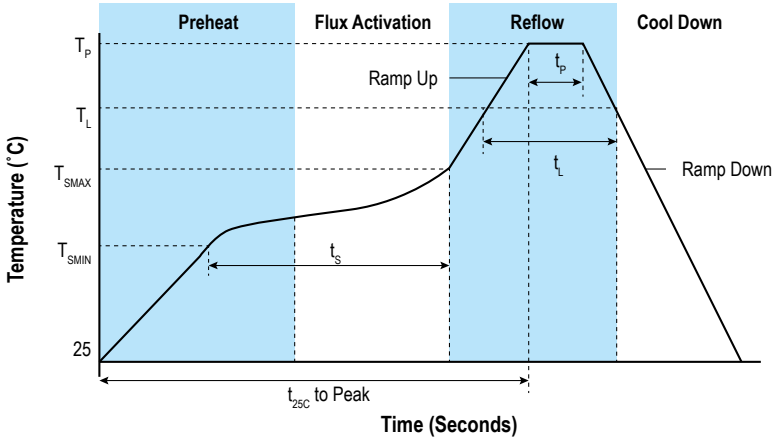
The reflow process usually includes four phases:

1. **Preheat Phase—**The preheat phase brings the assembly from 25 °C to T_S. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
   - **Solder Ball Spattering—**Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
   - **Bridging—**Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase—**As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase—**The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase—**Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 8: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_P	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
t_{25C} to T_p	Time from 25 °C to peak temperature	8 minutes maximum

Figure 21: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. 易灵思® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices, and user applications. Because of this, 易灵思 FPGAs do not come with preset thermal solutions.

Table 9: Device/Package Thermal Resistance

Measurements taken at 25 °C ambient temperature.

Device	Package	Pitch	Dimensions (mm)	Θ_{JA} (°C/W) Still Air	Θ_{JA} (°C/W) 1 m/s	Θ_{JA} (°C/W) 2 m/s	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
Ti60	WLCSP64	0.4	3.5 x 3.4	37.24	33.56	32.42	11.95	0.14
Ti60	FBGA100	0.5	5.5 x 5.5	45.62	41.53	40.14	26.13	20.35
Ti60	FBGA225	0.65	10 x 10	36.89	33.15	32.03	22.32	11.03
Ti180	FBGA484	0.8	18 x 18	(4)	(4)	(4)	(4)	(4)

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance
- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

(4) Pending characterization.

PCB Guidelines for BGA Packages

Solder Mask Defined Guidelines

易灵思 provides solder mask defined (SMD) diameter information. Use this data when creating your board layout so that the board pads match the landing pads.

Figure 22: SMD Pad Specification

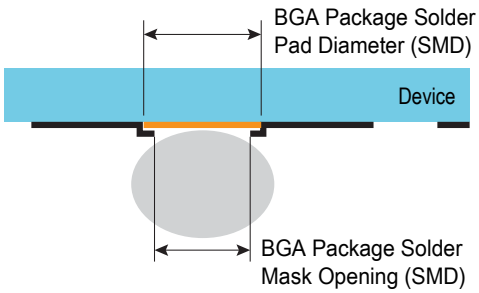


Table 10: PCB Solder Pad Recommendations

Package	Pitch (mm)	BGA Package Solder Mask Opening (mm)	Optimum PCB (SMD) Opening (mm)
WLCSP64	0.4	N/A	0.2
FBGA100	0.5	0.325	0.245
FBGA225	0.65	0.4	0.3
FBGA484	0.8	(5)	(5)

(5) Pending characterization.

Non-Solder-Mask Defined Guidelines

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better "grip" area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball. This size allows you to use a trace between pads while meeting clearance requirements.

Figure 23: Routing Traces between Pads on the Top Layer

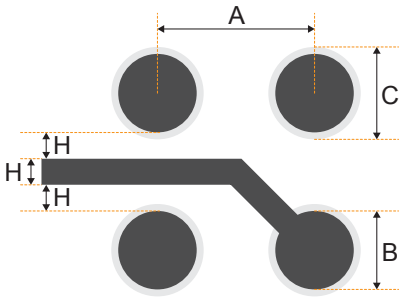


Table 11: Routing Measurements

Measurement	Description	Ball Count				Unit
		W64	F100	F225	F484	
A	Ball pitch.	0.4	0.5	0.65	0.8	mm
	Ball ϕ.	0.2	0.25	0.35	(6)	mm
B	Width of the solder landing pad ϕ.	0.2	0.25	0.35	(6)	mm
C	Width of the solder mask opening ϕ.	0.3	0.35	0.45	(6)	mm
H (min.)	Minimum space between the trace and the landing pad.	(7)	0.08	0.08	(6)	mm

(6) Pending characterization.
(7) The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an “offset via,” is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 24: Via Dimensions

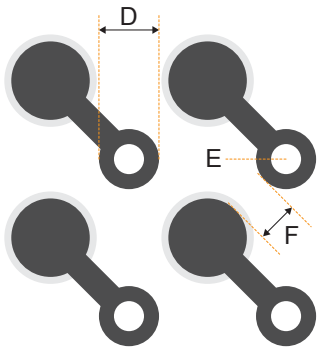


Table 12: Via Measurements

Measurement	Description	Ball Count				Unit
		W64	F100	F225	F484	
D	Via capture pad width.	0.25	0.25	0.4	(8)	mm
E	Finished via ϕ.	0.127	0.127(9)	0.2	(8)	mm
F (min.)	Space between the landing pad and via.	(10)	0.072	0.122	(8)	mm

(8) Pending characterization.
(9) This is a laser via.
(10) The via is under the pad, no traces between landing pads.

Routing Guidelines

You can route a trace between two solder pads, which allows you to route the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 25: BGA Trace Routing for Top and Second Layers

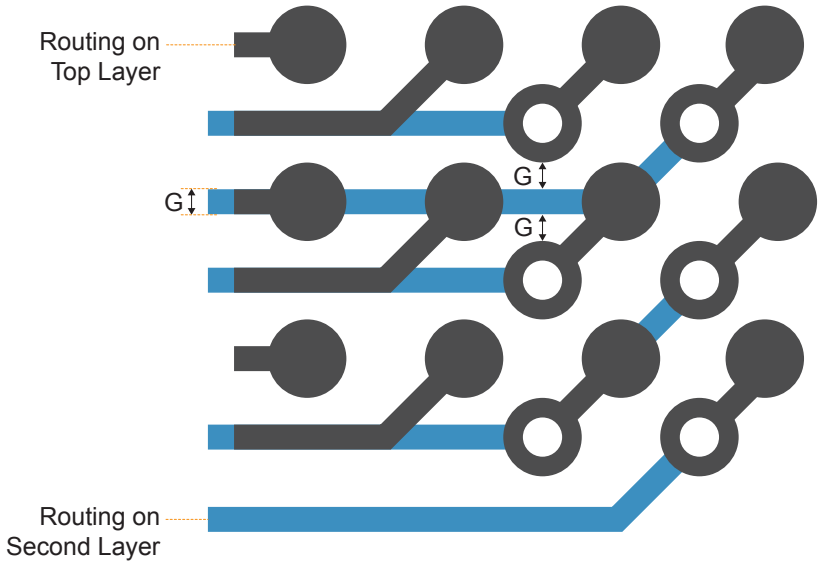


Table 13: Routing Measurements

Measurement	Description	Ball Count				Unit
		W64	F100	F225	F484	
G (min.)	Minimum space required between via trace and spacing.	0.08	0.08	0.08	(11)	mm

(11) Pending characterization.

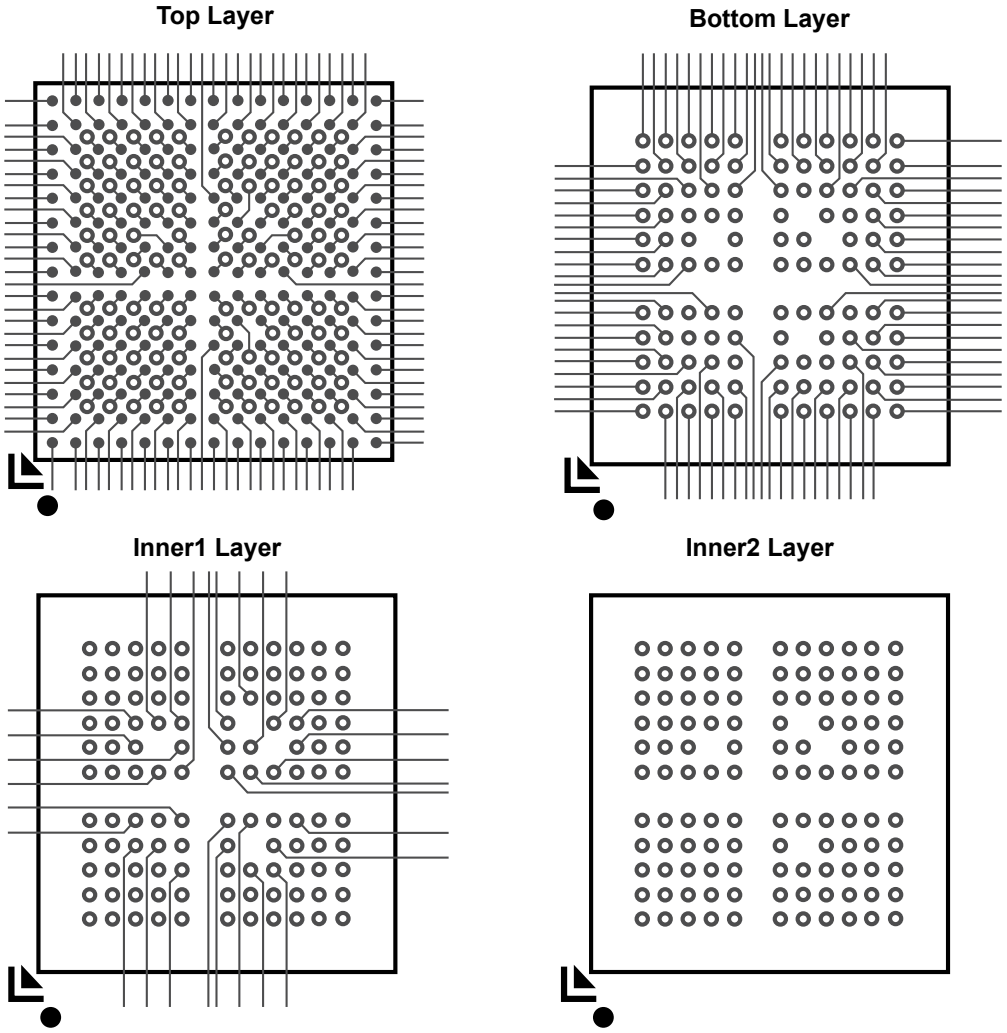
F225 Escape Routing

The following table and figure show how to perform escape routing for the F225 package. These guidelines are one example of acceptable routing using three PCB layers. You can do a different escape routing scheme with a different number of layers. The minimum number of PCB layers is four.

Table 14: 钛金系列 F225 PCB Escape Routing Parameter

Parameter	Specification	Unit
Width of the solder landing pad ϕ	0.35	mm
Width of the solder mask opening ϕ	0.45	mm
Trace width	0.08	mm
Clearance	0.08	mm
Via capture pad width	0.4	mm
Via drill diameter	0.2	mm

Figure 26: 4-Layer 钛金系列 F225 PCB Escape Routing Diagram



Green Packaging

易灵思 FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. 易灵思 refers to these products as "green" packaging.

Tape and Reel Packaging

易灵思 offers WLCSP devices in tape and reel packaging.

Table 15: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
WLCSP64	12	9.5	8	13	2,500

Figure 27: Pin 1 Location (WLCSP64 Packages)

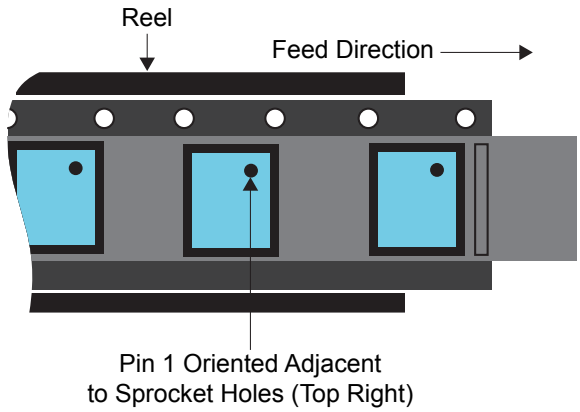
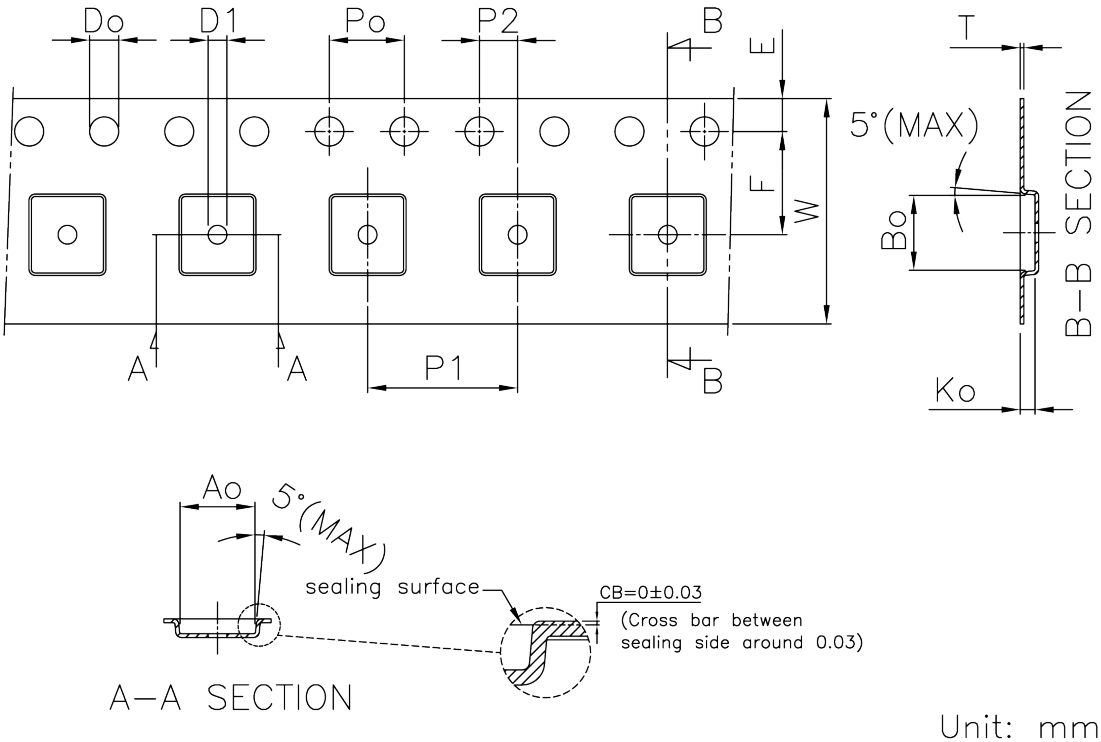


Figure 28: Tape Outline (WLCSP64 Packages)



Unit: mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.59±0.05	3.75±0.05	0.67±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	$1.50^{+0.10}_{-0}$	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity ≥ $1.0*10^5$ & ≤$1.0*10^8$ ohm/sq.
7. Tooling type : Male tooling.

Tray Packaging

易灵思 offers BGA devices in tray packaging.

Table 16: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Quantity per Stack
FBGA100	490	14 x 35	10 + 1	4,900
FBGA225	168	8 x 21	10 + 1	1,680

Revision History

Table 17: Revision History

Date	Version	Description
February 2022	2.0	Added F484 package. Updated available package options table.
December 2021	1.2	Updated PCB Solder Pad Recommendations, Routing Measurements, and added PCB Routing Example. (DOC-649) Updated A7 pin name in 64-Ball WLCSP diagrams.
September 2021	1.1	Updated PCB guidelines. (DOC-504) Updated W64 package outline. (DOC-504) Updated available package options.
June 2021	1.0	Initial release.