DDR Hard Memory Controller-Reset Core User Guide

UG-DDRCTRL-v2.4
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Introduction

Resetting a DDR block involves more than a simple reset; you also need to reconfigure the block and re-initialize the memory. The DDR Hard Memory Controller-Reset core manages this process for you. The DDR Hard Memory Controller-Reset core resets and re-initializes the Trion FPGA's DDR interface as well as the DDR module(s). You use this soft logic reset when you want to reset the DDR system while the FPGA is in user mode.

Use the IP Manager to select IP, customize it, and generate files. The DDR Hard Memory Controller-Reset core has an interactive wizard to help you set parameters. The wizard also has options to create a testbench and/or example design targeting an 易灵思® development board.

Features

- Resets the DDR controller and PHY and external memory
- Re-initializes the external memory
- Verilog RTL and simulation testbench

FPGA Support

The DDR Hard Memory Controller-Reset core supports Trion T20 (BGA324 and BGA400 packages only), T35, T55, T85, and T120 FPGAs.

Resource Utilization and Performance

Note: The resources and performance values provided are just guidance and change depending on the device resource utilization, design congestion, and user design.

Trion Resource Utilization and Performance

FPGA	Logic Utilizations (LUTs)	Registers	Memory Blocks	Multipliers	f_{MAX} (MHz)[1]	Efinity® Version[2]
T20 BGA256 C4	34	26	0	0	234	2021.1

(1) Using default parameter settings.
(2) Using Verilog HDL.

Functional Description

The DDR interface block has three input pins for reset control:

- Master reset (active low)
- Sequencer reset (active high)
- Sequencer start (active high)

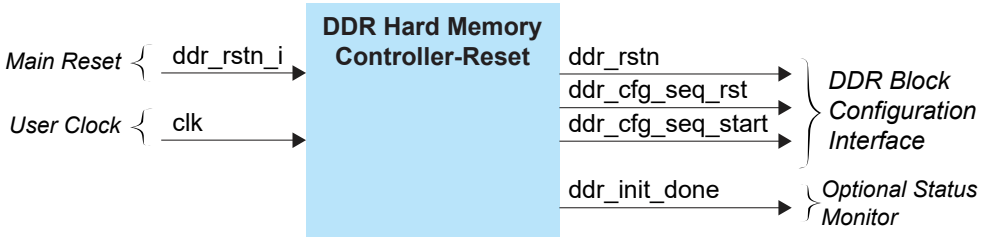
Note: These reset pins are not available if you are using I^2C calibration.

You provide a single reset signal and a clock to the DDR Hard Memory Controller-Reset core, and it generates outputs that drive these reset pins. Optionally, the code generates a status signal. Your system can monitor the status to know when the reset and DDR re-initialization completes and that read/write operations to the DDR AXI interfaces can resume.

The core contains one parameter, `FREQ`, which should correspond to the `clk` signal's frequency.

Note: You do not need to reset the DDR block when the FPGA configures or when the FPGA initially goes into user mode. The DDR reset and initialization is triggered automatically during configuration.

Figure 1: DDR Hard Memory Controller-Reset Core Block Diagram



Ports

Table 1: DDR Hard Memory Controller-Reset Core Ports

Port	Direction	Description
ddr_rstn_i	Input	Master asynchronous reset.
clk	Input	User clock.
ddr_rstn	Output	Active-low master DDR reset. Requires re-configuration and initialization after de-assertion. Connect to DDR interface block.
ddr_cfg_seq_rst	Output	Active-high DDR configuration controller reset. Connect to DDR interface block.
ddr_cfg_seq_start	Output	Start the DDR configuration controller. Connect to DDR interface block.
dr_init_done	Output	Optional status monitor for user logic. Goes high when reconfiguration and re-initialization is complete.

IP Manager

The Efinity® IP Manager is an interactive wizard that helps you customize and generate 易灵思® IP cores. The IP Manager performs validation checks on the parameters you set to ensure that your selections are valid. When you generate the IP core, you can optionally generate an example design targeting an 易灵思 development board and/or a testbench. This wizard is helpful in situations in which you use several IP cores, multiple instances of an IP core with different parameters, or the same IP core for different projects.

Note: Not all 易灵思 IP cores include an example design or a testbench.

Generating a Core with the IP Manager

The following steps explain how to customize an IP core with the IP Configuration wizard.

1. Open the IP Catalog.
2. Choose an IP core and click **Next**. The **IP Configuration** wizard opens.
3. Enter the module name in the **Module Name** box.

   Note: You cannot generate the core without a module name.
4. Customize the IP core using the options shown in the wizard. For detailed information on the options, refer to the IP core's user guide or on-line help.
5. (Optional) In the **Deliverables** tab, specify whether to generate an IP core example design targeting an 易灵思® development board and/or testbench. For SoCs, you can also optionally generate embedded software example code. These options are turned on by default.
6. (Optional) In the **Summary** tab, review your selections.
7. Click **Generate** to generate the IP core and other selected deliverables.
8. In the **Review configuration generation** dialog box, click **Generate**. The Console in the **Summary** tab shows the generation status.

   Note: You can disable the **Review configuration generation** dialog box by turning off the **Show Confirmation Box** option in the wizard.
9. When generation finishes, the wizard displays the **Generation Success** dialog box. Click **OK** to close the wizard.

The wizard adds the IP to your project and displays it under **IP** in the Project pane.

Generated Files

The IP Manager generates these files and directories:

- **<module name>_define.vh**—Contains the customized parameters.
- **<module name>_tmpl.v**—Verilog HDL instantiation template.
- **<module name>_tmpl.vhd**—VHDL instantiation template.
- **<module name>.v**—IP source code.
- **settings.json**—Configuration file.
- **<kit name>_devkit**—Has generated RTL, example design, and Efinity® project targeting a specific development board.
- **Testbench**—Contains generated RTL and testbench files.

Note: Refer to the IP Manager chapter of the Efinity® Software User Guide for more information about the Efinity® IP Manager.

Customizing the DDR Hard Memory Controller-Reset

The core has parameters so you can customize its function. You set the parameters in the General tab of the core's IP Configuration window.

Table 2: DDR Hard Memory Controller-Reset Core Parameter

Parameter	Options	Description
Clock Frequency	50, 100	Defines the core clock frequency. Default: 50

DDR Hard Memory Controller-Reset Testbench

You can choose to generate the testbench when generating the core in the IP Manager Configuration window.

Note: You must include all **.v** files generated in the **/testbench** directory in your simulation.

易灵思 provides a simulation script for you to run the testbench quickly using the Modelsim software. To run the Modelsim testbench script, run `vsim -do modelsim.do` in a terminal application. You must have Modelsim installed in your computer to use this script.

Revision History

Table 3: Revision History

Date	Version	Description
February 2023	2.4	Added note about the resource and performance values in the resource and utilization table are for guidance only.
March 2022	2.3	Corrected ddr_rstn_i port name. (DOC-742)
October 2021	2.2	Added note to state that the f_{MAX} in Resource Utilization and Performance, and Example Design Implementation tables were based on default parameter settings.
June 2021	2.1	Added note about including all **.v** generated in testbench folder is required for simulation.
December 2020	2.0	Fixed typo; in Table 1 ddr_rst_n changed to ddr_rst_i. Updated core name to DDR Hard Memory Controller-Reset. Updated user guide for 易灵思® IP Manager which includes added IP Manager topics, updated parameters, and user guide structure.
January 2020	1.0	Initial release.