FMC DDR3 and GPIO Daughter Card User Guide

DDR3-GPIO-DC-UG-v1.0
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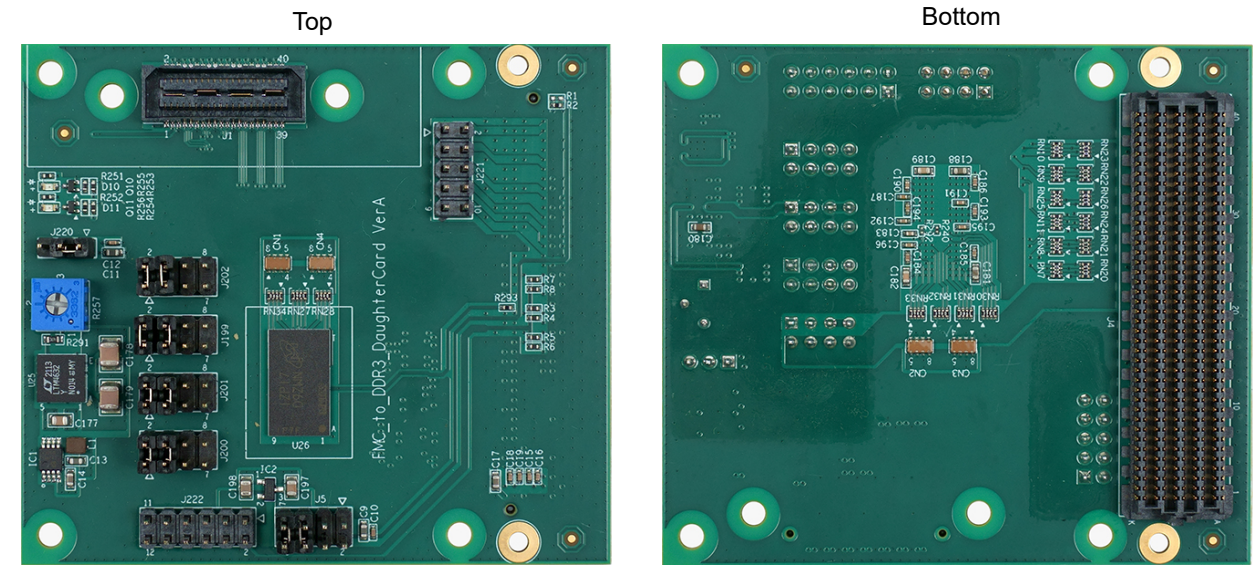
Contents

Introduction

The FMC DDR3 and GPIO Daughter Card (part number: EFX_FMC_DDR3_GPIO) has a 8Gb DDR module and also includes a QSE connector and a 10-pin header for GPIO connections. The DDR3 on the FMC DDR3 and GPIO Daughter Card , U26, is from Micron (part number: MT41K512M16).

Learn more: Refer to the FMC DDR3 and GPIO Daughter Card Schematics and BOM for the part details and schematics.

Figure 1: FMC DDR3 and GPIO Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Supported Development Boards

You can use FMC DDR3 and GPIO Daughter Card with:

- 钛金系列 Ti180 M484 Development Board

Features

- 8Gb x16 DDR3L memory
- Supports data rate of up to 800 Mbps
- QSE connector and 10-pin header for GPIO
- Power supplied from the development board; no external power required

What's in the Box?

The FMC DDR3 and GPIO Daughter Card includes:

- FMC DDR3 and GPIO Daughter Card
- 2 standoffs
- 2 screws
- 2 nuts

Installing Standoffs

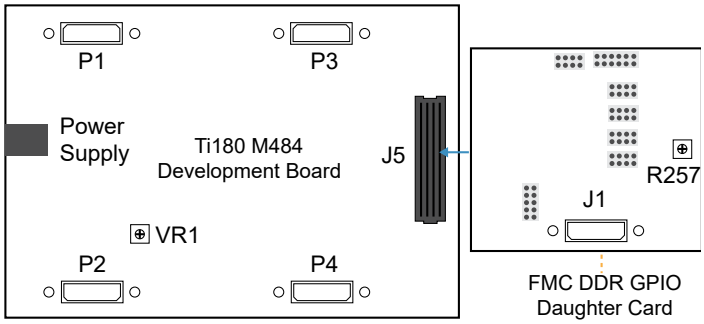
Before using the board, attach the standoffs with the screws provided in the kit.

Warning: You can damage the board if you over tighten the screws. Tighten all screws to a torque between 4 ± 0.5 kgf/cm and 5 ± 0.5 kgf/cm.

Attaching the FMC DDR3 and GPIO Daughter Card Daughter Card

The FMC DDR3 and GPIO Daughter Card attaches to the 钛金系列 Ti180 M484 Development Board. 易灵思® recommends that you also perform voltage tuning before using the FMC DDR3 and GPIO Daughter Card.

Figure 2: Attaching FMC DDR3 and GPIO Daughter Card



To connect a daughter card and tune the voltage supply:

1. Without attaching the FMC DDR3 and GPIO Daughter Card, Turn on the 钛金系列 Ti180 M484 Development Board.
2. Probe the PT4 test point and use the potentiometer VR1 to tune the voltage to 1.35 V.
3. Turn off the 钛金系列 Ti180 M484 Development Board.
4. Ensure the power supply and board power switch are turned off, then connect FMC DDR3 and GPIO Daughter Card to the 钛金系列 Ti180 M484 Development Board.
5. Turn on the 钛金系列 Ti180 M484 Development Board.
6. Probe pin 1 or 2 on the J199 header and use potentiometer R257 to tune the voltage to 1.35 V.

Headers

Table 1: FMC DDR3 and GPIO Daughter Card Headers

Reference Designator	Description
J1	40-pin multi-purpose high-speed QSE connector for GPIO
J4	FMC connector
J199, J200, J201, J202	VDD, VDDQ, VREF, and VTT supply selector
J221	10-pin header for GPIO
J222	HVIO pins (J1) pull-up selector

J1 (QSE Connector)

J1 is a multi-purpose high-speed QSE interface connector for Ti180's GPIO

Table 2: J1 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	GPIOR_P_43
3	5V_B	4	GPIOR_N_43
5	GND	6	GND
7	GPIOT_P_12_EXTFB	8	GPIOR_P_42
9	GPIOT_N_12	10	GPIOR_N_42
11	GND	12	GND
13	GPIOT_P_13_CLK16_P	14	GPIOR_P_41
15	GPIOT_N_13_CLK16_N	16	GPIOR_N_41
17	GND	18	GND
19	GPIOT_P_20_CLK23_P	20	GPIOB_P_16_EXTSPICLK_CLK3_P
21	GPIOT_N_20_CLK23_N	22	GPIOB_N_16_CLK3_N
23	GND	24	GND
25	GPIOR_P_45_PLLIN0	26	GPIOB_P_15_CLK2_P
27	GPIOR_N_45	28	GPIOB_N_15_CLK2_N
29	GND	30	GND
31	GPIOR_P_44_EXTFB	32	GPIOT_P_19_CLK22_P
33	GPIOR_N_44	34	GPIOT_N_19_CLK22_N
35	GND	36	GND
37	GPIOB_P_22_CDI11	38	GPIOB_P_17_CLK4_P
39	GPIOB_N_22_CDI10	40	GPIOB_N_17_CLK4_N

J4 (FMC Development Board Connector)

J4 is a 400-pin FMC LPC interface connector for connecting the FMC DDR3 and GPIO Daughter Card to the 钛金系列 Ti180 M484 Development Board.

J199, J200, J201, J202, J220, and J222

J199, J200, J201, J202, J220, and J222 are 8-pin headers to select voltage supplies for VDD, VDDQ, VREF, and VTT.

- VDD and VDDQ—Use power from either the on-board regulator or the 钛金系列 Ti180 M484 Development Board
- VREF and VTT—Use power from either the on-board regulator or en external power supply

Table 3: J199 (VDD) and J200 (VDDQ) Pin Assignments

Jumper	Description
Connect Pins 1 and 2 Connect Pins 3 and 4	Use on-board regulator (default)
Connect Pins 5 and 6 Connect Pins 7 and 8	Use supply from the 钛金系列 Ti180 M484 Development Board

Table 4: J201 (VREF) and J202 (VTT) Pin Assignments

Jumper	Description
Connect Pins 1 and 2 Connect Pins 3 and 4	Use on-board regulator (default)
Connect Pins 5 and 6 Connect Pins 7 and 8	Use supply from an external supply

J221 (GPIO)

J221 is a 10-pin header that is connected to the Ti180's GPIO.

Table 5: J221 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	GPIOT_P_14_CLK17_P	6	GPIOT_N_14_CLK17_N
2	GPIOT_P_15_CLK18_P	7	GPIOT_N_15_CLK18_N
3	GPIOT_P_16_CLK19_P	8	GPIOT_N_16_CLK19_N
4	GPIOT_P_17_CLK20_P	9	GPIOT_N_17_CLK20_N
5	GPIOT_P_18_CLK21_P	10	GPIOT_N_18_CLK21_N

J222

J222 is a 12-pin header to select the pull-up for HVIO pins available on header J1.

Table 6: J222 Pin Assignments

Jumper	Description
Connect Pins 1 and 2 Connect Pins 3 and 4	1.8 V pull-up (default)
Connect Pins 5 and 6 Connect Pins 7 and 8	3.3 V pull-up
Connect Pins 9 and 10 Connect Pins 11 and 12	Use pull-up value from the 钛金系列 Ti180 M484 Development Board

DDR Signal Mapping

Table 7: DDR Signal Mapping for 钛金系列 Ti180 M484 Development Board

DDR Signal	Ti180 Pin Name	DDR Signal	Ti180 Pin Name
CK			
CK	GPIOR_P_27_CLK8_P	CK#	GPIOR_N_27_CLK8_N
Address			
A0	GPIOR_N_31	A10	GPIOR_N_23_CLK12_N
A1	GPIOR_P_31_PLLIN1	A11	GPIOR_P_23_CLK12_P
A2	GPIOR_P_28	A12	GPIOR_N_22_CLK13_N
A3	GPIOR_N_28	A13	GPIOR_P_22_CLK13_P
A4	GPIOR_N_26_CLK9_N	A14	GPIOR_N_21_CLK14_N
A5	GPIOR_P_26_CLK9_P	A15	GPIOR_P_21_CLK14_P
A6	GPIOR_N_25_CLK10_N	BA0	GPIOR_P_20_CLK15_P
A7	GPIOR_P_25_CLK10_P	BA1	GPIOR_N_20_CLK15_N
A8	GPIOR_P_24_CLK11_P	BA2	GPIOR_N_19
A9	GPIOR_N_24_CLK11_N	–	–
Control			
CS#	GPIOR_N_17	WE#	GPIOR_P_19
CKE	GPIOR_P_17	ODT	GPIOR_P_16_PLLIN1
RAS#	GPIOR_P_18	RESET#	GPIOR_N_16
CAS#	GPIOR_N_18	–	–
Data			
DQ0	GPIOB_P_34	DQ8	GPIOB_P_30_CDI25
DQ1	GPIOB_N_34	DQ9	GPIOB_N_30_CDI24
DQ2	GPIOB_P_33_CDI31	DQ10	GPIOB_N_29_CDI23
DQ3	GPIOB_N_33_CDI30	DQ11	GPIOB_P_29_CDI22
DQ4	GPIOB_N_32_CDI29	DQ12	GPIOB_N_28_CDI20
DQ5	GPIOB_P_32_CDI28	DQ13	GPIOB_P_27_CDI19
DQ6	GPIOB_P_31_CDI27	DQ14	GPIOB_N_27_CDI18

DDR Signal	Ti180 Pin Name	DDR Signal	Ti180 Pin Name
DQ7	GPIOB_N_31_CDI26	DQ15	GPIOB_N_26_CDI17
DQS0	GPIOB_P_25_CDI15	DQS1	GPIOB_P_24_EXTFB
DQS0#	GPIOB_N_25_CDI14	DQS1#	GPIOB_N_24_CDI13
DM0	GPIOB_P_26_CDI16	DM1	GPIOB_N_23_CDI12

Revision History

Table 8: Revision History

Date	Version	Description
January 2023	1.0	Initial release.