钛金系列 Ti60 F225 Development Kit User Guide

Ti60F225-DK-UG-v2.1
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Contents

Introduction

Thank you for choosing the 钛金系列 Ti60 F225 Development Kit (part number: YLS_Ti60F225C-DK), which allows you to explore the features of the Ti60 FPGA.

Whether you are capturing video, aggregating sensor data, or designing for mobile or IoT applications, the 钛金系列 Ti60 F225 Development Kit provides everything you need to get started quickly. Capture video with the included Raspberry Pi camera module, process it in the Ti60 FPGA, and then stream the result to the provided mini-DSI display. The camera and DSI converter daughter cards support up to 2 cameras or displays, respectively. The kit also includes an I/O expansion daughter card so you can connect to other components more easily.

Warning: The board can be damaged without proper anti-static handling.

What's in the Box?

The 钛金系列 Ti60 F225 Development Kit includes:

- 钛金系列 Ti60 F225 Development Board
- 1 Mini-DSI Panel Connector Daughter Card
- 1 Dual MIPI to DSI Converter Daughter Card
- 1 MIPI and LVDS Expansion Daughter Card
- 1 Dual Raspberry Pi Camera Connector Daughter Card
- 1 Mini-DSI panel
- 1 Raspberry Pi v2 camera module with 15-pin flat cable
- 1 30-pin opposite-side contact flat cable
- 2 USB type-C cable
- 18 jumpers
- 10 standoffs, 10 screws, and 6 nuts
- Universal AC to DC power adapter

Register Your Kit

When you purchase an 易灵思 development kit, you also receive a license for the Efinity® software plus one year of software upgrades and patches. After the first year you can request a free maintenance renewal. The Efinity® software is available for download from the Support Center.

To download the software, first register at our Support Center (**http://www.elitestek.com/register**) and then register your development kit.

Download the Efinity® Software

To develop your own designs for the Ti60 FPGA on the board, you must install the Efinity® software. You can obtain the software from the 易灵思 Support Center under Efinity Software .

The Efinity® software includes tools to program the device on the board. Refer to the Efinity® Software User Guide for information about how to program the device.

Learn more: Efinity® documentation is installed with the software (see **Help** > **Documentation**) and is also available in the Support Center under Documentation .

Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
```

Note: If your board was connected to your computer before you executed these commands, you need to disconnect and re-connect it.

Installing the Windows USB Drivers

The 钛金系列 Ti60 F225 Development Board development board has an FTDI FT4232H chip to communicate with the USB port. This chip has separate channels that the board uses for the SPI, JTAG, and UART interfaces.

Note: If you have another 易灵思 board and are using the 钛金系列 Ti60 F225 Development Board, you must manage drivers accordingly. Refer to AN 050: Managing Windows Drivers for more information.

On Windows, you use software from Zadig to install drivers. Download the Zadig software (version 2.7 or later) from **zadig.akeo.ie**. (You do not need to install it; simply run the downloaded executable.)

Important: Install drivers for interfaces 0 and 1 only. You do not need to install drivers for interfaces 2 and 3 because when you connect the 钛金系列 Ti60 F225 Development Board to your computer, Windows automatically installs a driver for them.

To install the driver:

1. Connect the board to your computer with the appropriate cable and power it up.
2. Run the Zadig software.

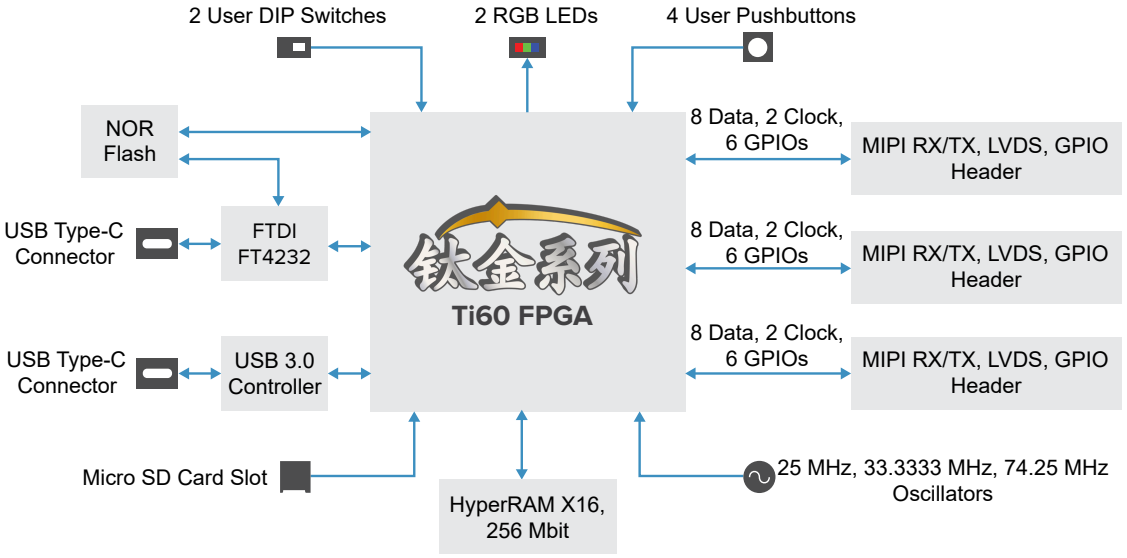
> **Note:** To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

3. Choose **Options** > **List All Devices**.
4. Repeat the following steps for each interface. The interface names end with (Interface N), where N is the channel number.
   - Select **libusb-win32** in the **Driver** drop-down list.
   - Click **Replace Driver**.
5. Close the Zadig software.

Board Functional Description

The 钛金系列 Ti60 F225 Development Board contains a variety of components to help you build designs for the 钛金系列 Ti60 device.

Figure 1: 钛金系列 Ti60 F225 Development Board Block Diagram



Features

- 易灵思 Ti60F225C4 device in an 225-ball FineLine BGA package
- HyperRAM x16 bits memory:
  - 256 Mb
  - 1.8 V power supply
  - 200 MHz maximum clock rate
  - Up to 400 Mbps double-data rate
  - Supports single ended clock (CK) and differential clock (CK/CK#)
- 64 Mbit SPI NOR flash memory
- Three MIPI, LVDS, and GPIO high-speed connectors to attach the daughter cards included in the kit or your own custom daughter cards
- Micro-SD card slot
- USB v3.0 interface and type-C connector
- USB Type-C connector for programming the flash or Ti60 FPGA using the Efinity® software
- 25, 33.3333, and 74.25 MHz oscillators for Ti60F225C4 PLL input
- User LEDs and switches:
  - 2 RGB LEDs on Ti60F225C4 banks 3B
  - 4 pushbutton switches (connected to bank 3B, TL and BR I/O pins)
  - 2 DIP switches (connected to bank 1B I/O pins)
- Power:
  - 12.0 V power supply connector
  - On-board regulator sources: 0.95 V (5A), 1.2 V (5A), 1.5 V (0.5A), 1.8 V (5A), 3.3 V (5A)
  - Fixed 1.8 V VCCIO for I/O banks 1A, 1B, 2A, and 2B
  - Fixed 3.3 V VCCIO for I/O bank BL
  - User selectable voltages from 1.8 V and 3.3 V for I/O banks TR, TL, and BR
  - User selectable voltages from 1.2 V, 1.5 V, and 1.8 V I/O banks 3A, 3B, 4A, and 4B
- Power good and Ti60F225C4 configuration done LEDs

Overview

The board features the 易灵思 Ti60 programmable device in a 225-ball FBGA package, which is fabricated using 易灵思 Quantum® technology. The Quantum®-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. Ti60 devices also include embedded memory blocks and DSP blocks. You create designs for the Ti60 device in the Efinity® software, and then download the resulting configuration bitstream to the board using the USB connection.

Learn more: For more information on Ti60 FPGAs, refer to the Ti60 Data Sheet.

Figure 2: 钛金系列 Ti60 F225 Development Board Components (Top)

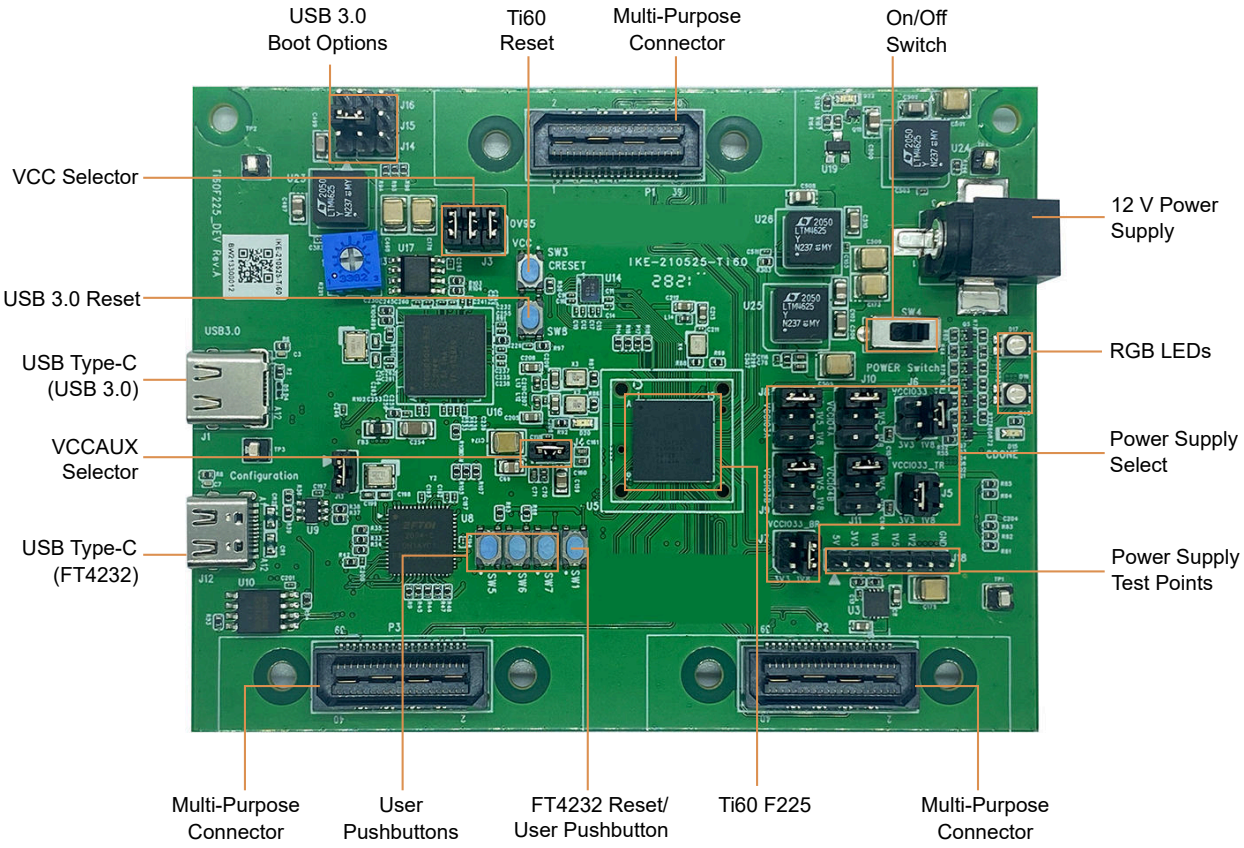


Figure 3: 钛金系列 Ti60 F225 Development Board Components (Bottom)

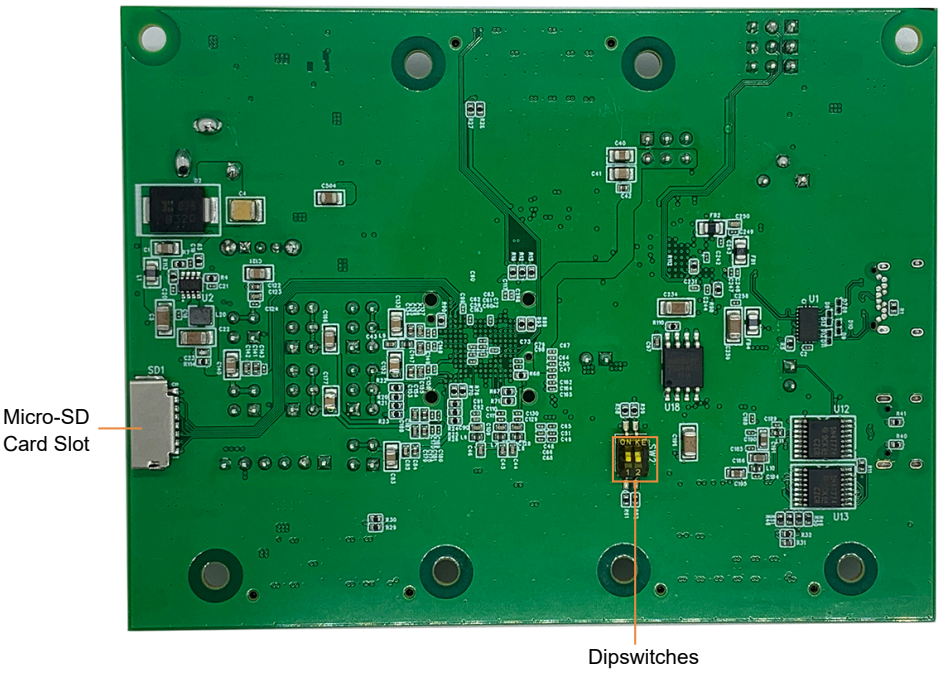
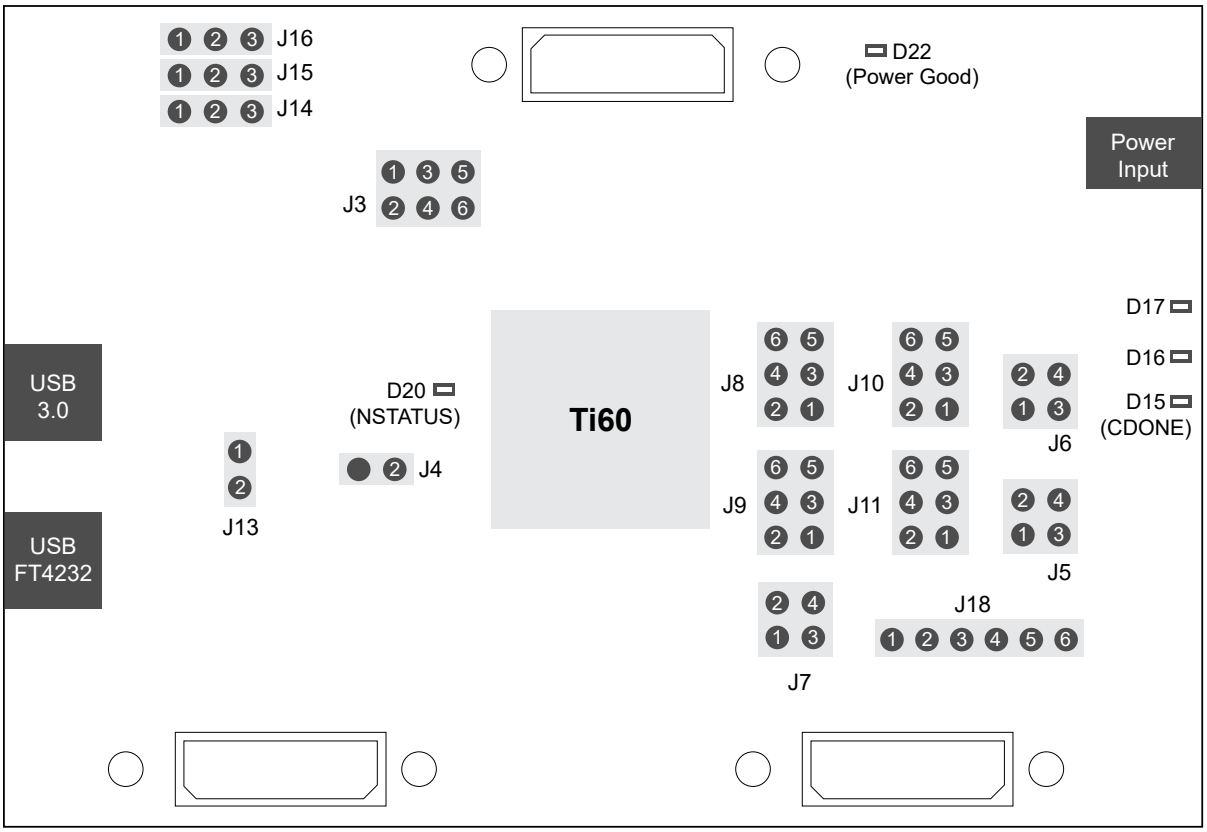


Figure 4: 钛金系列 Ti60 F225 Development Board Header and LED Definition



The 钛金系列 Ti60 F225 Development Board provides three multi-purpose 0.8 mm high-speed ground plane sockets. These sockets can be used for GPIO, MIPI CSI-2 TX/RX, and LVDS TX/RX. The board includes two USB type-C ports, one for USB 3.0 interface and the other for the FTDI interface.

The FTDI FT4232H module has four channels to support the following interfaces:

- SPI—FTDI interface 0
- FPGA JTAG—FTDI interface 1
- FPGA UART—FTDI interface 2
- USB 3.0 chip UART—FTDI interface 3

The FTDI module receives the Ti60 configuration bitstream from a USB host and writes to the Ti60 FPGA in SPI passive configuration. You can write a configuration bitstream to the on-board SPI NOR flash memory through JTAG with the JTAG SPI Flash Loader Core. Additionally, it supports a UART interface to the Ti60 and the USB 3.0 chip.

The SPI NOR flash memory stores the configuration bitstream. The Ti60 device accesses this configuration bitstream when it is in active configuration mode (default).

Learn more: Refer to the 钛金系列 Ti60 F225 Development Board Schematics and BOM for more information about the components used in the 钛金系列 Ti60 F225 Development Board.

Power On

To turn on the development board, turn on switch SW4. The 12 V DC power is input to the on-board regulators to generate the required 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.2 V for components on the board. When these voltages are up and stable, the power-good LED, D22 illuminates, giving you a visual confirmation of the status.

Reset

The Ti60F225C4 device is typically brought out of reset with the CRESET signal. Upon power up, the Ti60F225C4 device is held in reset until CRESET toggles high-low-high.

Note: You can manually assert the high-low-high transition with pushbutton switch SW3.

CRESET has a pull-up resistor. When you press SW3, the board drives CRESET low; when you release SW3, the board drives CRESET high. Thus, a single press of SW3 provides the required high-low-high transition.

After toggling CRESET, the Ti60F225C4 device goes into configuration mode and reads the device configuration bitstream from the flash memory. When configuration completes successfully, the device drives the CDONE signal high. CDONE is connected to a green LED (D15), which turns on when the Ti60F225C4 device enters user mode.

USB 3.0 Reset

You can reset the USB 3.0 module manually with the SW8 pushbutton.

Clock Sources

Three on-board oscillators (25, 33.3333, and 74.25 MHz) are available to drive the Ti60F225C4 PLL input pin and clock input.

Table 1: Oscillator and Clock Generator Sources

Clock Source	PLL Input Pin Resources	PLL
25 MHz oscillator	GPIOL_P_18_PLLIN0	PLL_TL0
33.3333 MHz oscillator	GPIOL_P_00_PLLIN0	PLL_BL0
74.25 MHz oscillator	GPIOT_P_17_PLLIN1	PLL_TR0

Configuration

The 钛金系列 Ti60 F225 Development Board has a DIP switch, SW2, to select the configuration image from the SPI flash device.

Table 2: Configuration Pins

Reference	Configuration Pin	Notes
SW2.2	CBSEL	Choose which image to load from the SPI flash device. Default: Off (both)
SW2.1		

Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 3: 钛金系列 Ti60 F225 Development Board Headers

Reference Designator	Description
P1	40-pin multi-purpose high-speed connector for MIPI TX/RX, LVDS, or GPIO
P2	40-pin multi-purpose high-speed connector for MIPI TX/RX, LVDS, or GPIO
P3	40-pin multi-purpose high-speed connector for MIPI TX/RX, LVDS, or GPIO
J1	USB type-C receptacle (USB 3.0)
J2	12 V DC power supply input jack
J3	VCC selector
J4	VCCAUX selector
J5	User selectable VCCIO for bank TR (1.8 V and 3.3 V)
J6	User selectable VCCIO for bank TL (1.8 V and 3.3 V)
J7	User selectable VCCIO for bank BR (1.8 V and 3.3 V)
J8	User selectable VCCIO for bank 3A (1.2 V, 1.5 V, and 1.8 V)
J9	User selectable VCCIO for bank 3B (1.2 V, 1.5 V, and 1.8 V)
J10	User selectable VCCIO for bank 4A (1.2 V, 1.5 V, and 1.8 V)
J11	User selectable VCCIO for bank 4B (1.2 V, 1.5 V, and 1.8 V)
J12	USB type-C receptacle (FTDI FT4232)
J13	SPI flash voltage leveler enable jumper
J14 – J16	USB boot-up configuration
J18	Power output
TP1 – TP5	Ground test points
SD1	Micro-SD card slot

Headers P1, P2, and P3 (Multi-Purpose)

P1, P2, and P3 are multi-purpose high-speed interface connectors for either MIPI TX/RX, LVDS, or GPIO that support 2 clock lanes and 8 data lanes. You can use these connectors to attach a Dual Raspberry Pi Camera Connector Daughter Card, Dual MIPI to DSI Converter Daughter Card, Mini-DSI Panel Connector Daughter Card, or HDMI Output Daughter Card.

Note: The GPIOs on pins 32, 34, 38, and 40 of headers P1, P2, and P3 support speed of up-to 10 MHz when used as I^2C interface.

Table 4: P1 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	GPIOR_P_11_CLK8_P
3	5V	4	GPIOR_N_11_CLK8_N
5	GND	6	GND
7	GPIOR_P_15	8	GPIOR_P_12
9	GPIOR_N_15	10	GPIOR_N_12
11	GND	12	GND
13	GPIOR_P_16	14	GPIOR_P_10_CLK9_P
15	GPIOR_N_16	16	GPIOR_N_10_CLK9_N
17	GND	18	GND
19	GPIOR_P_17	20	GPIOR_P_13
21	GPIOR_N_17	22	GPIOR_N_13
23	GND	24	GND
25	GPIOR_P_18	26	GPIOR_P_14
27	GPIOR_N_18	28	GPIOR_N_14
29	GND	30	GND
31	GPIOR_P_19_PLLIN0	32	GPIOR_21
33	GPIOR_N_19	34	GPIOR_22
35	GND	36	GND
37	GPIOL_P_05	38	GPIOL_09
39	GPIOL_N_05	40	GPIOL_10

Table 5: P2 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	GPIOB_P_12_CDI12
3	5V	4	GPIOB_N_12_CDI13
5	GND	6	GND
7	GPIOR_P_00_PLLIN0	8	GPIOB_P_13_CDI14
9	GPIOR_N_00_CDI22	10	GPIOB_N_13_CDI15
11	GND	12	GND
13	GPIOR_P_01_EXTFB	14	GPIOB_P_14_CDI16
15	GPIOR_N_01_CDI23	16	GPIOB_N_14_CDI17
17	GND	18	GND
19	GPIOR_P_02_CDI24	20	GPIOB_P_15_CDI18
21	GPIOR_N_02_CDI25	22	GPIOB_N_15_CDI19
23	GND	24	GND
25	GPIOR_P_03_CDI26	26	GPIOB_P_17_PLLIN1
27	GPIOR_N_03_CDI27	28	GPIOB_N_17
29	GND	30	GND
31	GPIOR_P_04_CDI28	32	GPIOR_24
33	GPIOR_N_04_CDI29	34	GPIOR_25
35	GND	36	GND
37	GPIOL_P_04_CDI2	38	GPIOR_27
39	GPIOL_N_04_CDI3	40	GPIOR_28

Table 6: P3 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	3V3	2	GPIOB_P_00_PLLIN1
3	5V	4	GPIOB_N_00
5	GND	6	GND
7	GPIOB_P_06_CDI8	8	GPIOB_P_01_EXTFB
9	GPIOB_N_06_CDI9	10	GPIOB_N_01
11	GND	12	GND
13	GPIOB_P_07_CLK15_P	14	GPIOB_P_03_CDI6
15	GPIOB_N_07_CLK15_N	16	GPIOB_N_03_CDI7
17	GND	18	GND
19	GPIOB_P_09_CLK13_P	20	GPIOB_P_02_CDI4
21	GPIOB_N_09_CLK13_N	22	GPIOB_N_02_CDI5
23	GND	24	GND
25	GPIOB_P_08_CLK14_P	26	GPIOB_P_04_SSU_N
27	GPIOB_N_08_CLK14_N	28	GPIOB_N_04
29	GND	30	GND
31	GPIOB_P_10_CLK12_P	32	GPIOL_03
33	GPIOB_N_10_CLK12_N	34	GPIOL_04
35	GND	36	GND
37	GPIOT_P_16_EXTFB	38	GPIOL_06
39	GPIOT_N_16	40	GPIOL_07

Header J1 (USB 3.0)

J1, a type-C-USB type C receptacle, is the interface between the board and your computer for communication that supports USB 3.0. You can set the boot options for the USB 3.0 interface on the 钛金系列 Ti60 F225 Development Board. See **Headers J14, J15, and J16 (USB 3.0 Boot Option)** on page 15 for information about USB 3.0 boot options.

Header J2 (Power Supply)

J2 is a 12 V DC power supply input jack. J2 supplies power to regulators on the board that power the Ti60. The maximum current supply to this input jack is 10 A.

Header J3 (VCC Selector)

J3 is a 6-pin header used to select the voltage supply for VCC to use an internal or external supply. By default, the jumper connects pin 1 and 2, which is the 0.95 V internal supply. You can disconnect the jumper, and connect an external source to pins 2, 4, or 6. This header is also useful when you want to evaluate the power draw of the 钛金系列 Ti60 F225 Development Board.

Important: The 钛金系列 Ti60 F225 Development Board includes a potentiometer to tune the internal VCC supply to 0.95 V. 易灵思 recommends that you do not change the potentiometer setting. If tuning is required, remove the J3 jumper before tuning the potentiometer to obtain the 0.95 V supply.

Header J4 (VCCAUX Selector)

J3 is a 2-pin header used to select the voltage supply for VCCAUX to use an internal or external supply. By default, the jumper connects pin 1 and 2, which is the 1.8 V internal supply. You can disconnect the jumper, and connect an external source to pin 2. This header is also useful when you want to evaluate the power draw of the board.

Headers J5, J6, and J7 (TR, TL, and BR Voltage)

J4, J5, and J6 are a 4-pin headers used to select the voltage supply for bank TR, TL, and BR. By default, the jumpers connect pins 3 and 4, which is 1.8 V. Connect the jumpers as shown in the following table to change the voltages.

Table 7: Voltage Selection for Banks TR, TL, and BR

Jumper	TR (J5)	TL (J6)	BR (J7)
Connect pins 1 and 2	3.3 V	3.3 V	3.3 V
Connect pins 3 and 4	1.8 V (default)	1.8 V (default)	1.8 V (default)

Headers J8, J9, J10, and J11 (3A, 3B, 4A, and 4B Voltage)

J8, J9, J10, and J11 are 6-pin headers used to select the voltage supply for banks 3A, 3B, 4A, and 4B. By default, the jumpers connect pins 1 and 2, which is 1.8 V. Connect the jumpers as shown in the following table to change the voltages.

Table 8: Voltage Selection for Banks 3A, 3B, 4A, and 4B

Jumper	3A (J8)	3B (J9)	4A (J10)	4B (J11)
Connect pins 1 and 2	1.8 V (default)	1.8 V (default)	1.8 V (default)	1.8 V (default)
Connect pins 3 and 4	1.5 V	1.5 V	1.5 V	1.5 V
Connect pins 5 and 6	1.2 V	1.2 V	1.2 V	1.2 V

Header J12 (USB FTDI FT4232)

J12, a type-C USB receptacle, is the interface between the board and your computer for communication through the FTDI FT4232 chip. Connect the type-C USB cable for configuring Ti60F225C4 the FPGA and NOR flash. The board supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode.

Header J13 (SPI Flash Voltage Leveler)

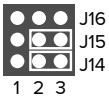
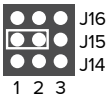
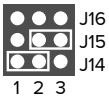
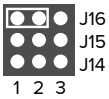
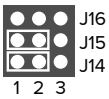
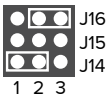
J13 is a 2 pin jumper used to enable the SPI flash voltage leveler, U12. By default, the jumper is connected. You may want to disconnect the jumper when troubleshooting configuration errors.

Headers J14, J15, and J16 (USB 3.0 Boot Option)

J14, J15, and J16 are 3-pin jumpers for selecting the USB 3.0 interface boot options. These jumpers are used together when selecting the boot options.

Connect the jumpers as shown in the following table to change the USB 3.0 interface boot options. Press pushbutton SW8 to reset the USB 3.0 controller each time after you change the jumper settings.

Table 9: Boot Options for USB 3.0 Interface

Boot Option	Jumper Setting	Boot Option	Jumper Setting
Sync ADMux (16-bit)		I^2C, On Failure, USB Boot Enabled	
Async ADMux (16-bit)		I^2C only	
USB Boot		SPI, On Failure, USB Boot Enabled	

Header J18 (Supply Test Points)

J18 is a 6-pin header connected to the available 钛金系列 Ti60 F225 Development Board power supplies. Connect to the following pins to evaluate the corresponding power supply.

Table 10: J18 Pin Assignments

Pin Number	Voltage
1	5 V
2	3.3 V
3	1.8 V
4	1.5 V
5	1.2 V

Test Points TP1, TP2, TP3, TP4 (Ground)

Test points TP1, TP2, TP3, TP4 are test points connected to ground. You can use any of the test points to get a ground reference on the 钛金系列 Ti60 F225 Development Board.

SD1 (Micro-SD Card Slot)

The 钛金系列 Ti60 F225 Development Board includes a micro-SD card slot, SD1. SD1 connects to GPIO pins in bank TR. The micro-SD supports data rate of up-to 25 MB/s.

Table 11: SD1

Pin Name	Signal Name	Ti60F225C4 Pin Name
T1	DAT2	GPIOR_20
T2	CD/DAT3	GPIOR_13
T3	CMD	GPIOR_16
T4	VDD	–
T5	CLK	GPIOR_15
T6	GND	–
T7	DAT0	GPIOR_18
T8	DAT1	GPIOR_19
9	GND	–
10	GND	–

User Outputs

The board has 2 RGB user LEDs that are connected to I/O pins in Ti60F225C4 banks 3B. By default, the Ti60F225C4 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.

Note: When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

Table 12: User Outputs

Reference Designator	Schematic Name	LED Colour	Ti60F225C4 Pin Name	Active
D16	USER_LED0	Blue	GPIOR_P_07	High
		Red	GPIOR_P_09_CLK10_P	High
		Green	GPIOR_P_08_CLK11_P	High
D17	USER_LED1	Blue	GPIOR_N_07	High
		Red	GPIOR_N_09_CLK10_N	High
		Green	GPIOR_N_08_CLK11_N	High

User Inputs

The board has 4 pushbutton switches and 2 DIP switches that you can use as inputs to the Ti60F225C4 device. The Ti60F225C4 bank 1A, 1B, and 2B I/O signals connect to Ti60F225C4 pins to control the functionality. When building designs using these switches, turn on an internal pull up for these pins in the Interface Designer.

When you press the pushbutton switches the signal drives low, indicating user input. Turning the DIP switch to the on position drives the signal low.

Table 13: User Pushbuttons

Reference Designator	Schematic Name	Ti60F225C4 Pin Name	Active
SW1	USER_BTN3	GPIOR_29_PLLIN2	Low
SW5	USER_BTN0	GPIOR_P_06_CDI20	Low
SW6	USER_BTN1	GPIOR_N_06_CDI21	Low
SW7	USER_BTN2	GPIOL_11_PLLIN2	Low

Table 14: User DIP Switches

Reference Designator	Ti60F225C4 Pin Name	Active
SW2.1	GPIOL_P_13_CBSEL0	Low
SW2.2	GPIOL_N_13_CBSEL1	Low

Note: You can only use the DIP switch SW2 as user input after configuration.

USB 3.0 Controller

The board's USB 3.0 interface uses the FX3 USB controller by Cypress. The USB 3.0 controller is preloaded with a design to run with the board demonstration design. **UVC Video Output** on page 38 explains more about the design example.

Learn more: For more information about developing your own USB 3.0 controller designs with UVC, refer to the **AN75779 - How to Implement an Image Sensor Interface Using EZ-USB FX3 in a USB Video Class (UVC) Framework** provided by Cypress.

You need to use the **EZ-USB FX3 Software Development Kit (SDK)** to program the FX3 USB controller. The SDK also includes development tools for the FX3 USB controller.

To program the FX3 USB controller, you must first set the USB 3.0 boot option jumper settings to USB Boot. Then use the Control Center software included in the SDK to program the controller with a binary image (**.img**) file.

Note: When designing your board with USB 3.0, you can use PI5USB30213A instead of PI3USB302A for the USB signal mux switch (U1). The PI5USB30213A USB signal mux switch provides hardware cable orientation detection. For more information, refer to **Designing Type-C products based on EZ-USB™ FX3 and CX3** from Cypress.

Setting-up USB 3.0 Boot Option for Programming

To set up the USB 3.0 controller boot option for programming:

1. Connect the USB header J1 to a USB 3.0 port of your computer.
2. Set the jumper J14, J15, and J16 to USB Boot mode as shown in **Table 9: Boot Options for USB 3.0 Interface** on page 16.
3. Press pushbutton SW8 to reset the USB 3.0 controller
4. Open the **Device Manager** of your computer and verify that **Cypress FX3 USB Bootloader Device** is installed under the **Universal Serial Bus** controllers group.
5. If the device is not recognized, update the driver with the one included in the EZ-USB FX3 SDK. The driver can be found in **..\<EZ-USB FX3 SDK installation folder>\1.3\driver** directory.

Program the USB 3.0 Controller

You can either boot the USB 3.0 controller from I^2C EEPROM or the board's SPI flash. By default, the USB 3.0 controller boots from I^2C EEPROM. To program the I^2C EEPROM or the board's SPI flash:

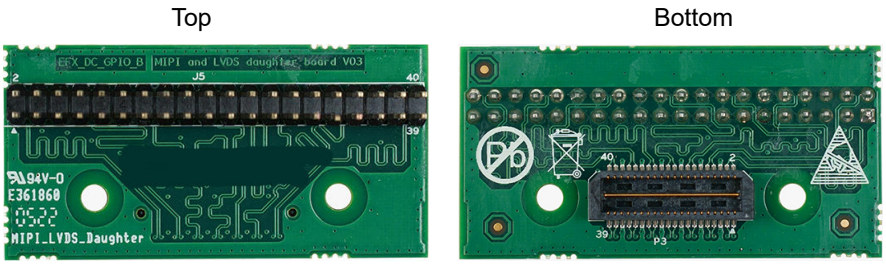
1. Open the **USB Control Center** in the Cypress SDK list.
2. Select **Cypress FX3 USB Bootloader Device** in the list.
3. Choose:
   - I^2C EEPROM—**Program** > **FX3** > **I2C EEPROM**
   - SPI flash—**Program** > **FX3** > **SPI Flash**
4. Select the binary image (**.img**) file which which you want to program to the board, then click **Open**. The software prompts `Success` when the programming is completed.
5. Set the jumper J14, J15, and J16 as shown in **Table 9: Boot Options for USB 3.0 Interface** on page 16:
   - I^2C EEPROM—I^2C, On Failure, USB Boot Enabled
   - SPI flash—SPI, On Failure, USB Boot Enabled
6. Press pushbutton SW8 to reset the USB 3.0 controller

MIPI and LVDS Expansion Daughter Card

The MIPI and LVDS Expansion Daughter Card (part number: EFX_DC_GPIO_B) converts the signals from the development board's QSE connector.

Learn more: Refer to the MIPI and LVDS Expansion Daughter Card Schematics and BOM for the part details and schematics.

Figure 5: MIPI and LVDS Expansion Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin QSE connector on the development board to a 40-pin header
- Power supplied from the development board; no external power required
  - Each pin supports up to 3 A

Headers

Table 15: MIPI and LVDS Expansion Daughter Card Headers

Reference Designator	Description
P3	40-pin QTE connector bringing MIPI or LVDS signals, power, and 1.8 V GPIO pins from the development board.
J5	40-pin header.

Headers P3 (QTE Connector) and J5 (40-Pin Header)

P3 is a 40-pin QTE connector to connect the daughter card to the QSE connector on the development board. J5 is a 40-pin header.

Table 16: P3 and J5 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO_H01	User I/O	2	GPIO_H02	User I/O
3	GPIO_H03	User I/O	4	GPIO_H04	User I/O
5	GND	Ground	6	GND	Ground
7	GPIO_H07	User I/O	8	GPIO_H08	User I/O
9	GPIO_H09	User I/O	10	GPIO_H10	User I/O
11	GND	Ground	12	GND	Ground
13	GPIO_H13	User I/O	14	GPIO_H14	User I/O
15	GPIO_H15	User I/O	16	GPIO_H16	User I/O
17	GND	Ground	18	GND	Ground
19	GPIO_H19	User I/O	20	GPIO_H20	User I/O
21	GPIO_H21	User I/O	22	GPIO_H22	User I/O
23	GND	Ground	24	GND	Ground
25	GPIO_H25	User I/O	26	GPIO_H26	User I/O
27	GPIO_H27	User I/O	28	GPIO_H28	User I/O
29	GND	Ground	30	GND	Ground
31	GPIO_H31	User I/O	32	GPIO_H32	User I/O
33	GPIO_H33	User I/O	34	GPIO_H34	User I/O
35	GND	Ground	36	GND	Ground
37	GPIO_H37	User I/O	38	GPIO_H38	User I/O
39	GPIO_H39	User I/O	40	GPIO_H40	User I/O

Signal Mapping

LVDS and MIPI Signal Mapping

This table shows the pin mapping from the multi-purpose headers (P1, P2 and P3) to the daughter card headers.

Note: The multi-purpose headers support LVDS and MIPI signals of up to 1.0 Gbps.

Table 17: LVDS Signal Mapping

Pin #	Daughter Card Pin	P1 Pin	P2 Pin	P3 Pin
1	GPIO_H01	3V3	3V3	3V3
2	GPIO_H02	GPIOR_P_11_CLK8_P	GPIOB_P_12_CDI12	GPIOB_P_00_PLLIN1
3	GPIO_H03	5V	5V	5V
4	GPIO_H04	GPIOR_N_11_CLK8_N	GPIOB_N_12_CDI13	GPIOB_N_00
5	GND	GND	GND	GND
6	GND	GND	GND	GND
7	GPIO_H07	GPIOR_P_15	GPIOR_P_00_PLLIN0	GPIOB_P_06_CDI8
8	GPIO_H08	GPIOR_P_12	GPIOB_P_13_CDI14	GPIOB_P_01_EXTFB
9	GPIO_H09	GPIOR_N_15	GPIOR_N_00_CDI22	GPIOB_N_06_CDI9
10	GPIO_H10	GPIOR_N_12	GPIOB_N_13_CDI15	GPIOB_N_01
11	GND	GND	GND	GND
12	GND	GND	GND	GND
13	GPIO_H13	GPIOR_P_16	GPIOR_P_01_EXTFB	GPIOB_P_07_CLK15_P
14	GPIO_H14	GPIOR_P_10_CLK9_P	GPIOB_P_14_CDI16	GPIOB_P_03_CDI6
15	GPIO_H15	GPIOR_N_16	GPIOR_N_01_CDI23	GPIOB_N_07_CLK15_N
16	GPIO_H16	GPIOR_N_10_CLK9_N	GPIOB_N_14_CDI17	GPIOB_N_03_CDI
17	GND	GND	GND	GND
18	GND	GND	GND	GND
19	GPIO_H19	GPIOR_P_17	GPIOR_P_02_CDI24	GPIOB_P_09_CLK13_P
20	GPIO_H20	GPIOR_P_13	GPIOB_P_15_CDI18	GPIOB_P_02_CDI4
21	GPIO_H21	GPIOR_N_17	GPIOR_N_02_CDI25	GPIOB_N_09_CLK13_N
22	GPIO_H22	GPIOR_N_13	GPIOB_N_15_CDI19	GPIOB_N_02_CDI5
23	GND	GND	GND	GND
24	GND	GND	GND	GND
25	GPIO_H25	GPIOR_P_18	GPIOR_P_03_CDI26	GPIOB_P_08_CLK14_P
26	GPIO_H26	GPIOR_P_14	GPIOB_P_17_PLLIN1	GPIOB_P_04_SSU_N
27	GPIO_H27	GPIOR_N_18	GPIOR_N_03_CDI27	GPIOB_N_08_CLK14_N
28	GPIO_H28	GPIOR_N_14	GPIOB_N_17	GPIOB_N_04
29	GND	GND	GND	GND
30	GND	GND	GND	GND
31	GPIO_H31	GPIOR_P_19_PLLIN0	GPIOR_P_04_CDI28	GPIOB_P_10_CLK12_P
32	GPIO_H32	GPIOR_21	GPIOR_24	GPIOL_03
33	GPIO_H33	GPIOR_N_19	GPIOR_N_04_CDI29	GPIOB_N_10_CLK12_N
34	GPIO_H34	GPIOR_22	GPIOR_25	GPIOL_04
35	GND	GND	GND	GND

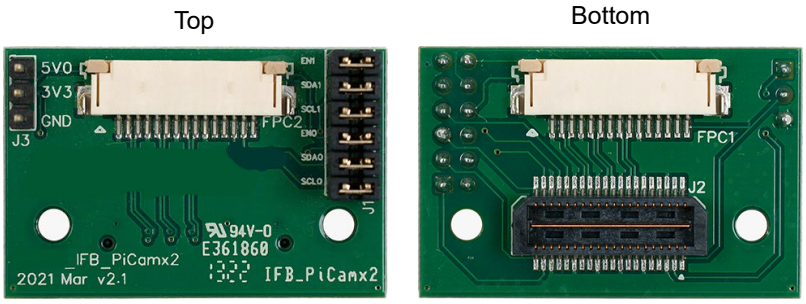
Pin #	Daughter Card Pin	P1 Pin	P2 Pin	P3 Pin
36	GND	GND	GND	GND
37	GPIO_H37	GPIOL_P_05	GPIOL_P_04_CDI2	GPIOT_P_16_EXTFB
38	GPIO_H38	GPIOL_09	GPIOR_27	GPIOL_06
39	GPIO_H39	GPIOL_N_05	GPIOL_N_04_CDI3	GPIOT_N_16
40	GPIO_H40	GPIOL_10	GPIOR_28	GPIOL_07

Dual Raspberry Pi Camera Connector Daughter Card

The Dual Raspberry Pi Camera Connector Daughter Card (part number: EFINIX_IFB_PICAMX2) bridges between the development board and two Raspberry Pi v2 camera modules. You can connect two Raspberry Pi cameras using the 15-pin flat cable to headers FPC1 (bottom) and FPC2 (top). Additionally, the board has a 12-pin header for optional camera control pins.

Learn more: Refer to the Dual Raspberry Pi Camera Connector Daughter Card Schematics and BOM for the part details and schematics.

Figure 6: Dual Raspberry Pi Camera Connector Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin MIPI CSI-2 interface on the development board to two 15-pin interfaces
- Pin to pin compatible with Raspberry Pi v2 camera modules
- Supports up to 1.5 Gbps on MIPI interface
- User selectable pins for optional camera functions
- Power supplied from the development board; no external power required

Note: For technical support using Raspberry Pi v2 camera modules, please refer to their web site at www.raspberrypi.org.

Headers

Table 18: Dual Raspberry Pi Camera Connector Daughter Card Headers

Reference Designator	Description
FPC1	15-pin flexible printed cable (FPC) receptacle for Raspberry Pi camera v2 camera modules
FPC2	15-pin flexible printed cable (FPC) receptacle for Raspberry Pi camera v2 camera modules
J1	12-pin header for optional camera signals
J2	40-pin QTE connector bringing MIPI signals, and power from the development board.
J3	3-pin header for supply test points

Headers FPC1 and FPC2 (Raspberry Pi v2 Camera Module Connector)

FPC1 and FPC2 are 15-pin flexible flat cable headers for connecting to Raspberry Pi v2 camera modules.

Table 19: FPC1 and FPC2 Pin Assignments

Pin Number	Pin Name		Description
	FPC1	FPC2	
1	GND	GND	Ground
2	DN0_1	DN0_0	Differential MIPI lane 0
3	DP0_1	DP0_0	
4	GND	GND	Ground
5	DN1_1	DN1_0	Differential MIPI lane 1
6	DP1_1	DP1_0	
7	GND	GND	Ground
8	CN0_1	CN0_0	MIPI clock lane
9	CP0_1	CP0_0	
10	GND	GND	Ground
11	CAM_EN_1	CAM_EN_0	Camera enable/reset
12	N.C.	N.C.	No connect
13	CAM_SCL_1	CAM_SCL_0	I^2C control
14	CAM_SDA_1	CAM_SDA_0	I^2C control
15	3V3	3V3	3.3 V power supply

Header J1 (Optional Camera Signals)

J1 is a 12-pin header that has optional pins (SCL and SDA) used for MIPI Camera Command Set (CSS) transactions. These signals are routed to the FPGA on the board. You can control these pins with an external device by removing the jumpers and connecting wires from the header to an external device. The header controls the settings for both cameras, but each camera has the dedicated pins shown in the following table.

Table 20: J1 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	SCL_0	I^2C signal for FPC2	2	CAM_SCL_0	I^2C signal for FPC2
3	SDA_0	I^2C signal for FPC2	4	CAM_SDA_0	I^2C signal for FPC2
5	EN_0	Camera GPIO for FPC2	6	CAM_EN_0	Camera GPIO for FPC2
7	SCL_1	I^2C signal for FPC1	8	CAM_SCL_1	I^2C signal for FPC1
9	SDA_1	I^2C signal for FPC1	10	CAM_SDA_1	I^2C signal for FPC1
11	EN_1	Camera GPIO for FPC1	12	CAM_EN_1	Camera GPIO for FPC1

Header J2 (QTE Connector)

J2 is a 40-pin QTE connector to connect the daughter card to the QSE connector on the development board.

Table 21: J2 Pin Assignments

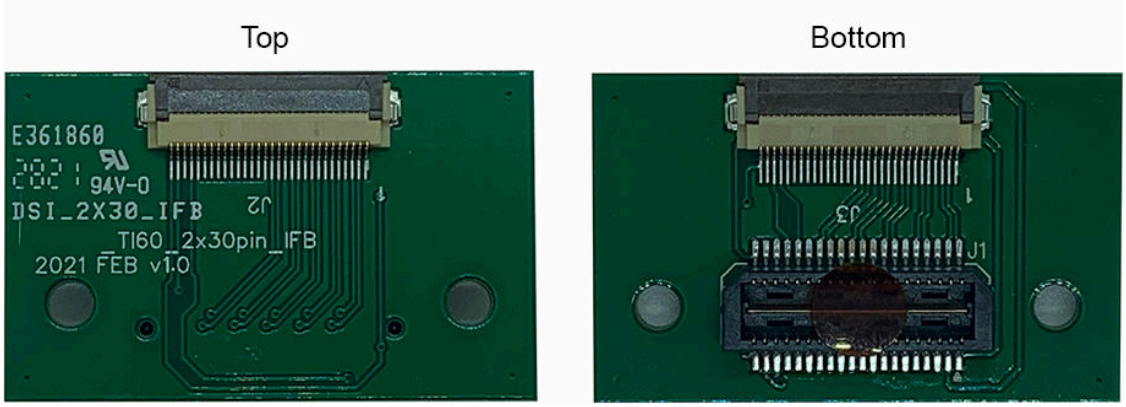
Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	3V3	3.3 V supply	2	N.C.	No connect
3	5V0	5.0 V supply	4	N.C.	No connect
5	GND	Ground	6	GND	Ground
7	DP0_0	Differential MIPI lane 0 for FPC2	8	N.C.	No connect
9	DN0_0	Differential MIPI lane 0 for FPC2	10	N.C.	No connect
11	GND	Ground	12	GND	Ground
13	DP1_0	Differential MIPI lane 1 for FPC2	14	CP0_1	MIPI clock lane for FPC1
15	DN1_0	Differential MIPI lane 1 for FPC2	16	CN0_1	MIPI clock lane for FPC1
17	GND	Ground	18	GND	Ground
19	CP0_0	MIPI clock lane for FPC2	20	DP1_1	Differential MIPI lane 1 for FPC1
21	CN0_0	MIPI clock lane for FPC2	22	DN1_1	Differential MIPI lane 1 for FPC1
23	GND	Ground	24	GND	Ground
25	N.C.	No connect	26	DP0_1	Differential MIPI lane 0 for FPC1
27	N.C.	No connect	28	DN0_1	Differential MIPI lane 0 for FPC1
29	GND	Ground	30	GND	Ground
31	N.C.	No connect	32	SCL_1	I^2C control pin for FPC1
33	N.C.	No connect	34	SDA_1	I^2C control pin for FPC1
35	GND	Ground	36	GND	Ground
37	SCL_0	I^2C control pin for FPC2	38	EN_1	Camera enable/reset for FPC1
39	SDA_0	I^2C control pin for FPC2	40	EN_0	Camera enable/reset for FPC2

Dual MIPI to DSI Converter Daughter Card

The Dual MIPI to DSI Converter Daughter Card (part number: EFINIX_TI60_2X30_IFB) converts the MIPI signals from the development board to a DSI interface for the Mini-DSI Panel Connector Daughter Card.

Learn more: Refer to the Dual MIPI to DSI Converter Daughter Card Schematics and BOM for the part details and schematics.

Figure 7: Dual MIPI to DSI Converter Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin QSE connector on 钛金系列 Ti60 F225 Development Board to two 30-pin FPC receptacles for Mini-DSI Panel Connector Daughter Card
- Power supplied from the 钛金系列 Ti60 F225 Development Board; no external power required

Headers

Table 22: Dual MIPI to DSI Converter Daughter Card Headers

Reference Designator	Description
J1	40-pin QTE connector bringing MIPI signals, and power from the development board.
J2	30-pin flexible printed cable (FPC) receptacle for Mini-DSI Panel Connector Daughter Card
J3	30-pin flexible printed cable (FPC) receptacle for Mini-DSI Panel Connector Daughter Card

Header J1 (Development Board Connector)

J1 is a 40-pin QTE connector to connect the daughter card to one of the development board's MIPI connectors.

Table 23: J1 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	3V3	3.3 V supply	2	DP0_1	Differential MIPI lane 0 for J3
3	5V0	5.0V supply	4	DN0_1	Differential MIPI lane 0 for J3
5	GND	Ground	6	GND	Ground
7	DP3_0	Differential MIPI lane 3 for J2	8	DP1_1	Differential MIPI lane 1 for J3
9	DN3_0	Differential MIPI lane 3 for J2	10	DN1_1	Differential MIPI lane 1 for J3
11	GND	Ground	12	GND	Ground
13	DP2_0	Differential MIPI lane 2 for J2	14	CP0_1	MIPI clock lane for J3
15	DN2_0	Differential MIPI lane 2 for J2	16	CN0_1	MIPI clock lane for J3
17	GND	Ground	18	GND	Ground
19	CP0_0	MIPI clock lane for J2	20	DP2_1	Differential MIPI lane 2 for J3
21	CN0_0	MIPI clock lane for J2	22	DN2_1	Differential MIPI lane 2 for J3
23	GND	Ground	24	GND	Ground
25	DP1_0	Differential MIPI lane 1 for J2	26	DP3_1	Differential MIPI lane 3 for J3
27	DN1_0	Differential MIPI lane 1 for J2	28	DN3_1	Differential MIPI lane 3 for J3
29	GND	Ground	30	GND	Ground
31	DP0_0	Differential MIPI lane 0 for J2	32	SCL_1	Touch panel I^2C control for J2
33	DN0_0	Differential MIPI lane 0 for J2	34	SDA	Touch panel I^2C control
35	GND	Ground	36	GND	Ground
37	SCL_0	Touch panel I^2C control for J1	38	INT_0	Touch panel interrupt for J1
39	EN	+/-5.5 V DC/DC enable pin	40	INT_1	Touch panel interrupt for J2

Headers J2 and J3 (Mini-DSI Panel Connector Daughter Card)

J2 and J3 are 30-pin FPC receptacles for connecting to the Mini-DSI Panel Connector Daughter Card.

Table 24: J2 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GND	Ground	2	DP0_0	Differential MIPI lane 0
3	DN0_0	Differential MIPI lane 0	4	GND	Ground
5	DP1_0	Differential MIPI lane 1	6	DN1_0	Differential MIPI lane 1
7	GND	Ground	8	CP0_0	MIPI clock lane
9	CN0_0	MIPI clock lane	10	GND	Ground
11	DP2_0	Differential MIPI lane 2	12	DN2_0	Differential MIPI lane 2
13	GND	Ground	14	DP3_0	Differential MIPI lane 3
15	DN3_0	Differential MIPI lane 3	16	GND	Ground
17	N.C	No connect	18	N.C	No connect
19	3V3	3.3 V supply	20	3V3	3.3 V supply
21	N.C	No connect	22	N.C	No connect
23	5V0	5.0 V supply	24	5V0	5.0 V supply
25	N.C	No connect	26	GND	Ground
27	SCL_0	Touch panel I^2C control	28	SDA	Touch panel I^2C control
29	INT_0	Touch panel interrupt	30	EN	+/-5.5 V DC/DC enable pin

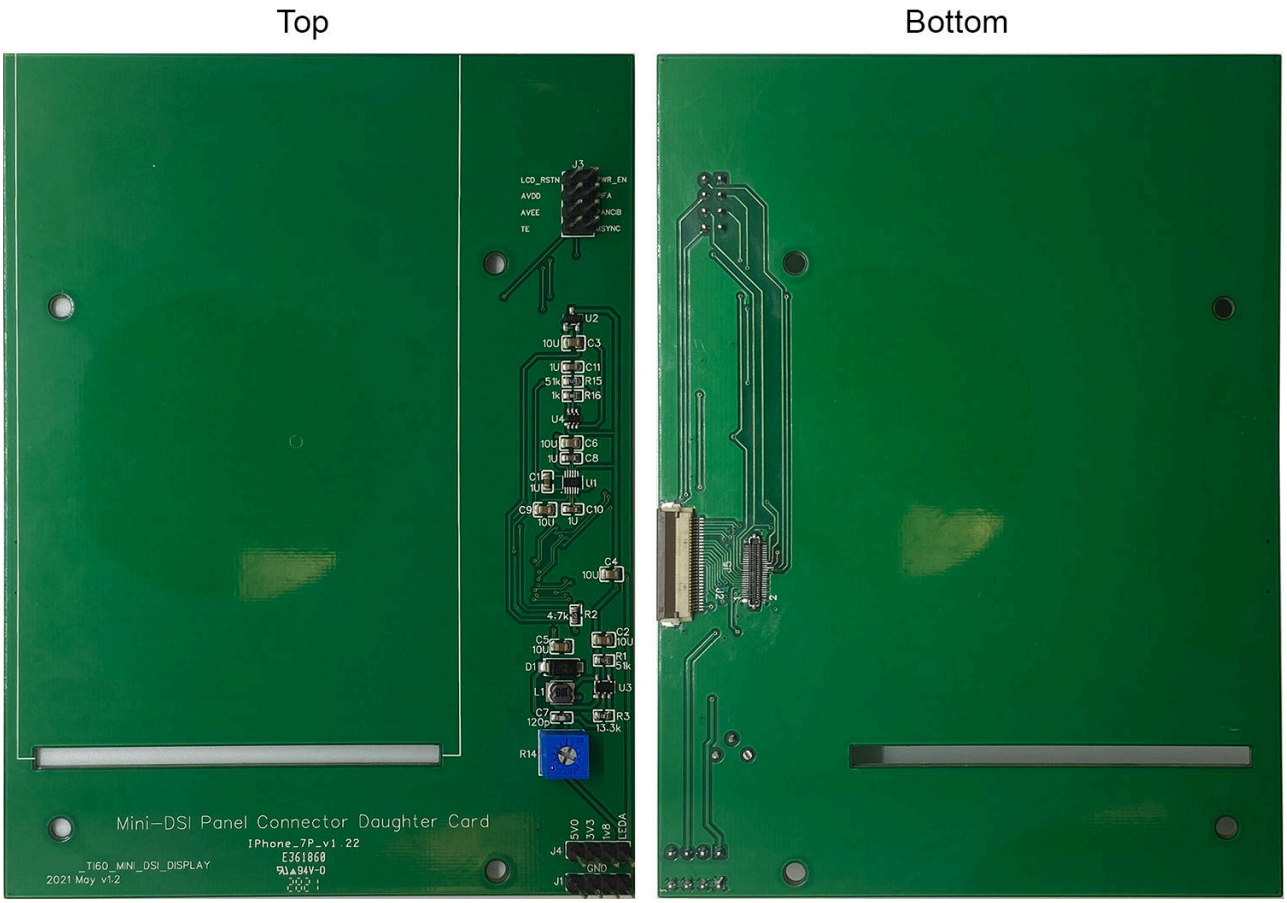
Table 25: J3 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GND	Ground	2	DP0_1	Differential MIPI lane 0
3	DN0_1	Differential MIPI lane 0	4	GND	Ground
5	DP1_1	Differential MIPI lane 1	6	DN1_1	Differential MIPI lane 1
7	GND	Ground	8	CP0_1	MIPI clock lane
9	CN0_1	MIPI clock lane	10	GND	Ground
11	DP2_1	Differential MIPI lane 2	12	DN2_1	Differential MIPI lane 2
13	GND	Ground	14	DP3_1	Differential MIPI lane 3
15	DN3_1	Differential MIPI lane 3	16	GND	Ground
17	N.C	No connect	18	N.C	No connect
19	3V3	3.3 V supply	20	3V3	3.3 V supply
21	N.C	No connect	22	N.C	No connect
23	5V0	5.0 V supply	24	5V0	5.0 V supply
25	N.C	No connect	26	GND	Ground
27	SCL_1	Touch panel I^2C control	28	SDA	Touch panel I^2C control
29	INT_1	Touch panel interrupt	30	EN	+/-5.5 V DC/DC enable pin

Mini-DSI Panel Connector Daughter Card

This daughter card connects the signals from the Dual MIPI to DSI Converter Daughter Card to the Mini-DSI panel.

Figure 8: Mini-DSI Panel Connector Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 30-pin MIPI DSI interface on Mini-DSI Panel Connector Daughter Card to a 48-pin FPC receptacle for a Mini-DSI panel
- Pin to pin compatible with Mini-DSI panel
- Power supplied from the 钛金系列 Ti60 F225 Development Board; no external power required

Headers

Table 26: Mini-DSI Panel Connector Daughter Card Headers

Reference Designator	Description
J2	30-pin flexible printed cable (FPC) receptacle for Dual MIPI to DSI Converter Daughter Card
J4	Voltage test points
J5	48-pin flexible printed cable (FPC) receptacle for Mini-DSI panel

Headers J2 (Mini-DSI Panel Connector Daughter Card)

J2 is a 30-pin FPC receptacle for connecting to the Mini-DSI Panel Connector Daughter Card.

Table 27: J2 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GND	Ground	2	DP0	Differential MIPI lane 0
3	DN0	Differential MIPI lane 0	4	GND	Ground
5	DP1	Differential MIPI lane 1	6	DN1	Differential MIPI lane 1
7	GND	Ground	8	CP0	MIPI clock lane
9	CN0	MIPI clock lane	10	GND	Ground
11	DP2	Differential MIPI lane 2	12	DN2	Differential MIPI lane 2
13	GND	Ground	14	DP3	Differential MIPI lane 3
15	DN3	Differential MIPI lane 3	16	GND	Ground
17	N.C	No connect	18	N.C	No connect
19	3V3	3.3 V supply	20	3V3	3.3 V supply
21	N.C	No connect	22	N.C	No connect
23	5V0	5.0 V supply	24	5V0	5.0 V supply
25	N.C	No connect	26	GND	Ground
27	N.C	No connect	28	N.C	No connect
29	LCD_RSTN	Display panel reset	30	N.C	No connect

Headers J4 (Test Points)

J4 is a 4-pin test points to measure the Mini-DSI panel backlight voltage.

Table 28: J4 Pin Assignments

Pin Number	Description
1	5 V supply
2	3.3 V supply
3	1.8 V supply
4	LEDA +16.5 V (Back-light positive voltage)

Header J5 (Mini-DSI Display Panel)

J5 is a 48-pin FPC receptacle for connecting the Mini-DSI display panel.

Table 29: J5 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GND	Ground	2	DN3	Differential MIPI lane 3
3	LEDA	Back-light positive voltage	4	DP3	Differential MIPI lane 3
5	GND	Ground	6	GND	Ground
7	GND	Ground	8	DN2	Differential MIPI lane 2
9	LEDA	Back-light positive voltage	10	DP2	Differential MIPI lane 2
11	GND	Ground	12	GND	Ground
13	GND	Ground	14	DN1	Differential MIPI lane 1
15	CN0	MIPI clock lane	16	DP1	Differential MIPI lane 1
17	CP0	MIPI clock lane	18	GND	Ground
19	PIFA	Panel test pin	20	DN0	Differential MIPI lane 0
21	MSYNC	Panel test pin	22	DP0	Differential MIPI lane 0
23	N.C	No connect	24	GND	Ground
25	AVEE	-5.8 V panel power	26	TE	Panel tearing effect output
27	N.C	No connect	28	LCD_RSTN	LCD_RSTN
29	N.C	No connect	30	AVDD	+5.8 V panel power
31	LCD_RSTN	Display reset	32	1V8	1.8 V supply
33	N.C	No connect	34	LCD_RSTN	LCD_RSTN
35	N.C	No connect	36	N.C	No connect
37	N.C	No connect	38	GND	Ground
39	N.C	No connect	40	N.C	No connect
41	N.C	No connect	42	N.C	No connect
43	N.C	No connect	44	N.C	No connect
45	N.C	No connect	46	N.C	No connect
47	N.C	No connect	48	N.C	No connect

Setting up the Board

Installing Standoffs

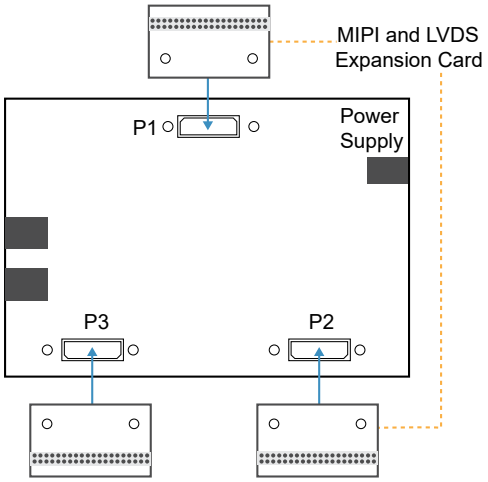
Before using the board, attach the standoffs with the screws provided in the kit.

Warning: You can damage the board if you over tighten the screws. Tighten all screws to a torque between 4 ± 0.5 kgf/cm and 5 ± 0.5 kgf/cm.

Attaching the MIPI and LVDS Expansion Daughter Card

The 钛金系列 Ti60 F225 Development Board supports an expansion daughter card that fans out the GPIO.

Figure 9: Attaching MIPI and LVDS Expansion Daughter Card



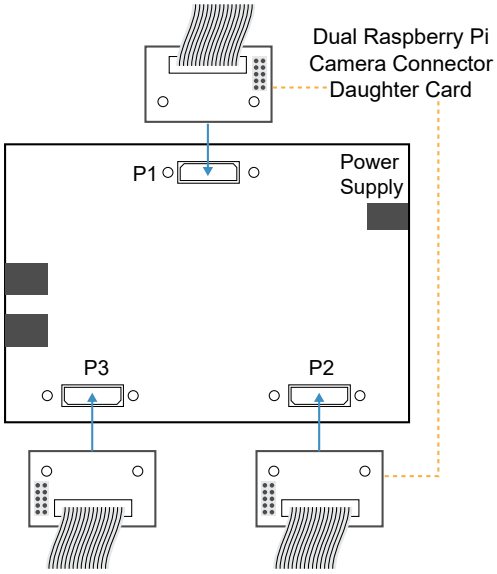
To connect the daughter card:

1. Remove power from the 钛金系列 Ti60 F225 Development Board.
2. Attach standoffs to the MIPI and LVDS Expansion Daughter Card.
3. Attach the MIPI and LVDS Expansion Daughter Card to one of the multi-purpose high-speed interface 40-pin headers on the 钛金系列 Ti60 F225 Development Board.
4. Connect any cables to the GPIO as needed for your application.
5. Power up the 钛金系列 Ti60 F225 Development Board.

Attaching the Dual Raspberry Pi Camera Connector Daughter Card

The Dual Raspberry Pi Camera Connector Daughter Card attaches to the multi-purpose high-speed interface headers.

Figure 10: Attaching Dual Raspberry Pi Camera Connector Daughter Card



Note: Headers P3 and P4 include only MIPI TX signals. No camera output signals are available in these headers. However, you still can connect the daughter card to these headers for a loop-back input setup, if required.

To connect a daughter card:

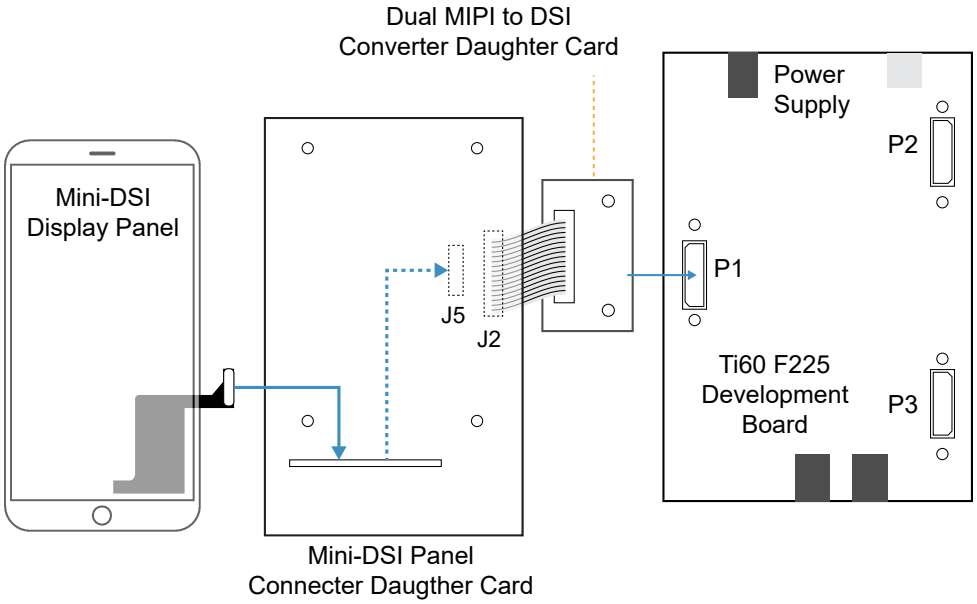
1. Remove power from the 钛金系列 Ti60 F225 Development Board.
2. Attach standoffs to the Dual Raspberry Pi Camera Connector Daughter Card.
3. Attach theDual Raspberry Pi Camera Connector Daughter Card to one of the multi-purpose high-speed interface 40-pin headers on the 钛金系列 Ti60 F225 Development Board.
4. Connect the camera module to the daughter card using a 15-pin flat cable. If you have a second camera module, connect it to the daughter card using an additional 15-pin flat cable.
5. Power up the board.

Attaching the Display and Daughter Cards

The Mini-DSI panel is connected to the 钛金系列 Ti60 F225 Development Board through the Dual MIPI to DSI Converter Daughter Card and Mini-DSI Panel Connector Daughter Card.

Important: When using the Mini-DSI Display panel for the first time, you need to verify that the panel backlight voltage is within the recommended range. Failing to comply may damage the Mini-DSI Display panel. See **Mini-DSI Panel Backlight Setup** on page 37 for steps to setup the backlight panel.

Figure 11: Attaching Display and Related Daughter Cards



Note: The following figure shows an example connection. You can connect the Dual MIPI to DSI Converter Daughter Card to any of the multi-purpose high-speed interface headers.

To connect the display and daughter cards:

1. Remove power from the 钛金系列 Ti60 F225 Development Board.
2. Attach standoffs to the daughter cards.
3. Attach the Dual MIPI to DSI Converter Daughter Card to the 40-pin header on the board.
4. Attach the Mini-DSI Panel Connector Daughter Card to the Dual MIPI to DSI Converter Daughter Card using a 30-pin flat cable.
5. Connect the Mini-DSI Display the Dual MIPI to DSI Converter Daughter Card using the attached 48-pin flat cable.
6. Power up the board.

Note: You can also attach a second Mini-DSI display to the same Dual MIPI to DSI Converter Daughter Card using an additional Mini-DSI Panel Connector Daughter Card.

Mini-DSI Panel Backlight Setup

Note: You only need to verify the backlight voltage when setting up the Mini-DSI panel for the first time.

The Mini-DSI panel backlight voltage must be within 15.5 V to 17.5 V. The Mini-DSI panel can be damaged if the backlight voltage is not within the recommended range.

Measuring and Tuning the Backlight Voltage

1. Connect the Mini-DSI Display the Dual MIPI to DSI Converter Daughter Card using the attached 48-pin flat cable.
2. Power up the board.

1. Attach standoffs to the daughter cards.
2. Remove power from the 钛金系列 Ti60 F225 Development Board.
3. Attach the Dual MIPI to DSI Converter Daughter Card to any of multi-purpose header on the 钛金系列 Ti60 F225 Development Board.
4. Attach the Mini-DSI Panel Connector Daughter Card to the Dual MIPI to DSI Converter Daughter Card using a 30-pin flat cable.

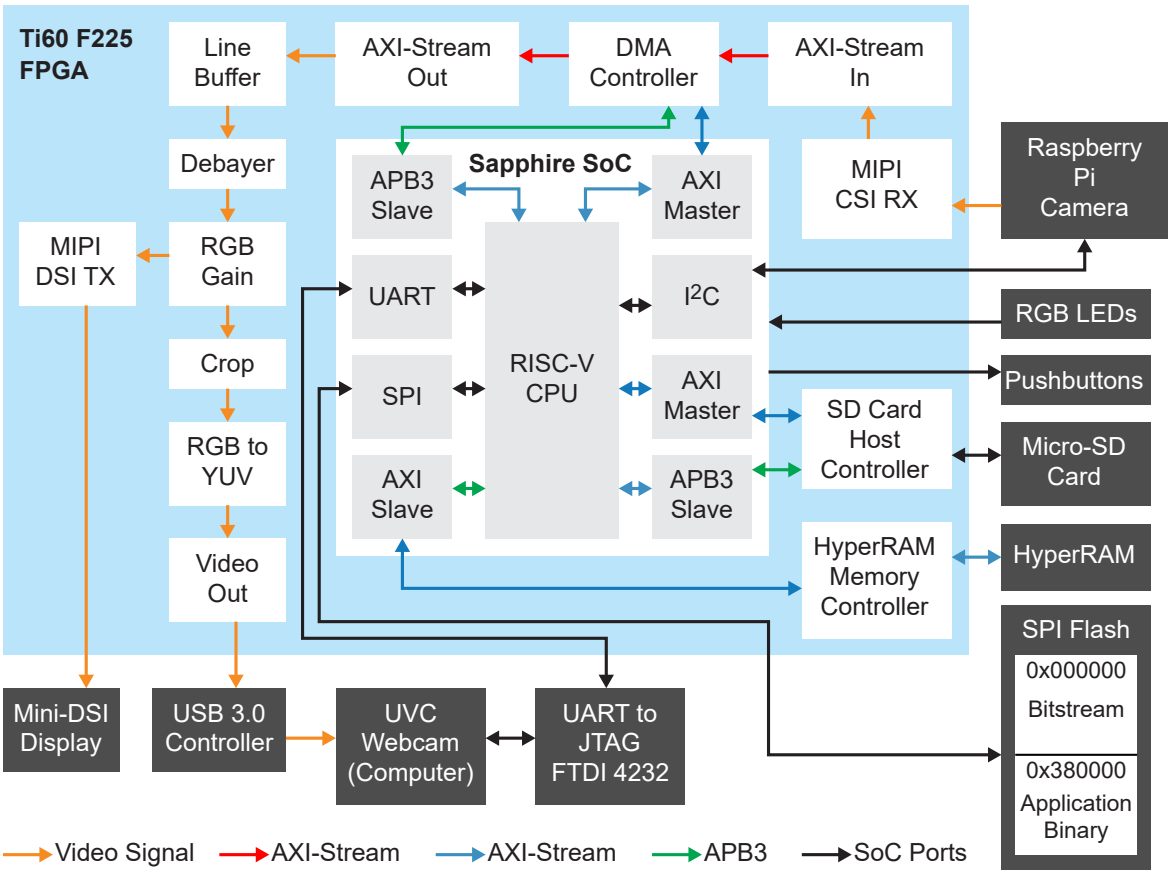
   Note: Do not connect the Mini-DSI panel.
5. Turn on the 钛金系列 Ti60 F225 Development Board.
6. On the Mini-DSI Panel Connector Daughter Card, monitor the voltage on header J4 pin 4 (LEDA).
7. If the voltage is not within 15.5 V to 17.5 V, adjust the variable resistor on the Mini-DSI Panel Connector Daughter Card, R14, until the voltage is with the range.

钛金系列 Ti60 F225 Development Board Example Design

易灵思 preloads the 钛金系列 Ti60 F225 Development Board with an example design that demonstrates the following functions:

- Mini-DSI panel video output
- USB video class (UVC) video output
- Read SD card Information

Figure 12: Example Design Block Diagram Overview



Mini-DSI Panel Video Output

The design receives video stream from the Raspberry Pi camera through a MIPI CSI RX block, then displays the video on the Mini-DSI panel through a MIPI DSI TX block. A Sapphire RISC-V SoC controls the operation flow of the design and assigns the DMA controller to stream video frame data to and from the HyperRAM.

UVC Video Output

The design streams the video to the computer through USB. The design sends video signal in YUV2 format to the USB 3.0 controller. Then the USB 3.0 controller streams it to the computer in UVC framework. The video can be displayed on standard computer camera software, for example, the Windows 10 Camera App.

Table 30: Video Stream Specifications

Item	Pixel Resolution	Frame Rate
Raspberry Pi Camera video input	1080 x 1920	30 FPS
Mini-DSI Panel Video Output	1080 x 1920	42 FPS
USB UVC Video Output (USB 3.0)	1080 x 1920	42 FPS
USB UVC Video Output (USB 2.0)	360 x 360	42 FPS

Read SD Card Information

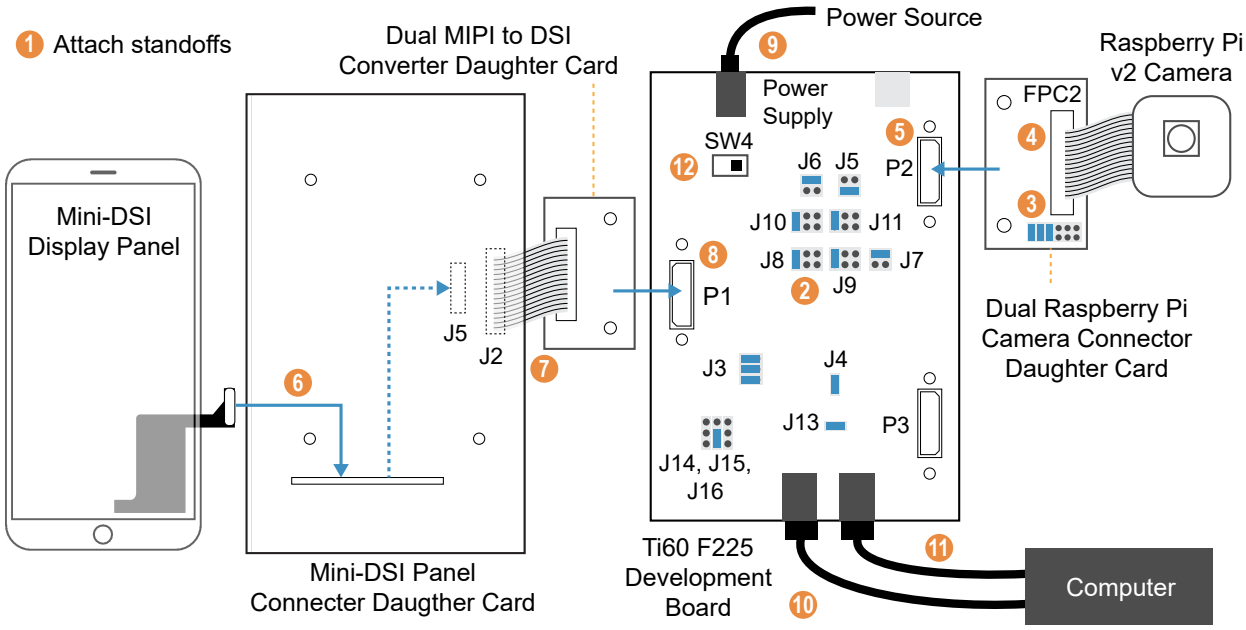
The design includes an SD host controller block that initializes the SD card and accesses the SD card information. You can retrieve the SD card information such as card size, speed and blocks using a terminal software on your computer.

Set Up the Hardware

Important: When using the Mini-DSI Display panel for the first time, you need to verify the panel backlight voltage is within the recommended range. Failing to comply may damage the Mini-DSI Display panel. See **Mini-DSI Panel Backlight Setup** on page 37 for steps to setup the backlight panel.

The following figure shows the hardware setup steps:

Figure 13: Hardware Setup



1. Attach standoffs to the board if you have not already done so.
2. On the 钛金系列 Ti60 F225 Development Board, connect the following jumpers:

Header	Net Name	State	Short Pins
J3	VCC	0.95V	1 and 2
J3	VCC	0.95V	3 and 4
J3	VCC	0.95V	5 and 6
J4	VCCAUX	1.8V	1 and 2
J5	VCCIO33_TR	3.3V	1 and 2
J6	VCCIO33_TL	1.8V	3 and 4
J7	VCCIO33_BR	1.8V	3 and 4
J8	VCCIO3A	1.2V	5 and 6
J9	VCCIO3B	1.2V	5 and 6
J10	VCCIO4A	1.2V	5 and 6
J11	VCCIO4B	1.2V	5 and 6
J13	SPI_ENA	Short	1 and 2
J14	FX3_PMODE0	Float	Unconnected
J15	FX3_PMODE1	Pull-up	1 and 2
J16	FX3_PMODE2	Float	Unconnected

3. On the Raspberry Pi Camera Connector Daughter Card, connect the following pins with jumpers: 1 - 2, 3 - 4, and 5 - 6.
4. Connect the Raspberry Pi v2 camera module to the FPC2 connector of the Raspberry Pi Camera Connector Daughter Card using the 15-pin flat cable.
5. Connect the Raspberry Pi Camera Connector Daughter Card to the P2 header of the 钛金系列 Ti60 F225 Development Board.
6. Connect the Mini-DSI Display panel to header J5 of the Mini-DSI Panel Connector Daughter Card using the attached 48-pin flat cable.

Note: Insert the Mini-DSI Display cable through the small opening to connect to header J5. The header is at the bottom of the board.

7. Connect connector J2 of Mini-DSI Panel Connector Daughter Card to connector J2 of Dual MIPI to DSI Converter Daughter Card using a flat cable.
8. Connect the Dual MIPI to DSI Converter Daughter Card to the P1 header of the 钛金系列 Ti60 F225 Development Board.
9. Ensure the board power switch is turned off, then connect the 12 V power cable to the board connector and to a power source.
10. Connect the USB header J1 to a USB 3.0 port of your computer.
11. Connect the USB header J12 to USB port of your computer.
12. Turn on the board's power switch.

After turning on the board, the board LEDs light up to indicate the following board status.

LED	Light Status	Description
D22	Green on	Power good
D15	Green on	FPGA configuration done
D20	Red on	FPGA configuration error

Running the Example Design

After the FPGA configures, you can run one of the preloaded example design functions as described in the following sections.

Mini-DSI Panel

1. When all modules are connected correctly, the Mini-DSI panel displays the video image captured from the Raspberry Pi camera after board boot-up. LED D16 lights up red if the Raspberry Pi camera is not connected.
2. Press pushbutton SW5; the Mini-DSI panel displays a color pattern.

Note: If the Raspberry Pi camera is not connected to the 钛金系列 Ti60 F225 Development Board, the Mini-DSI panel displays the same color pattern.

3. Press pushbutton SW5 again to switch back to the camera video stream.

Important: To protect the Mini-DSI panel from LCD flickering and LCD image retention, press pushbutton SW7 to turn-off the Mini-DSI panel before any of the following action:

- Turning off the board
- Loading a new design
- Pressing SW3 to reconfigure the board

USB UVC

Note: This example design function is designed to be used with the Windows 10 Camera app, and is not supported in Linux.

1. Use a USB cable to connect USB port J1 of the 钛金系列 Ti60 F225 Development Boardto a USB 3.0 port on your computer.

Note: If you connect the USB to a non-USB 3.0 port, or use USB cable that does not support USB 3.0, the video displayed is cropped to 360 x 360 pixels.

2. Open the Camera app in Windows 10.
3. If the 钛金系列 Ti60 F225 Development Board USB is connected, and the USB driver is recognized, the Camera app displays the video image captured by the Raspberry Pi camera. If more than one camera is connected to the computer, click **Switch** button on the top right corner of the Camera app to change cameras.
4. Press pushbutton SW5; the Camera app displays a color pattern.

Note: If the Raspberry Pi camera is not connected to the 钛金系列 Ti60 F225 Development Board, the Camera app displays the same color pattern.

5. Press pushbutton SW5 again to switch back to the camera video stream.

Note: If the Camera app displays an abnormal video stream, press SW8 to reset the USB 3.0 controller.

Note: If the computer detects the USB 3.0 connection only as USB 2.0, try changing the USB type-C cable orientation on the board, and reconnect it again. Then press SW8 to reset the USB 3.0 controller.

Read SD Card Information

1. Connect USB port J12 to the computer.
2. Open a terminal software on the computer. You can use any Windows or Linux terminal applications such as, PuTTy, Tera Term, Minicom, and others.
3. Select the available USB com port and set the following:
   - Baud rate: 115200
   - Data: 8-bit
   - Parity bit: No
   - Stop bit: 1
4. Insert the SD card and press pushbutton SW6. The SD card test starts.
5. If the test passed, LED D17 lights up green, and the console displays the SD Card information.

```
--- EFX-SD Card Demo---

Initialize...Loop: 0
Reponse: 0x40FF8000
Reponse: 0x40FF8000
Reponse: 0x40FF8000
Done

************START SD Card TEST************
**SD CLOCK SPEED = 50000
**CARD SPEED = 25000 kHz
**CARD SIZE = 15080 Mbyte Total BLOCK = 30883840
**SD BUS WIDTH = 4
**BLOCK SIZE = 512 BUFFER OF BLOCK = 256
**TEST SIZE - 128 kbyte
****************************************
```

6. If the test failed or there is no SD card inserted in the slot, LED D17 lights up red.

```
--- EFX-SD Card Demo---

Initialize...Loop: 0
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Loop: 1
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Reponse: 0x0
Err: ACMD41 OCR BUSY!
SD Initial Error
```

Creating Your Own Design

The 钛金系列 Ti60 F225 Development Board allows you to create and explore designs for the Ti60 FPGA. 易灵思® provides example code and designs to help you get started:

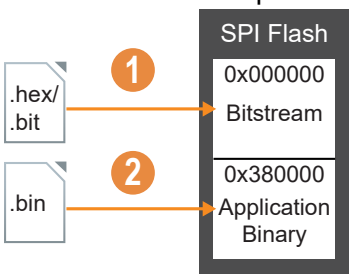
- Our Support Center includes examples targeting the board.
- The Efinity® software includes also example designs that you can use as a starting point for your own project and includes a step-by-step tutorial.

Restoring the Demonstration Design

After you have used the board for other designs, you may want to go back to the original pre-loaded example design. The preloaded example design project file is available in the Support Center.

Note: The example design available in the support center requires Efinity software v2021.2 or later.

To restore the example design, you need to:



1. Program the board's SPI flash with the Ti60 example design bitstream.
2. Copy the Sapphire RISC-V SoC application binary to the SPI flash.
3. Additionally, you may also need to program the USB 3.0 controller if you have programmed it with a different design. Refer to **USB 3.0 Controller** on page 19 for instructions on how to program the USB 3.0 controller. The example design includes a pre-compiled binary file (**TI60F225_OOB_UVC.img**) in the **../usb3/bin/** directory for you to program the USB 3.0 controller.

Program the Development Board

The example design file includes a bitstream file to get you started quickly. Download it to the board using these steps:

1. Download the file **efx_ti60f225_oob-v<version>.zip** from the Support Center.
2. Open the project (**ti60f225_oob.xml**) in the Efinity software. The project is located in the **efx_ti60f225_oob-v<version>/** directory.
3. Review the design.
4. Connect the 钛金系列 Ti60 F225 Development Board to your computer using a USB cable.
5. Use the Efinity® Programmer to download the bitstream file, **ti60f225_oob.hex**, to your board using SPI active mode. Set the **Starting Flash Address** to `0x000000`.

   Note: You use SPI active mode because you need to reset the FPGA. 易灵思 also includes the **ti60f225_oob.bit** file to be used with JTAG mode. Using JTAG mode requires you to reprogram the bitstream into the board when you reset the board.

Learn more: Instructions on how to use the Efinity® software and board documentation are available in the Support Center.

Sapphire RISC-V SoC Application Binary

You can program the user binary to the flash device using one of the following methods:
- Efinity Programmer (supported in Efinity software v2021.2 and later)
- 2 terminals method

The example design includes software files and pre-compiled binary files for the Sapphire RISC-V SoC.

Table 31: Sapphire RISC-V SoC Directories

Directory	Description
../embedded_sw/sapphire_soc	Example design Sapphire RISC-V SoC project files including Eclipse workspace directory.
../embedded_sw/sapphire_soc/software/standalone/ti60f225_oob_legacy	Example design software files to customize the software using the Legacy Eclipse IDE.
../embedded_sw/sapphire_soc/software/standalone/ti60f225_oob	Example design software files to customize the software using the Efinity RISC-V IDE.
../embedded_sw/bin	Pre-compiled application binary files for fast application deployment. • **ti60f225_oob.bin**—To program into SPI flash • **ti60f225_oob.elf**—To boot using OpenOCD debugger.

Learn more: Before working with the software included with this example design, you should already be familiar with using the Sapphire SoC and RISC-V SDK. Refer to the Sapphire RISC-V SoC Hardware and Software User Guide for more information about the Sapphire SoC.

Copy a User Binary to Flash (Efinity Programmer)

To program the user binary using the Efinity Programmer:

1. Open the Efinity Programmer.
2. Browse to the RISC-V application binary file (**EFX_HEX_ti60f225_oob.hex**) which can be found in the **../embedded_sw/bin** director, and click **Open**.
3. Select **SPI Active** from the **Programming Mode** drop-down list.
4. Specify the **Starting Flash Address** as to `0x00380000`.
5. Enable the **Erase Before Program** option.
6. Click **Start Program**.
7. Reset the FPGA or power cycle the board.

Copy a User Binary to Flash (2 Terminals)

Learn more: These instructions describe how to use a command prompt or shell to flash the **ti60f2225_oob.bin** binary file. Refer to the Debug with the OpenOCD Debugger chapter of the Sapphire RISC-V SoC Hardware and Software User Guidefor more information about booting using OpenOCD Debugger.

You use two command prompts or shells:
- The first terminal opens an OpenOCD connection to the SoC.
- The second connects to the first terminal to write to the flash.

Important: If you are using the OpenOCD debugger in Eclipse, terminate any debug processes before attempting to flash the memory.

Set Up Terminal 1

1. Open a Windows command prompt or Linux shell.
2. Change to **SDK_Windows** or **SDK_Ubuntu**.
3. Execute the **setup.bat** (Windows) or **setup.sh** (Linux) script.
4. Change to the directory that has the **cpu0.yaml** file.
5. Type the following commands to set up the OpenOCD server:

   Windows:

   ```
   openocd.exe -f bsp\efinix\EfxSapphireSoc\openocd\ftdi_ti.cfg
     -c "set CPU0_YAML cpu0.yaml"
     -f bsp\efinix\EfxSapphireSoc\openocd\flash_ti.cfg
   ```

   Linux:

   ```
   openocd -f bsp/efinix/EfxSapphireSoc/openocd/ftdi_ti.cfg
     -c "set CPU0_YAML cpu0.yaml"
     -f bsp/efinix/EfxSapphireSoc/openocd/flash_ti.cfg
   ```

   The OpenOCD server connects and begins listening on port 4444.

Set Up Terminal 2

1. Open a second command prompt or shell.
2. Enable telnet if it is not turned on. **Turn on telnet (Windows)**
3. Open a telnet local host on port 4444 with the command `telnet localhost 4444`.
4. In the OpenOCD shell or command prompt, use the following command to flash the user binary file:

   ```
   flash write_image erase unlock <path>/<ti60f2225_oob>.bin 0x380000
   ```

   Where <path> is the full, absolute path to the **.bin** file.

Note: For Windows, use \\ as the directory separators.

Close Terminals

When you finish:

- Type `exit` in terminal 2 to close the telnet session.
- Type Ctrl+C in terminal 1 to close the OpenOCD session.

Important: OpenOCD cannot be running in Eclipse when you are using it in a terminal. If you try to run both at the same time, the application will crash or hang. Always close the terminals when you are done flashing the binary.

Reset the FPGA

Press the reset button (SW3) on the development board. This reset ensures that the DDR memory initialization happens before the user application runs.

Revision History

Table 32: Revision History

Date	Version	Description
May 2023	2.1	Indicate that the flat cables included in the box are opposite-side contact. (DOC-1197) Updated micro-SD card and SD card example design description. (DOC-1280) Added note to headers P1, P2, and P3 about supported I^2C speed.
February 2023	2.0	Corrected SPI NOR flash memory to 64 Mbit. (DOC-1138) Added demonstration design directory to include new files for the Efinity RISC-V IDE. (DOC-1139)
January 2023	1.9	Updated kit part number.
November 2022	1.8	Corrected Pin 6 name in FPC1 and FPC2. (DOC-959) Added note for Installing Windows USB Drivers to link to AN050: Managing Window Drivers.
September 2022	1.7	Updated Installing Windows USB Drivers. Added note saying the multi-purpose headers support LVDS and MIPI signal of up to 1.0 Gbps with MIPI and LVDS Expansion Daughter Card.
June 2022	1.6	Corrected restoring example design figure. (DOC-794) Corrected P1 pins 37 and 39 in the LVDS and MIPI Signal Mapping for MIPI and LVDS Expansion Daughter Card.
March 2022	1.5	Added note about solving USB 3.0 detected as USB 2.0 issue. (DOC-745)
February 2022	1.4	Corrected the OpenOCD terminal setup commands. Added steps to program application binary using Efinity Programmer.
December 2021	1.3	Updated example design Set Up the Hardware steps and figure. Updated the Efinity project file directory for board demonstration design available in Support Center. Updated the Program the USB 3.0 Controller topic.
November 2021	1.2	Updated Mini-DSI Panel Connector Daughter Card J5 header pin assignments. Added USB 3.0 controller programming steps. (DOC-571) Added topics about restoring the demo example design. (DOC-571)
November 2021	1.1	Corrected the multi-purpose header signal names. Updated Mini-DSI Panel backlight setup steps.
September 2021	1.0	Initial release.