



易 灵 思

钛金系列 Packaging User Guide

UG-TI-PKG-v5.2
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Introduction

易灵思 offers 钛金系列 FPGAs in packages that are designed for the devices' maximum number of user's I/O pins. This document describes the 钛金系列 FPGAs' pin and package specifications as well as solder reflow guidelines.



- Learn more:** Refer to the following documents for more information:
 FPGA pinout specification
 FPGA data sheet for pin definitions

Available Package Options

Table 1: 钛金系列 Package Options

Package	Pitch (mm)	Size (mm)	Ti35	Ti60	Ti90	Ti120	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
64-ball WLCSP	0.4	3.5x3.4		✓								
100-ball FBGA	0.5	5.5x5.5	✓	✓								
225-ball FBGA	0.65	10x10	✓	✓	✓	✓	✓					
361-ball FBGA	0.65	13x13			✓	✓	✓					
400-ball FBGA	0.8	16x16			✓	✓	✓					
484-ball FBGA	0.65	15x15			✓	✓	✓	✓	✓			
484-ball FBGA	0.8	18x18			✓	✓	✓					
529-ball FBGA	0.8	19x19			✓	✓	✓					
625-ball FBGA	0.65	17x17						✓	✓	✓	✓	
784-ball FBGA	0.8	23x23						✓	✓	✓	✓	✓
1,156-ball FBGA	1.0	35x35								✓	✓	✓

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

Device Pinout File

易灵思 provides pinout files for 钛金系列 FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: Power and Ground Pinouts

xx indicates the bank location.

Function	Description
VCC	Core power supply.
VCCA_xx	PLL analog power supply.
VCCAUX	1.8 V auxiliary power supply.
VCCIO33_xx	HVIO bank power supply.
VCCIOxx	HSIO bank power supply.
VCCIOxx_yy_zz	Power for HSIO banks that are shorted together. xx, yy, and zz are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C
VQPS	1.8 V supply for security fuse.
GND	Ground.

Table 3: GPIO Pinouts

x indicates the location (T, B, L, or R); xx indicates the bank location; n indicates the number; yyyy indicates the function.

Function	Direction	Description
GPIOx_n	I/O	HVIO for user function. User I/O pins are single-ended.
GPIOx_n_yyyy	I/O	HVIO or multi-function pin.
GPIOx_N_n GPIOx_P_n	I/O	HSIO transmitter, receiver, or both.
GPIOx_N_n_yyyy GPIOx_P_n_yyyy	I/O	HSIO transmitter, receiver, both, or multi-function.
REF_RES_xx	-	<p>REF_RES is a reference resistor to generate constant current for the related circuits.</p> <p>Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% :</p> <ul style="list-style-type: none"> • REF_RES_2A and REF_RES_4A pins must be connected • REF_RES_2A, REF_RES_2C, REF_RES_4A, and REF_RES_4C pins must be connected • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. <p>You can leave the REF_RES pins floating if none of the above are applicable.</p>

Table 4: Alternate Function Pinouts

n is the number.

Function	Direction	Description
CLKn	Input	Single ended input for global clock and control network resource. The number of inputs is package dependent.
CLKn_P/N	Input	Differential input pair for global clock and control network resource. P pins can access to global clock and control network resource if it is in single-ended configuration.
PLLINn	Input	PLL reference clock resource. The number of reference clock resources is package dependent.

Table 5: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up During Configuration
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete. If you hold CDONE low, the device will not enter user mode.	✓
CRESET_N	Input	Initiates FPGA re-configuration (active low). Pulse CRESET_N low for a duration of t_{creset_N} before asserting CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	✓
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	✓
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

⁽¹⁾ CDONE has a drive strength of 12 mA at 1.8 V.

Table 6: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up During Configuration
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	✓ ⁽²⁾
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock.	Optional ⁽³⁾
CDIn	I/O	n is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. n: Parallel I/O. In multi-bit daisy chain connection, the CDIn (31:0) connects to the data bus in parallel.	Optional ⁽³⁾
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration (SPI and JTAG ⁽⁴⁾ configuration).	✓
CSO	Output	Chip select output. Selects the next device for cascading configuration. ⁽⁵⁾	N/A
NSTATUS	Output	Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SSL_N	Input	Active-low configuration mode select. The FPGA senses the value of SSL_N when it comes out of reset (pulse CRESET_N low to high). 0: Passive mode 1: Active mode In active configuration mode, SSL_N serves as a chip select to the flash device 1 (CDI0 - CDI3).	Optional ⁽³⁾
SSU_N	Output	In active configuration mode (dual quad mode), SSU_N serves as a chip select to the flash device 2 (CDI4 - CDI7).	Optional ⁽³⁾
EXT_CONFIG_CLK	I/O	In active mode, EXT_CONFIG_CLK pin is connected to an external clock, to be used as a configuration clock.	Optional ⁽³⁾
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓

⁽²⁾ Not applicable to single-image or remote update.

⁽³⁾ Optional unless pull-up is required by external load.

⁽⁴⁾ Chip select for JTAG mode is required for Ti35 and Ti60 FPGAs only.

⁽⁵⁾ Cascaded configuration is not supported in the F100S3F2 package.

Table 7: DDR Pinouts (Dedicated)

n indicates the number.

Function	Direction	Description
DDR_A[n]	Output	Address signals to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[n]	I/O	Data bus to/from the memories.
DDR_DM[n]	Output	Active-high data-mask signals to the memories.
DDR_DQS[n] DDR_DQS_N[n]	I/O	Differential data strobes to/from the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_CAL	Input	240 ohm to ground reference resistor port.
VDD_PHY	–	DDR digital power supply.
VDDQ_PHY	–	DDR I/O power supply.
VDDQX_PHY	–	DDR I/O pre-driver power supply.
VDDPLL_MCB_TOP_PHY	–	DDR PLL power supply.
VDDQ_CK_PHY	–	DDR I/O power supply for clock.

Table 8: Dedicated MIPI D-PHY Pinouts

m and n indicates the number. L indicates the lane

Function	Direction	Description
VCC18A_MIPIm_n_TX	–	Power supply for the MIPI D-PHY block. m and n are the MIPI channel numbers. For example: VCC18A_MIPIO_1_TX displays the power of MIPI D-PHY TX channel 0 and channel 1 being shorted together.
VCC18A_MIPIm_n_RX	–	Power supply for the MIPI D-PHY block. m and n are the MIPI interface numbers. For example: VCC18A_MIPIO_1_RX displays the power of MIPI D-PHY RX channel 0 and channel 1 being shorted together.
MIPIn_RXDPL MIPIn_RXDNL	I/O	MIPI differential transmit data lane.
MIPIn_RXDPL MIPIn_RXDNL	I/O	MIPI differential receive data lane.

64-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 64-Ball WLCSP Pinout Diagram

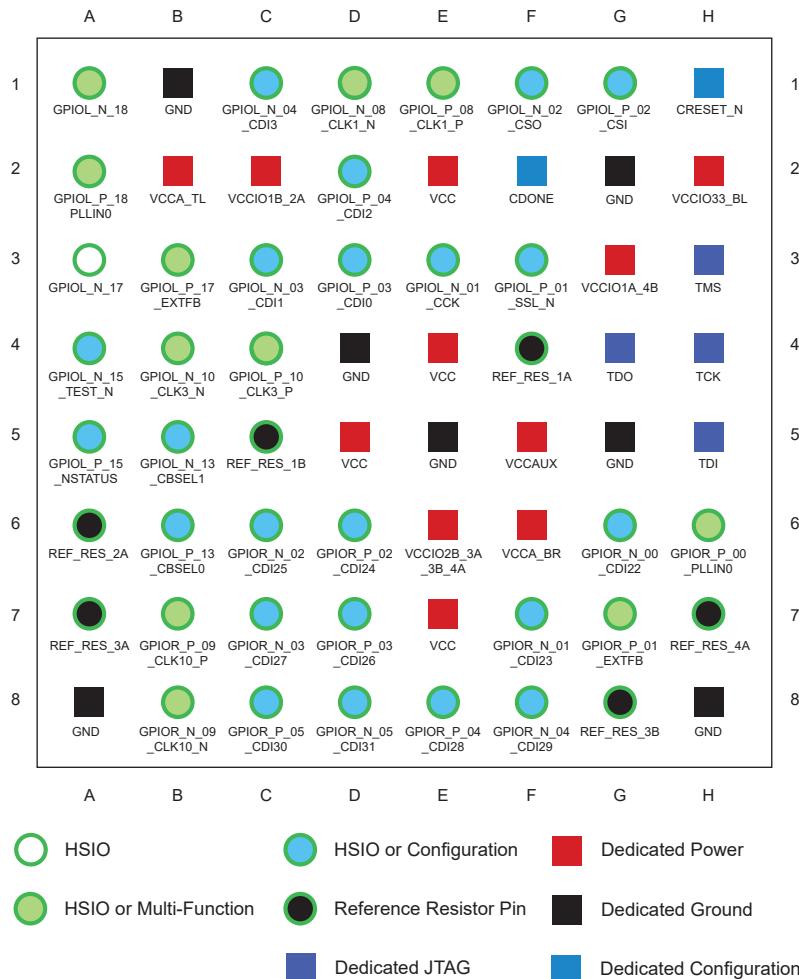


Figure 2: 64-Ball WLCSP I/O Bank Diagram

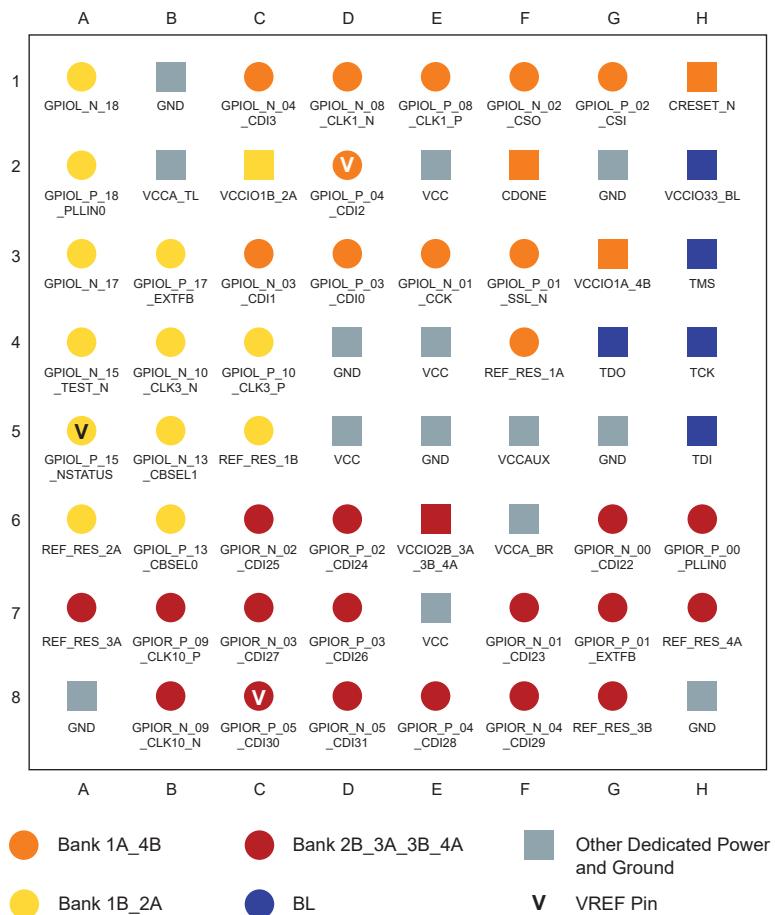


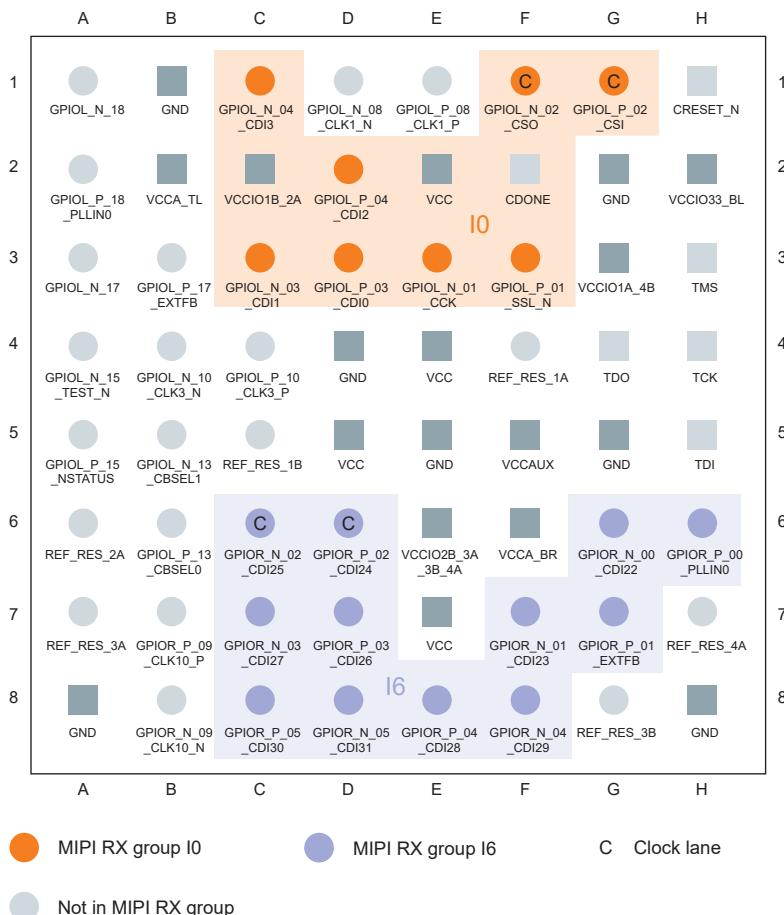
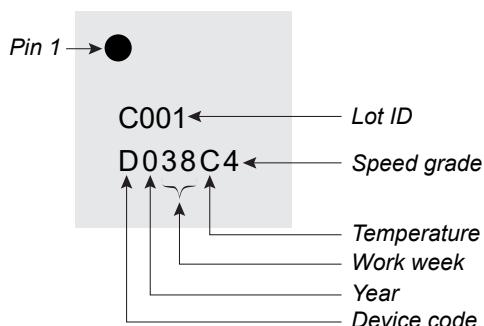
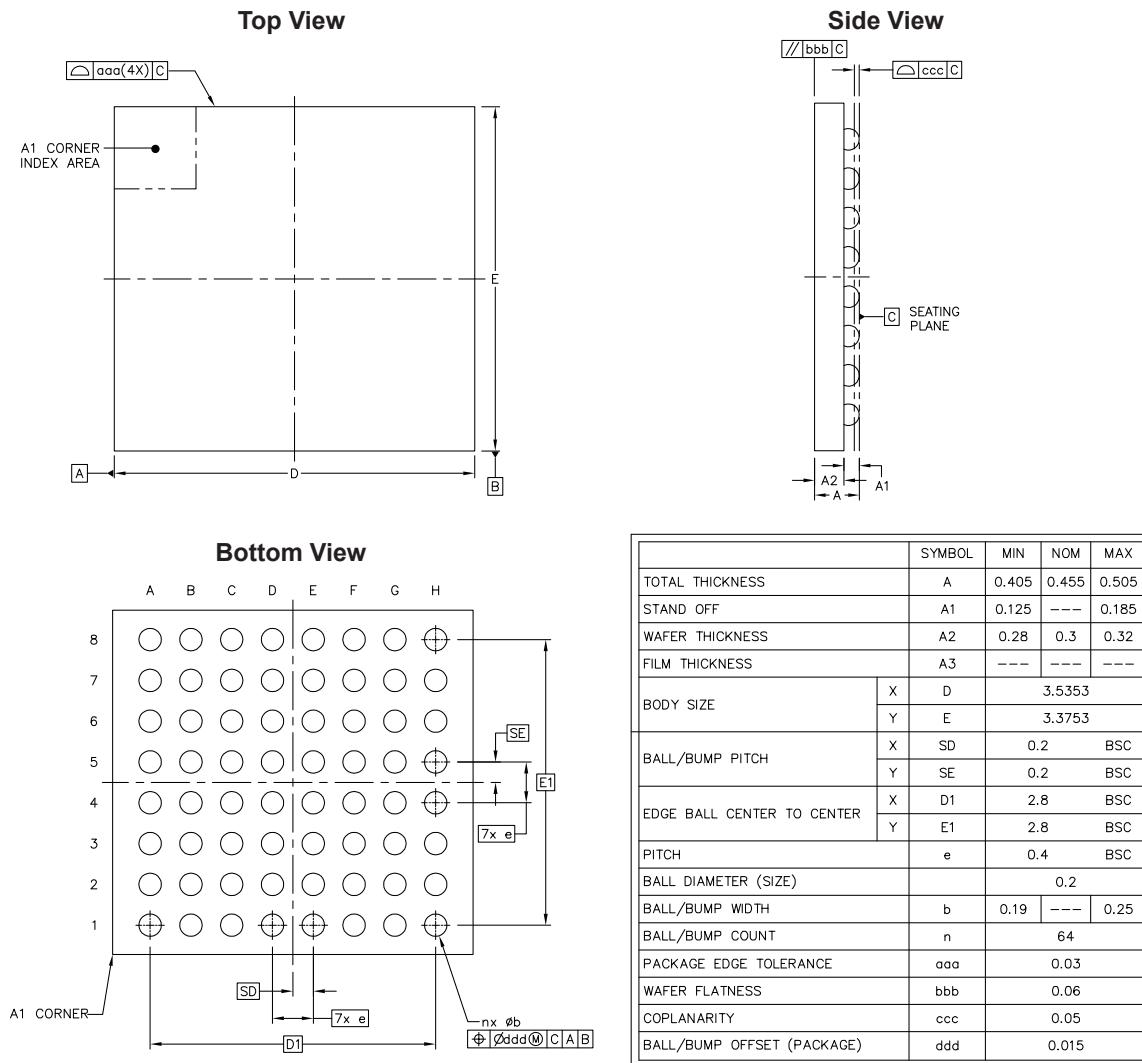
Figure 3: 64-Ball WLCSP Emulated MIPI RX Groups**Figure 4: 64-Ball WLCSP Package Marking**

Figure 5: 64-Ball WLCSP Package Outline



100-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 6: 100-Ball FBGA Pinout Diagram

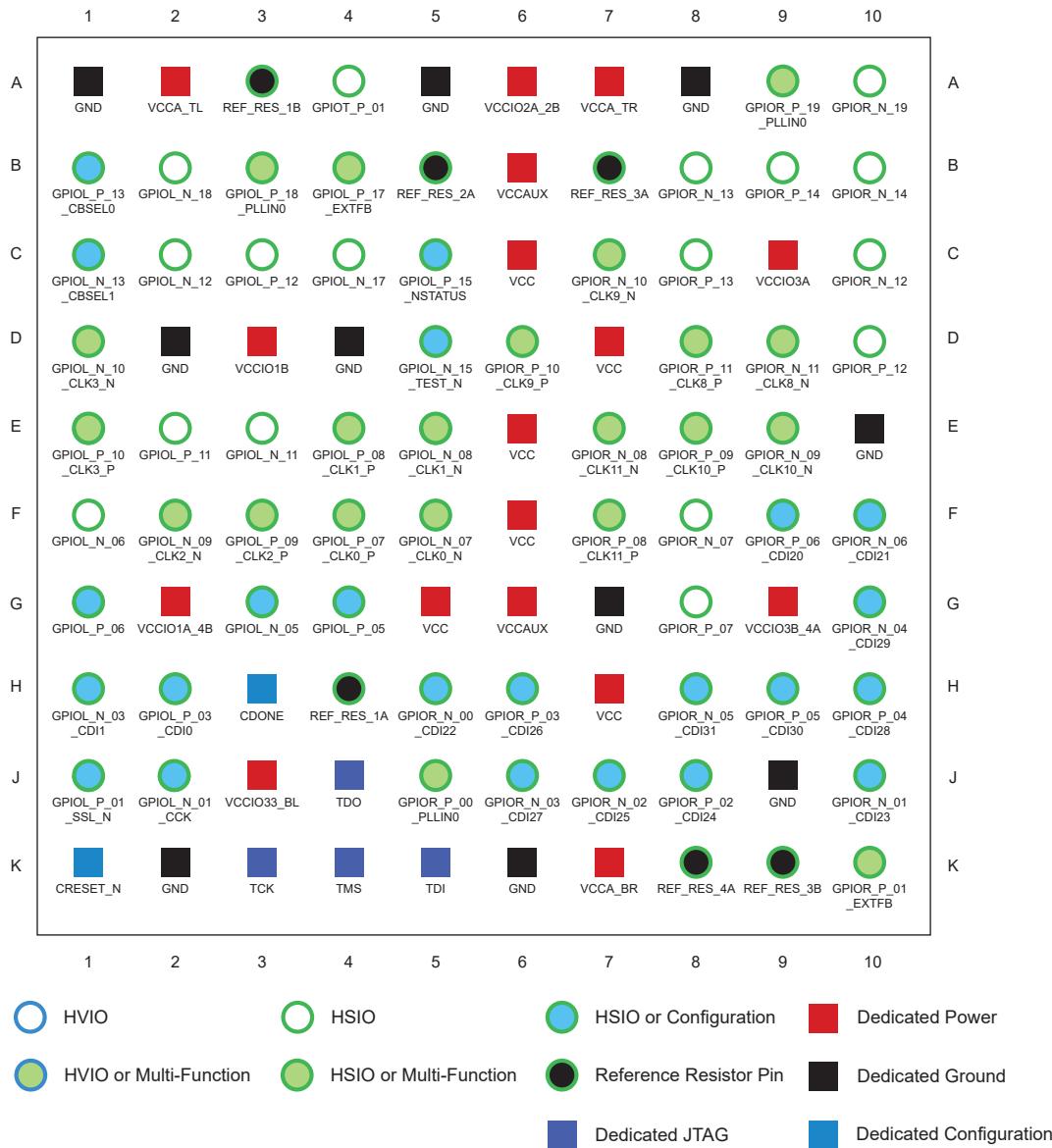


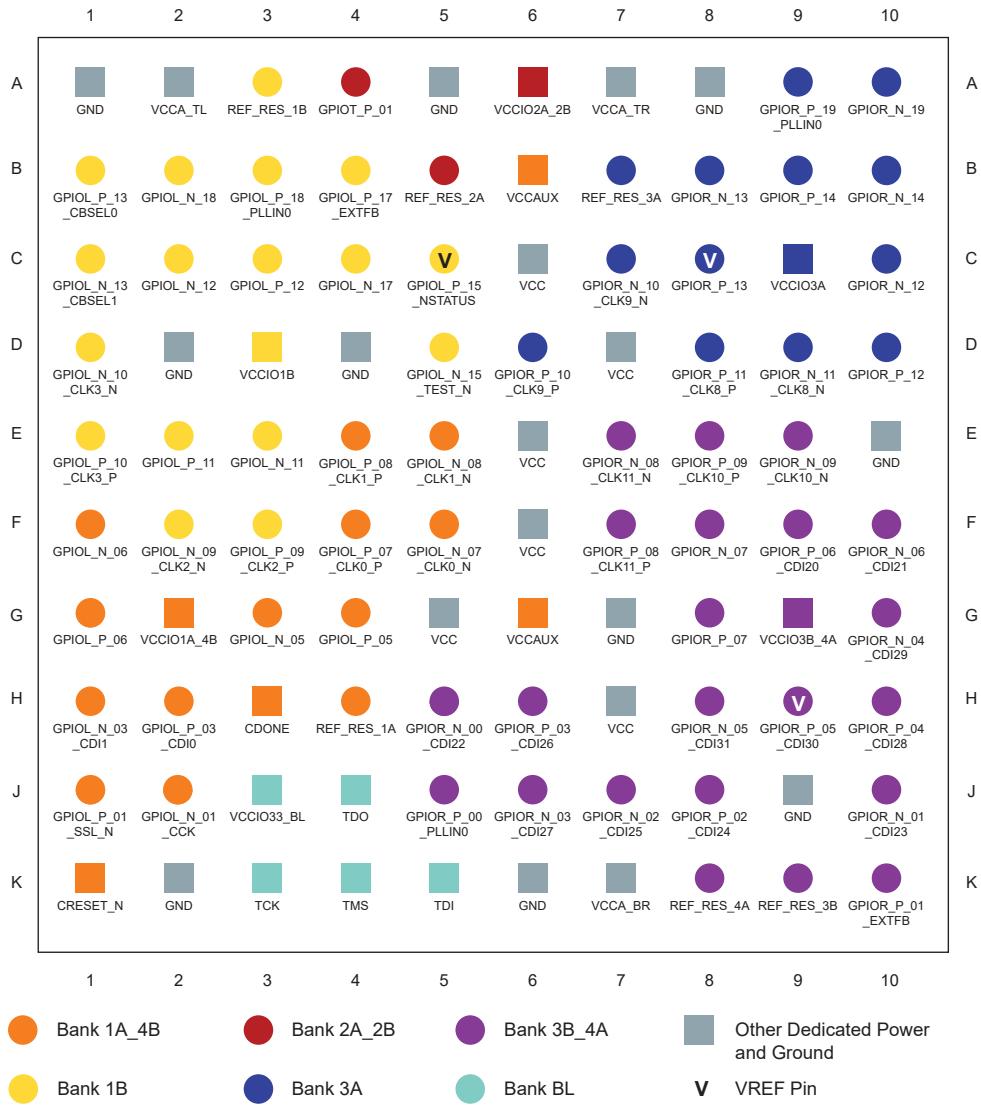
Figure 7: 100-Ball FBGA I/O Bank Diagram

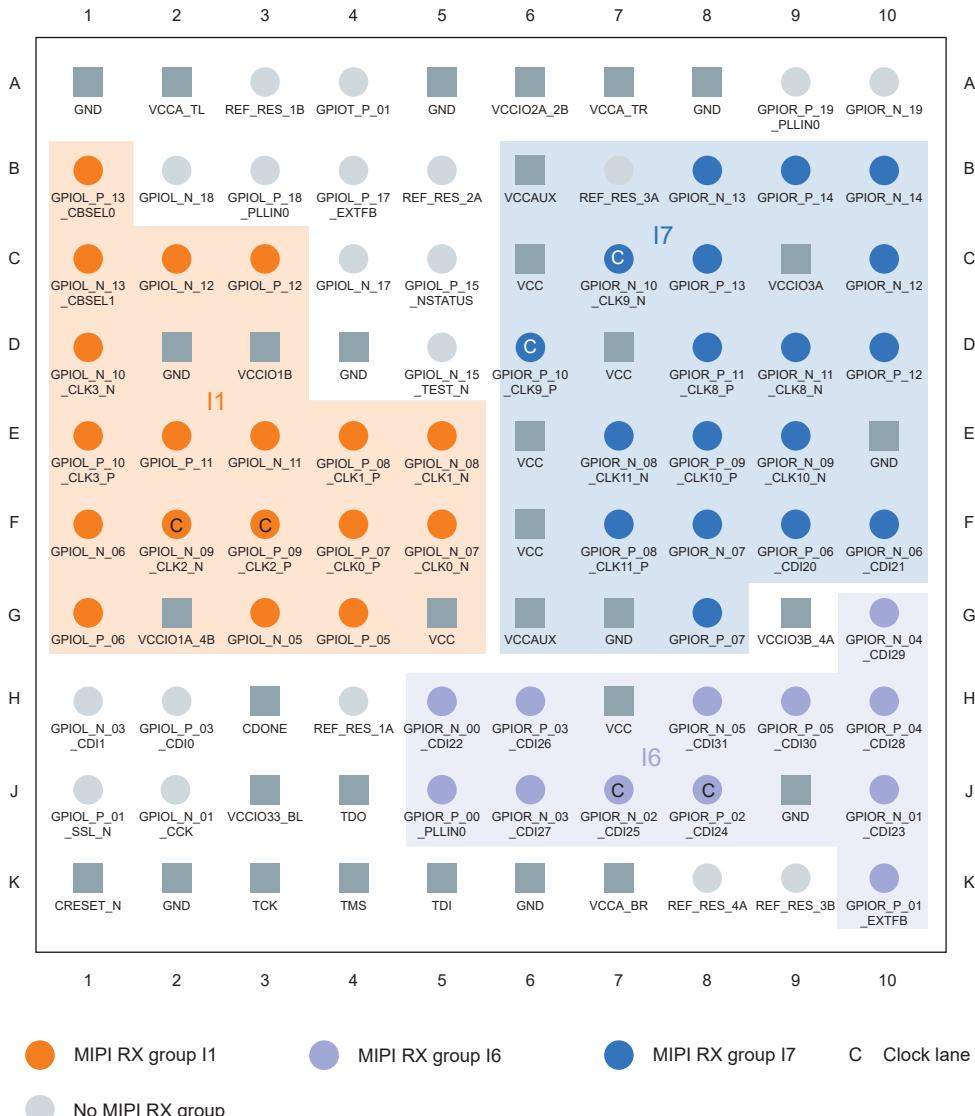
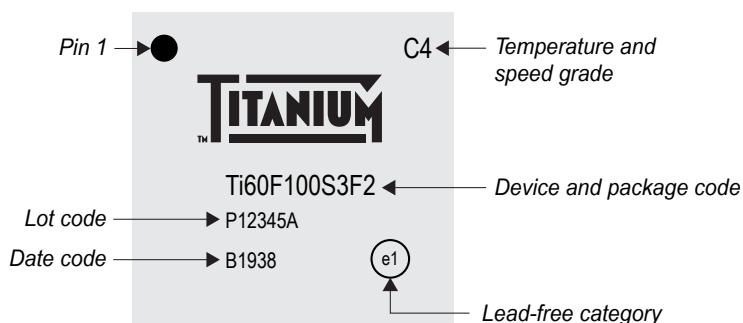
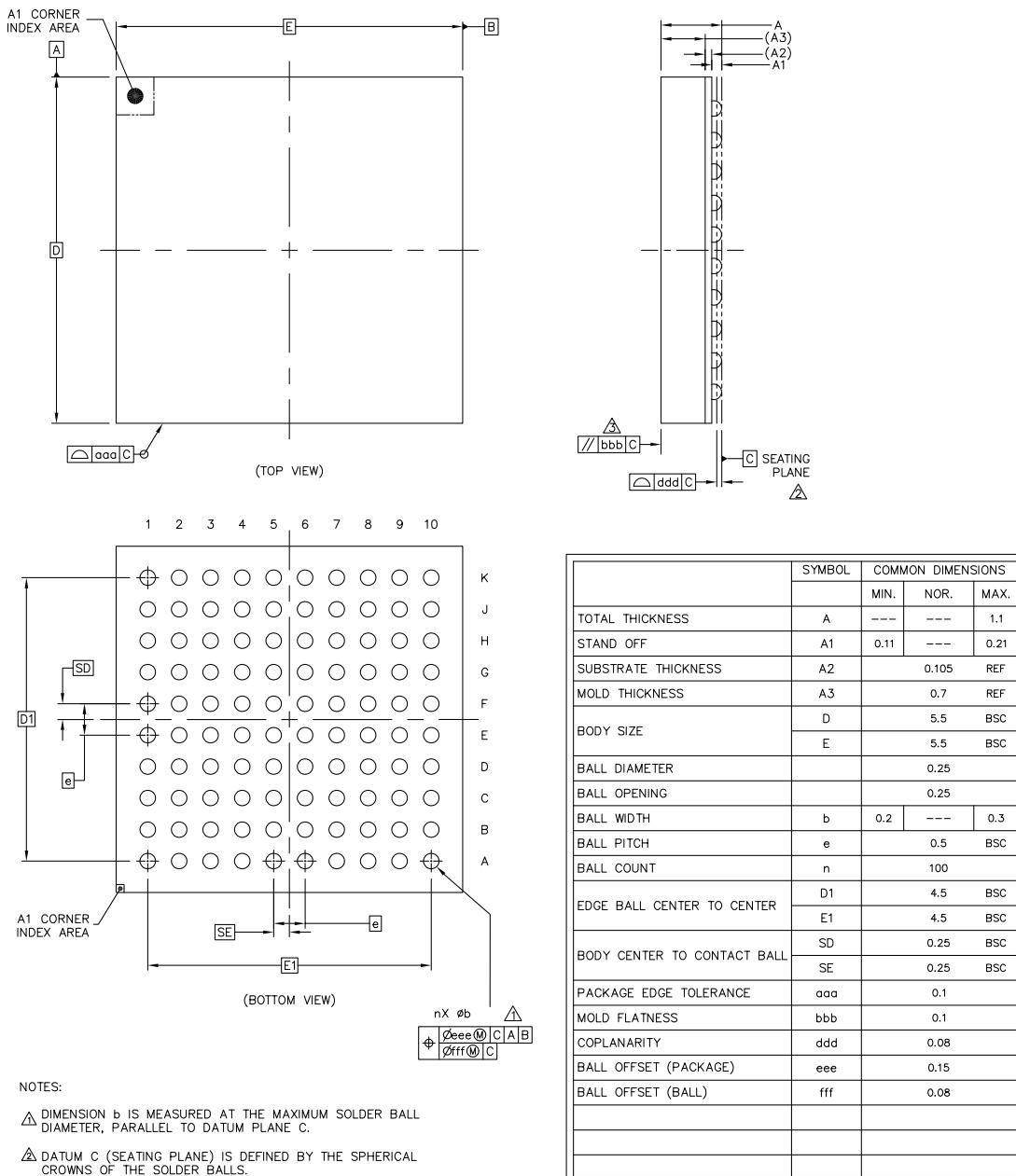
Figure 8: 100-Ball FBGA Emulated MIPI RX Groups**Figure 9: 100-Ball FPGA Package Marking**

Figure 10: 100-Ball FBGA Package Outline



225-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.



Note: Refer to the [F225 Escape Routing](#) on page 64 for an escape routing example.

Figure 11: 225-Ball FBGA Pinout Diagram

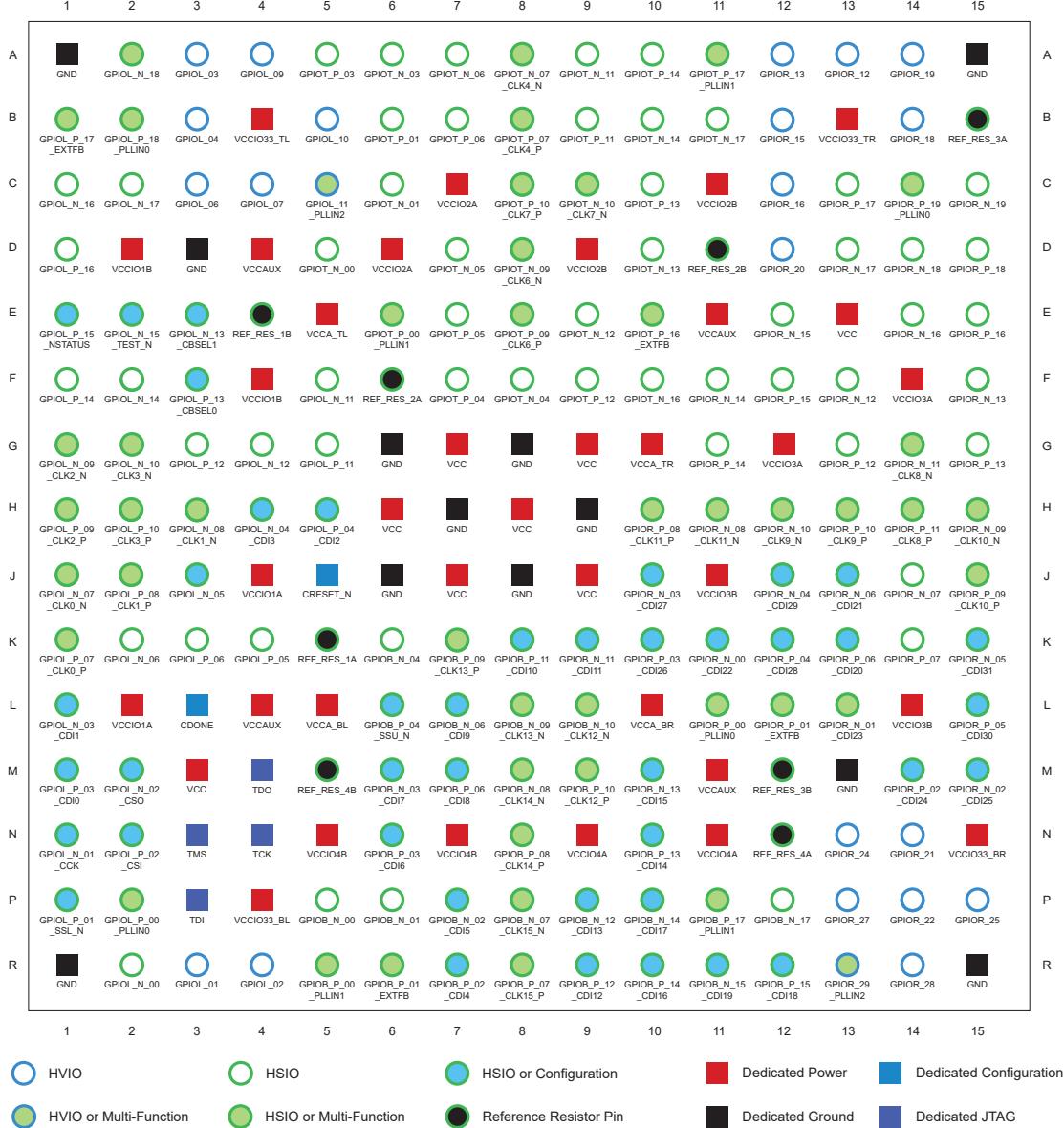


Figure 12: 225-Ball FBGA I/O Bank Diagram

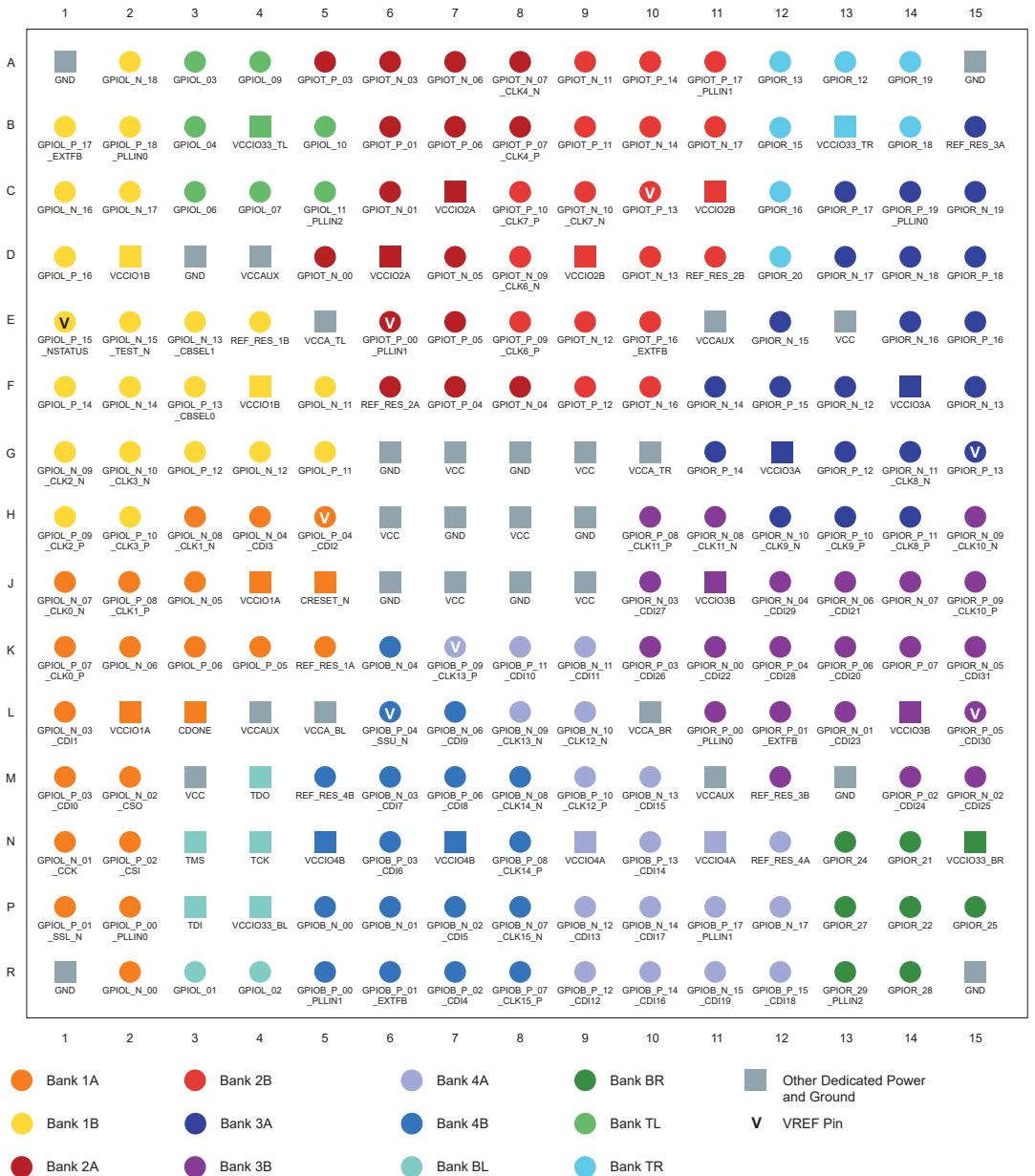


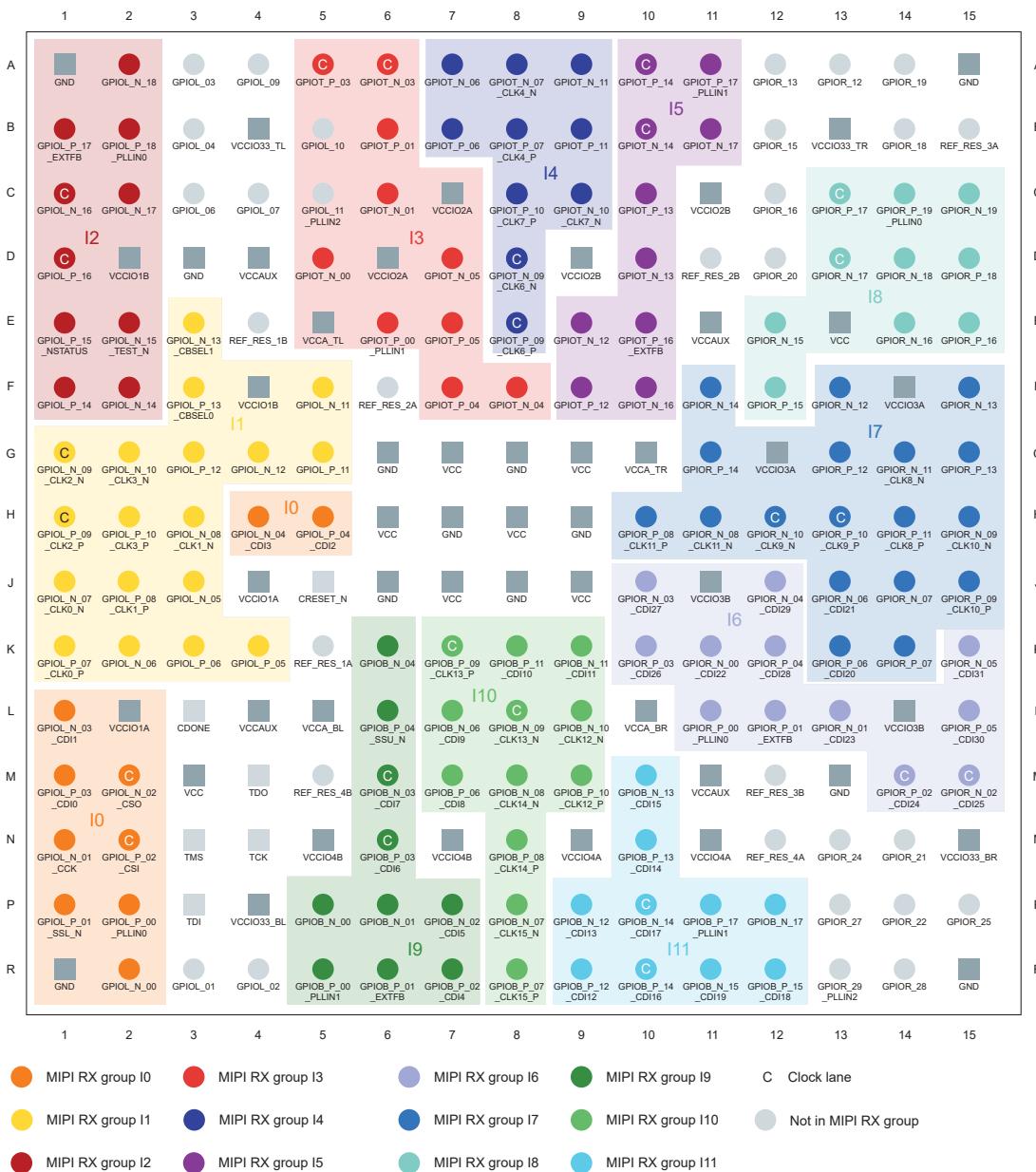
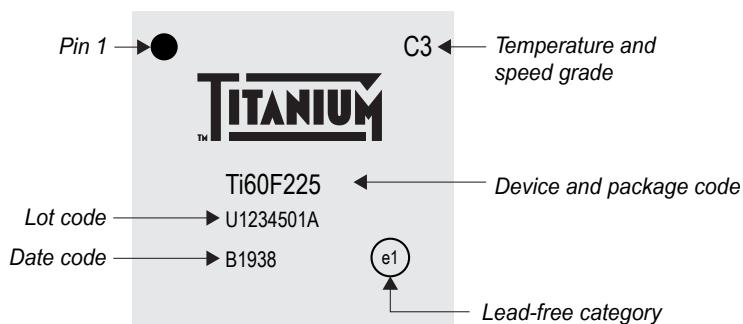
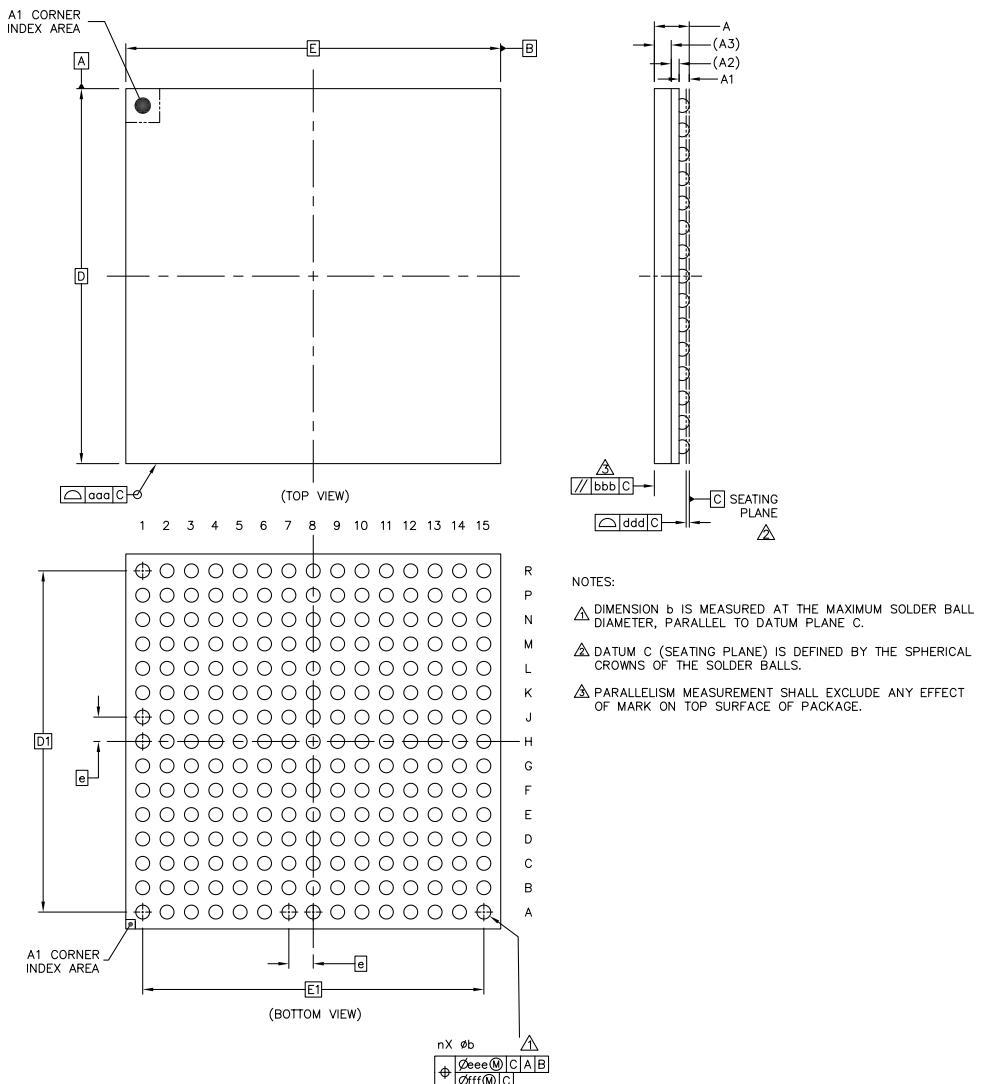
Figure 13: 225-Ball FBGA Emulated MIPI RX Groups**Figure 14: 225-Ball FPGA Package Marking**

Figure 15: 225-Ball FBGA Package Outline



For Lot Number: 'CXXXXXX'

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

For Other Lot Numbers

	Symbol	Common Dimensions		
		Min.	Nor.	Max.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

361-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

361-Ball (J) FBGA Package Specifications

Figure 16: 361-Ball (J) FBGA Pinout Diagram

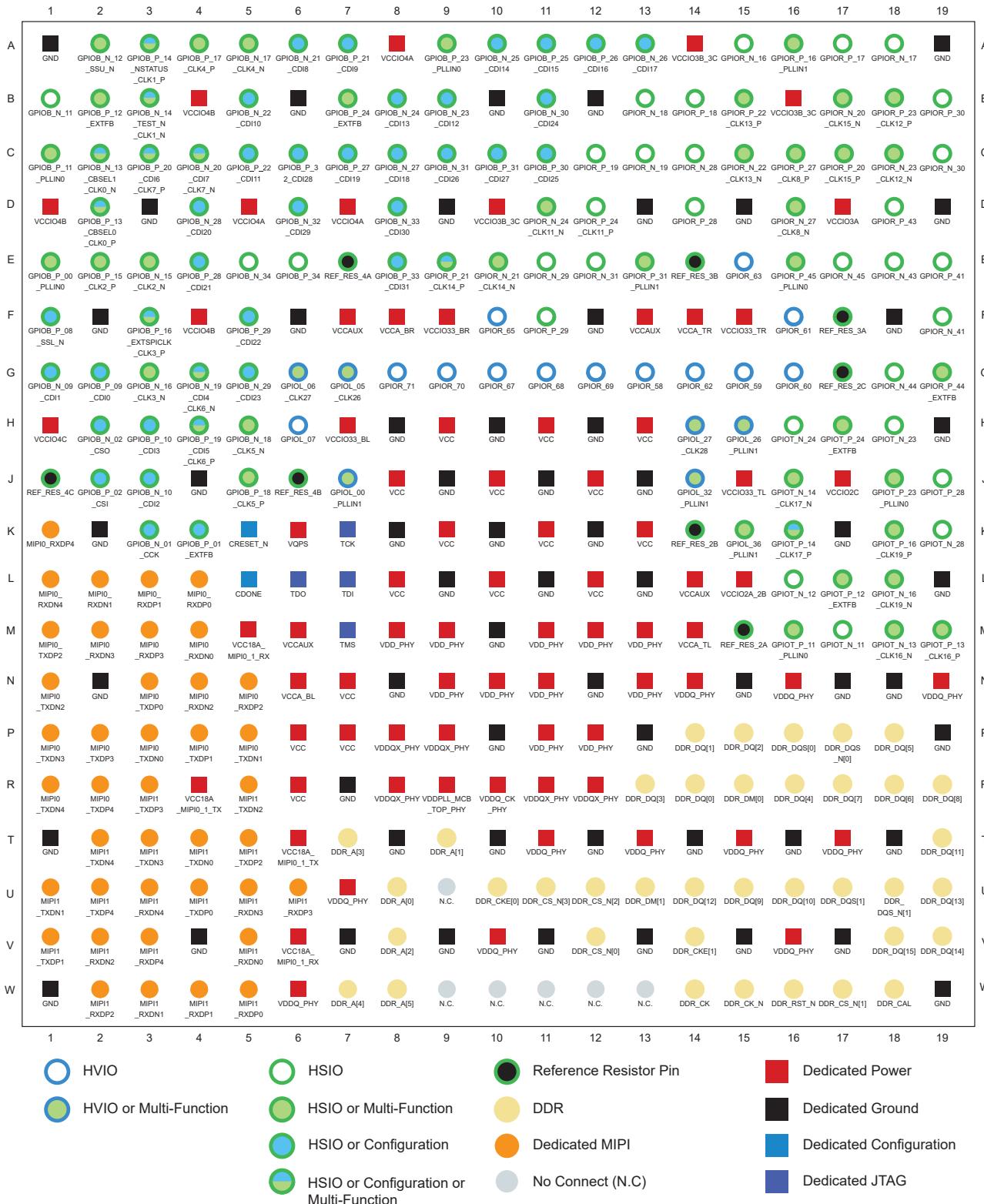


Figure 17: 361-Ball (J) FBGA I/O Bank Diagram

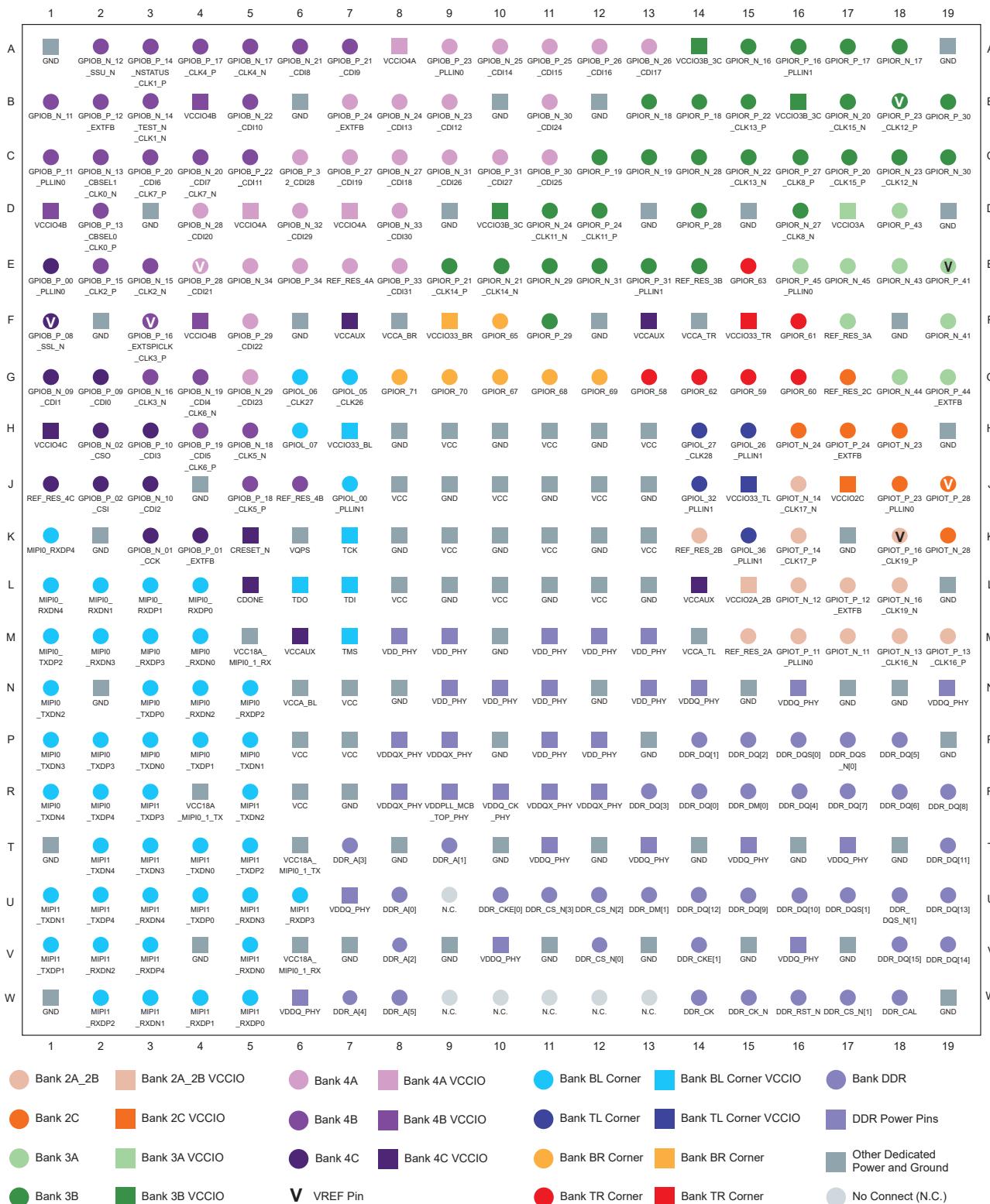


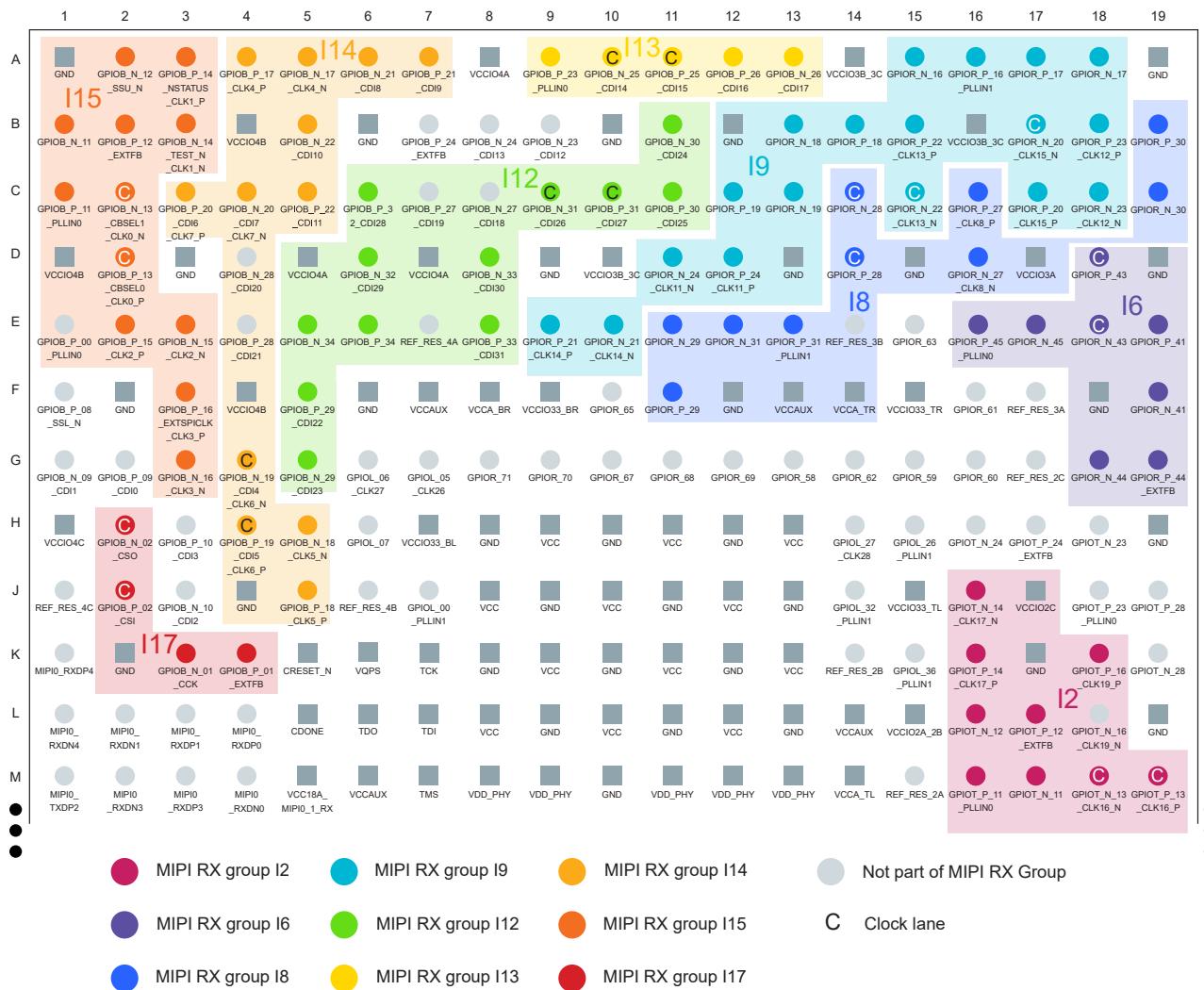
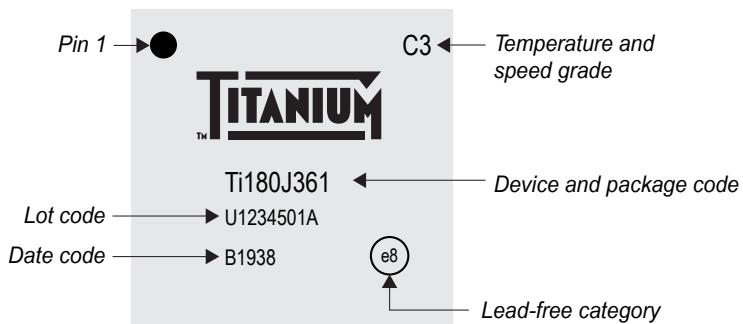
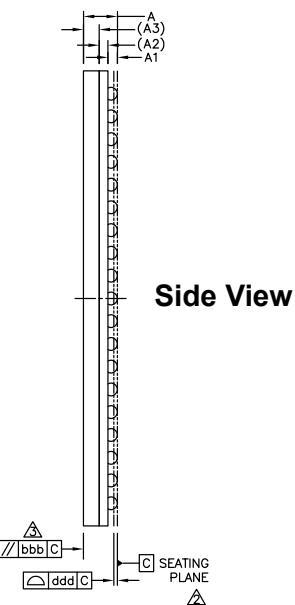
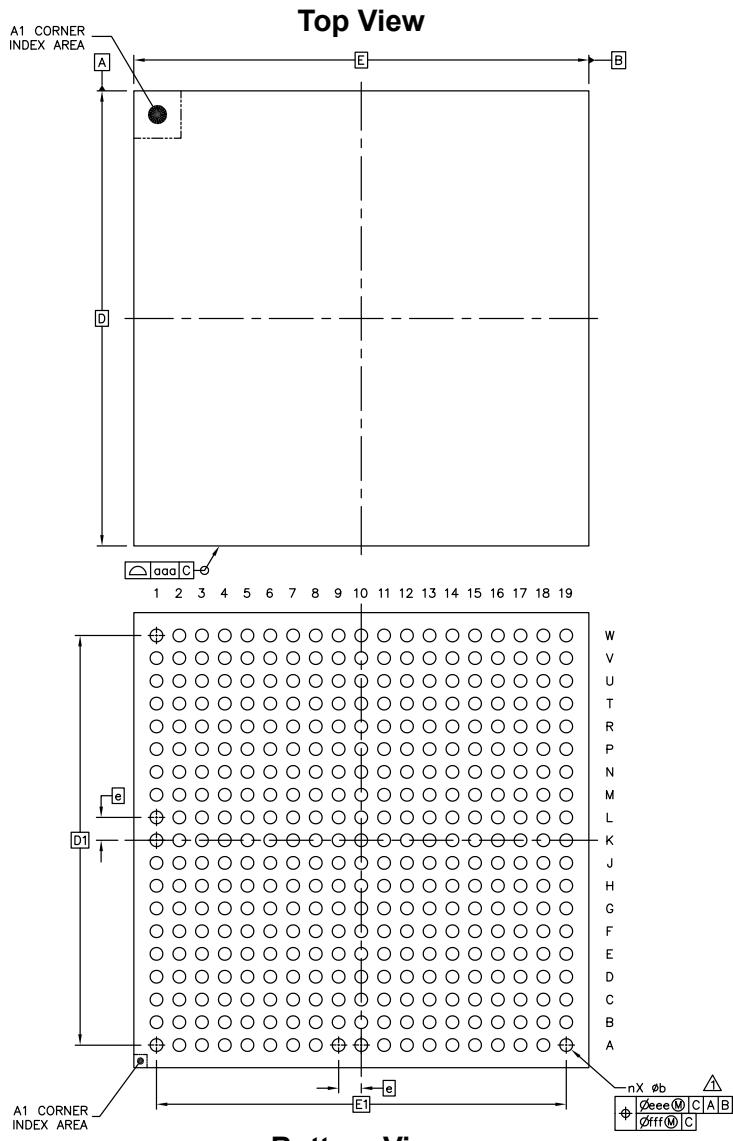
Figure 18: 361-Ball (J) FBGA Emulated MIPI RX Groups**Figure 19: 361-Ball (J) FPGA Package Marking**

Figure 20: 361-Ball (J) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.893	0.968	1.1
STAND OFF	A1	0.22	0.27	0.32
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D	13	BSC	
	E	13	BSC	
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	0.37	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n	361		
EDGE BALL CENTER TO CENTER	D1	11.7	BSC	
	E1	11.7	BSC	
BODY CENTER TO CONTACT BALL	SD	---	BSC	
	SE	---	BSC	
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.2		
COPLANARITY	ddd	0.1		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.08		

NOTES:

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.

△ DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

△ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

361-Ball (M) FBGA Package Specifications

Figure 21: 361-Ball (M) FBGA Pinout Diagram

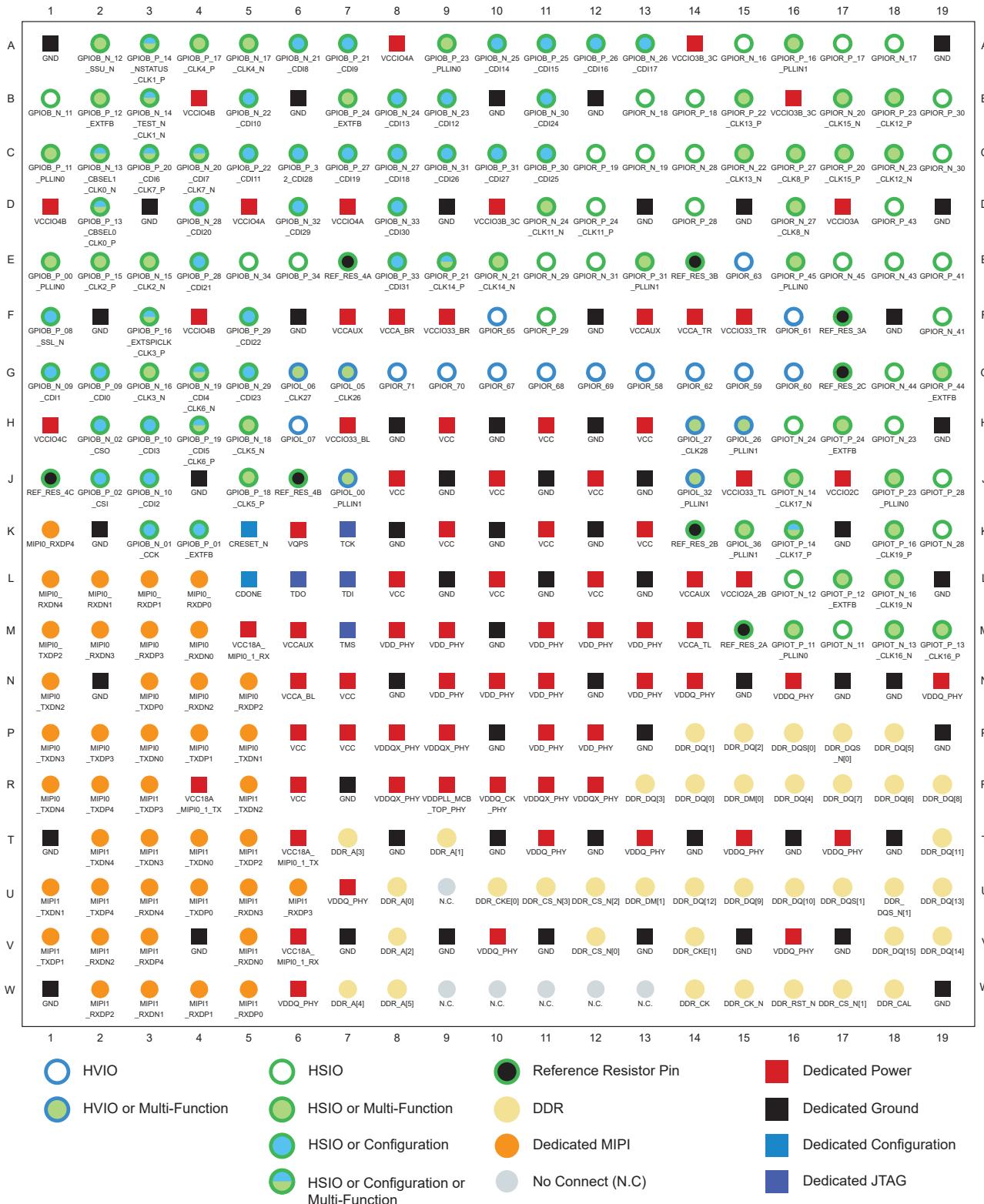


Figure 22: 361-Ball (M) FBGA I/O Bank Diagram

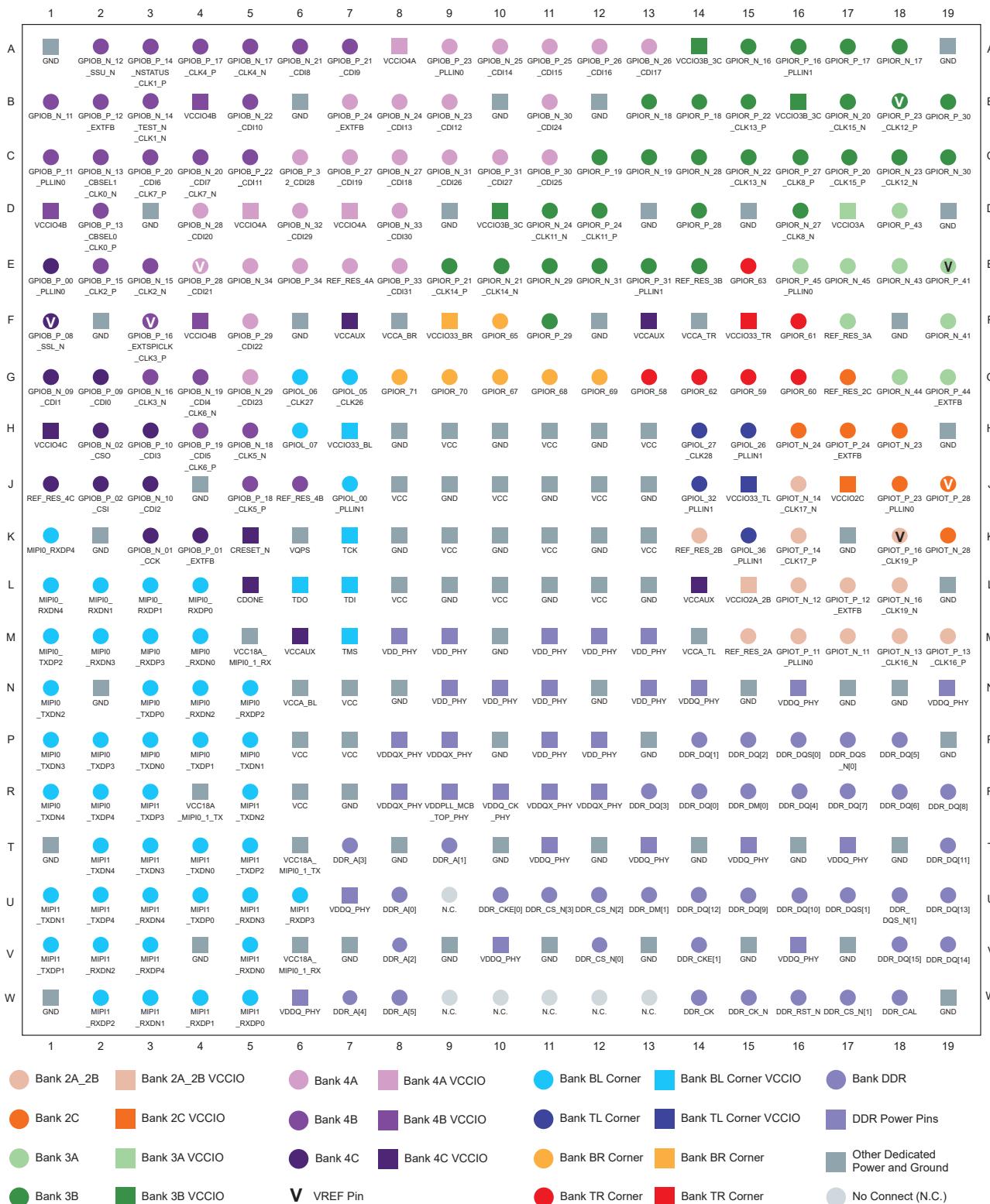


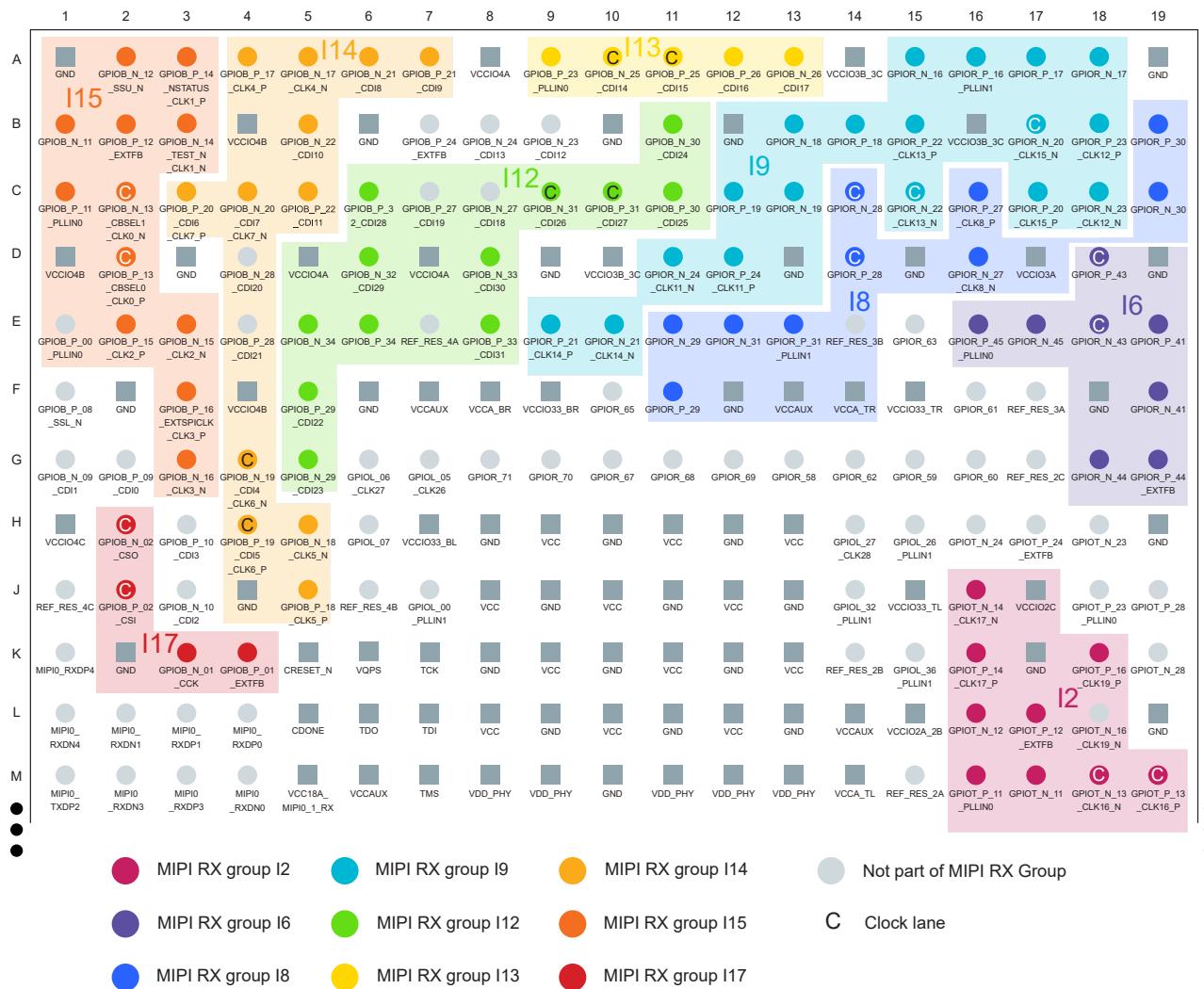
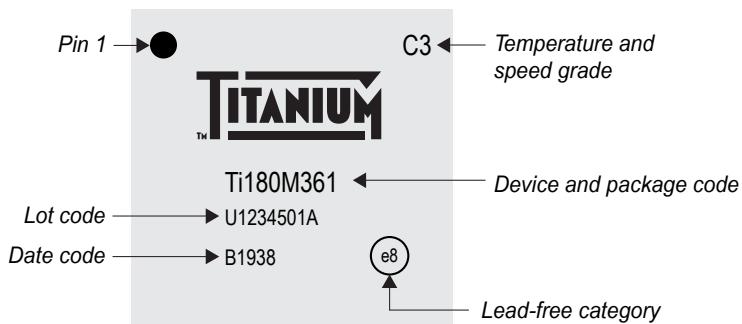
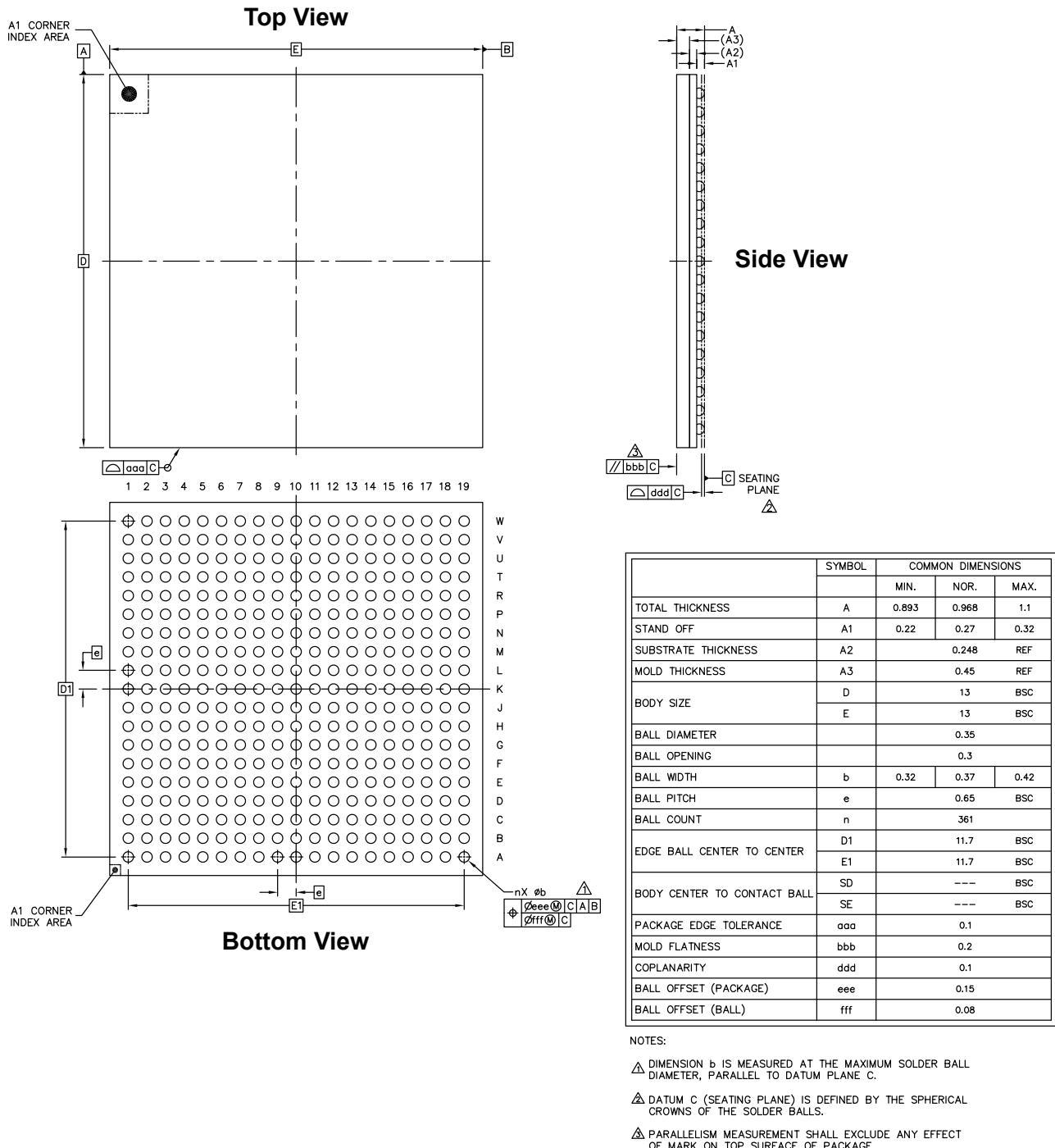
Figure 23: 361-Ball (M) FBGA Emulated MIPI RX Groups**Figure 24: 361-Ball (M) FPGA Package Marking**

Figure 25: 361-Ball (M) FBGA Package Outline



400-Ball (G) FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 26: 400-Ball (G) FBGA Pinout Diagram

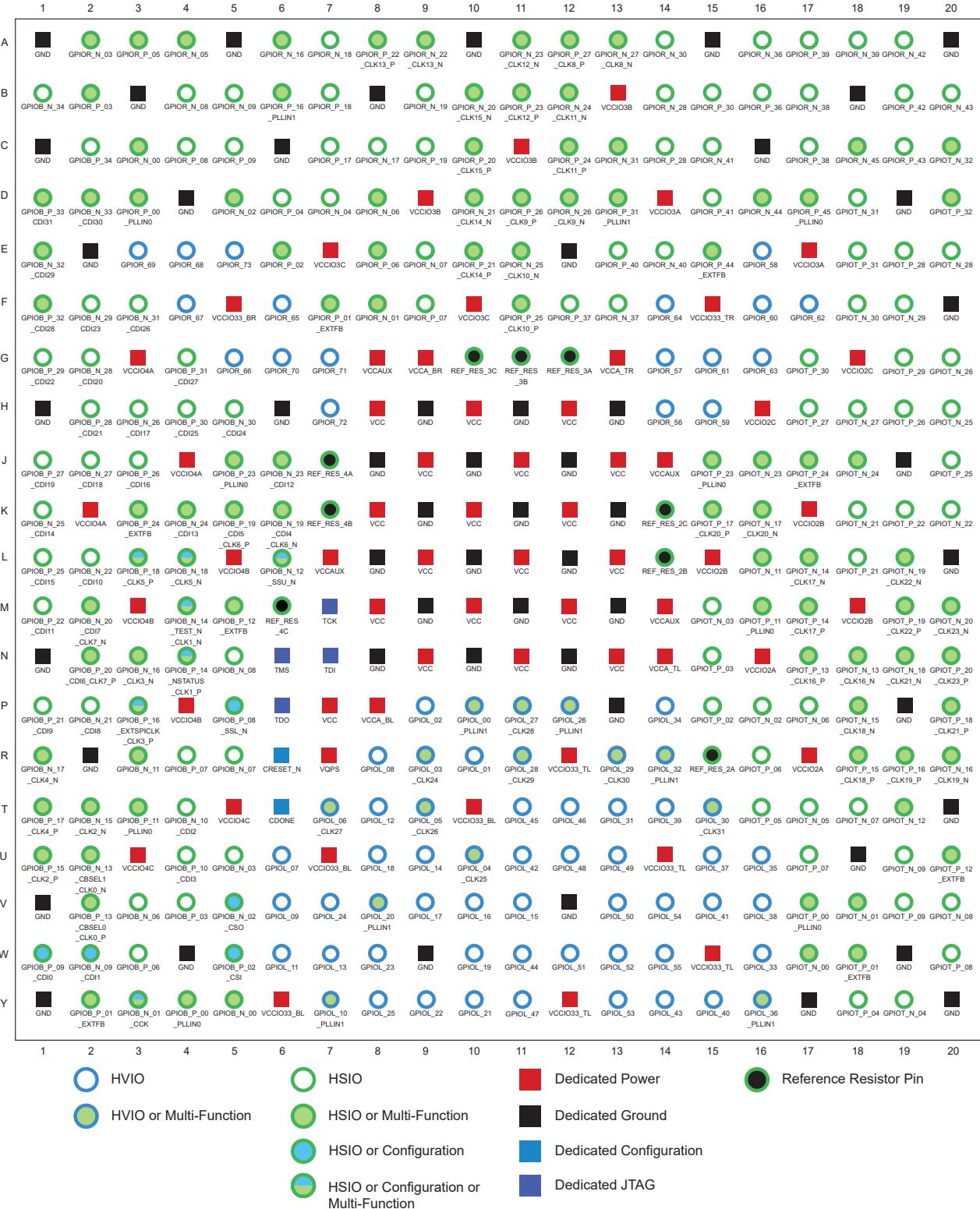


Figure 27: 400-Ball (G) FBGA I/O Bank Diagram

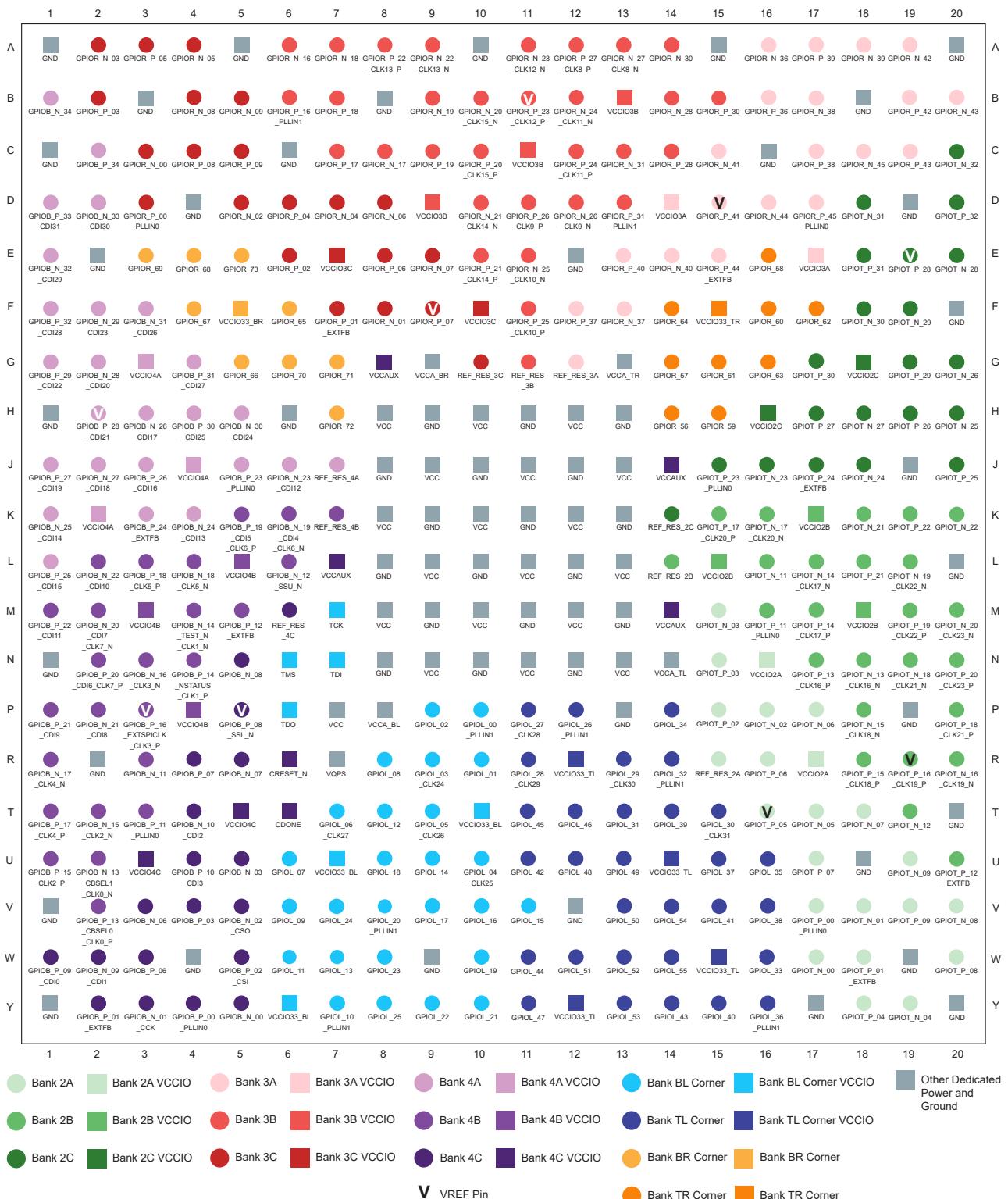


Figure 28: 400-Ball (G) FBGA Emulated MIPI RX Groups

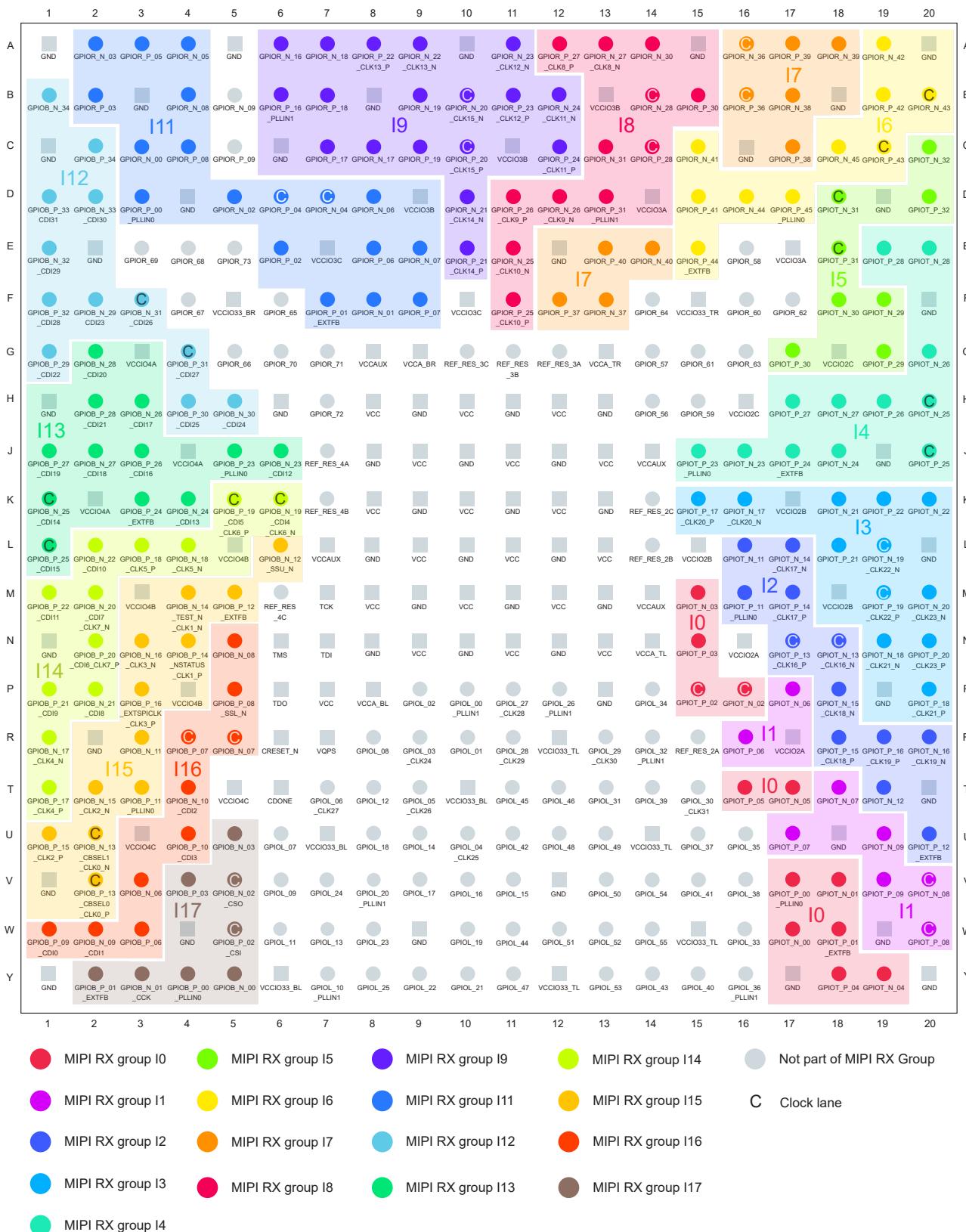


Figure 29: 400-Ball (G) FPGA Package Marking

Preliminary.

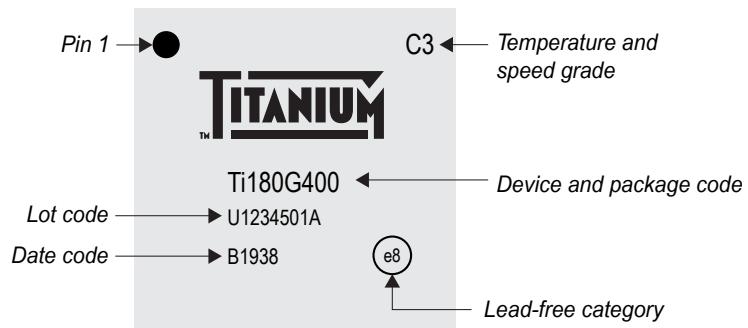
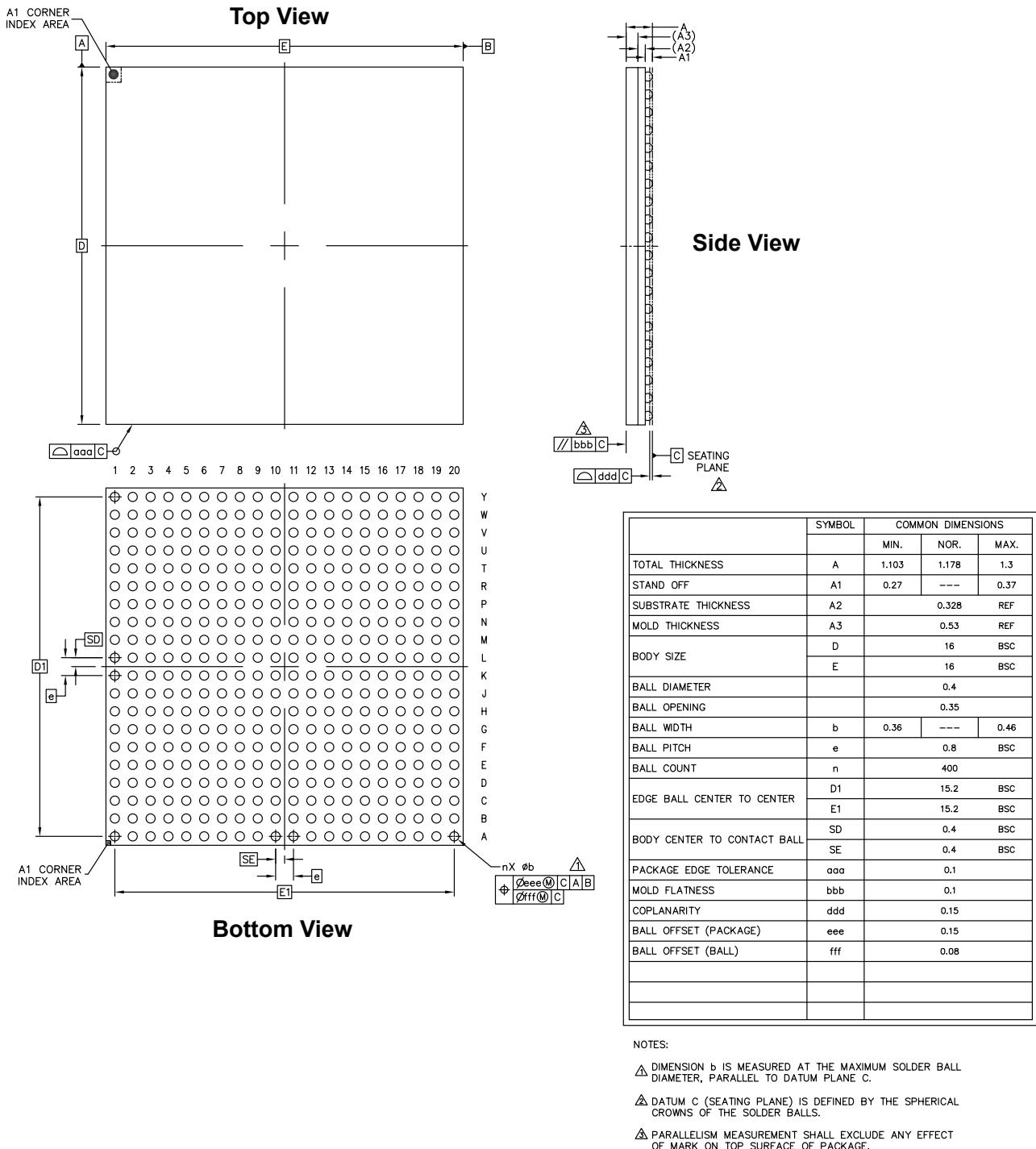


Figure 30: 400-Ball (G) FBGA Package Outline



484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

484-Ball (J) FBGA Package Specifications

Figure 31: 484-Ball (J) FBGA Pinout Diagram

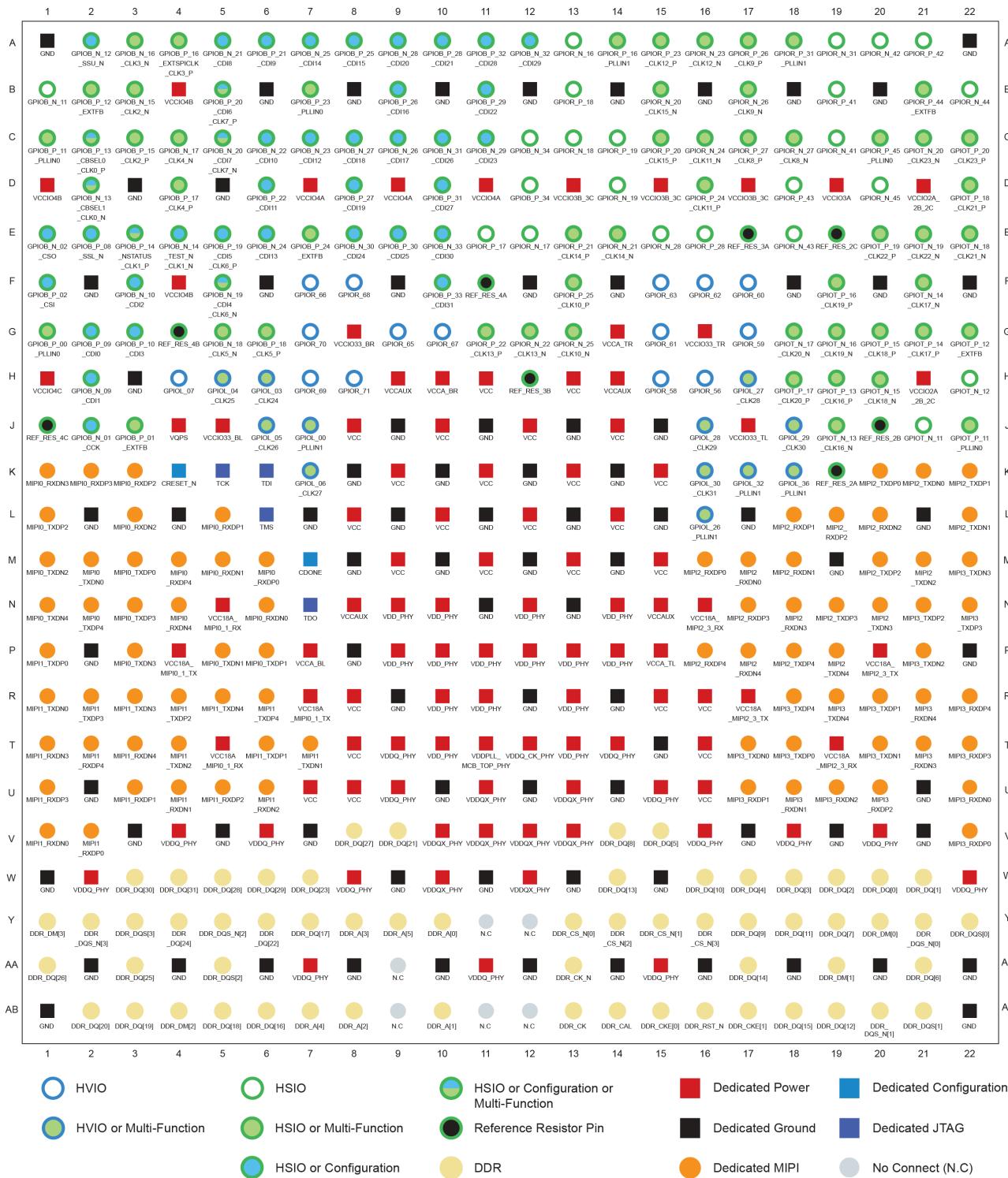


Figure 32: 484-Ball (J) FBGA I/O Bank Diagram

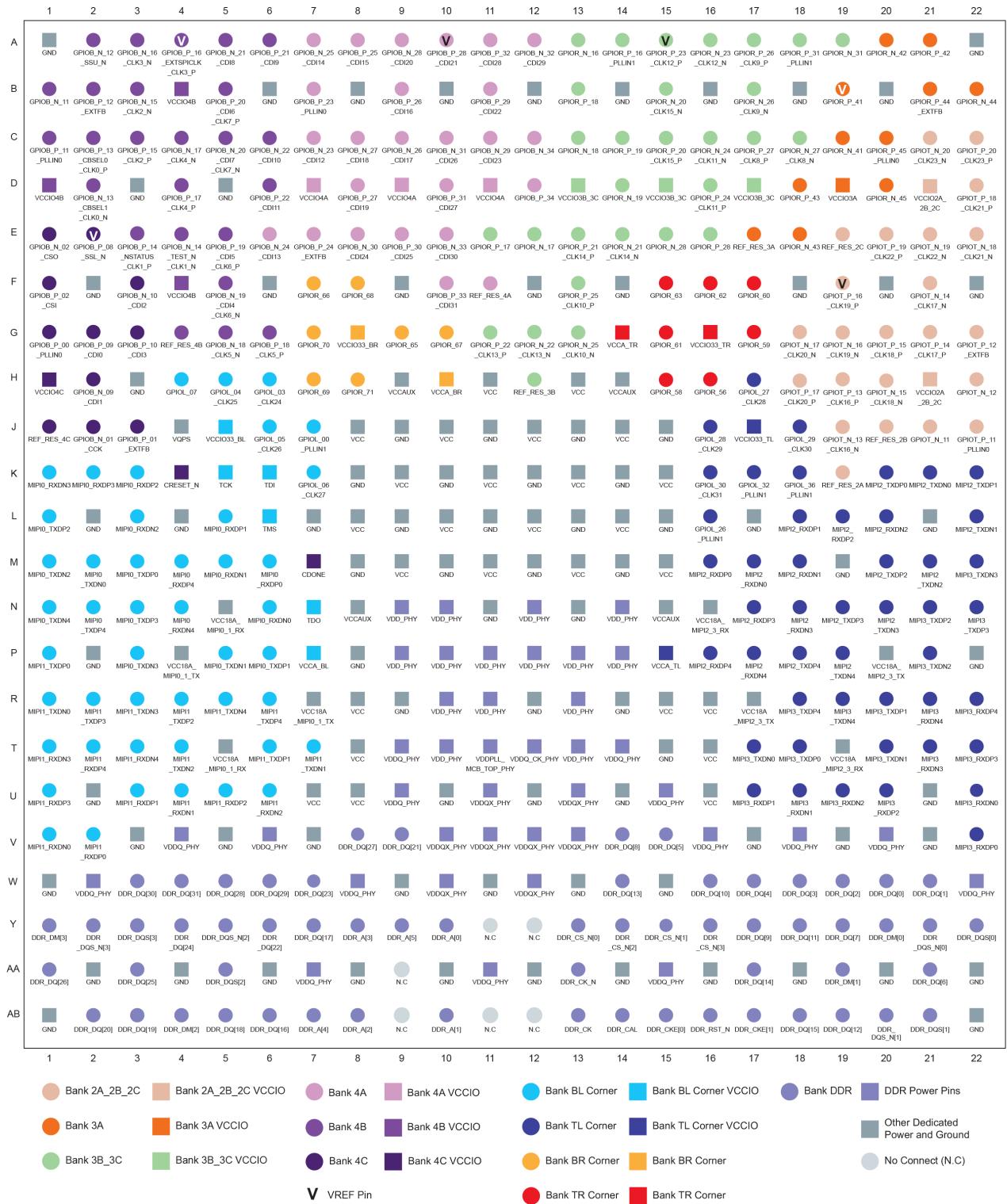


Figure 33: 484-Ball (J) FBGA Emulated MIPI RX Groups

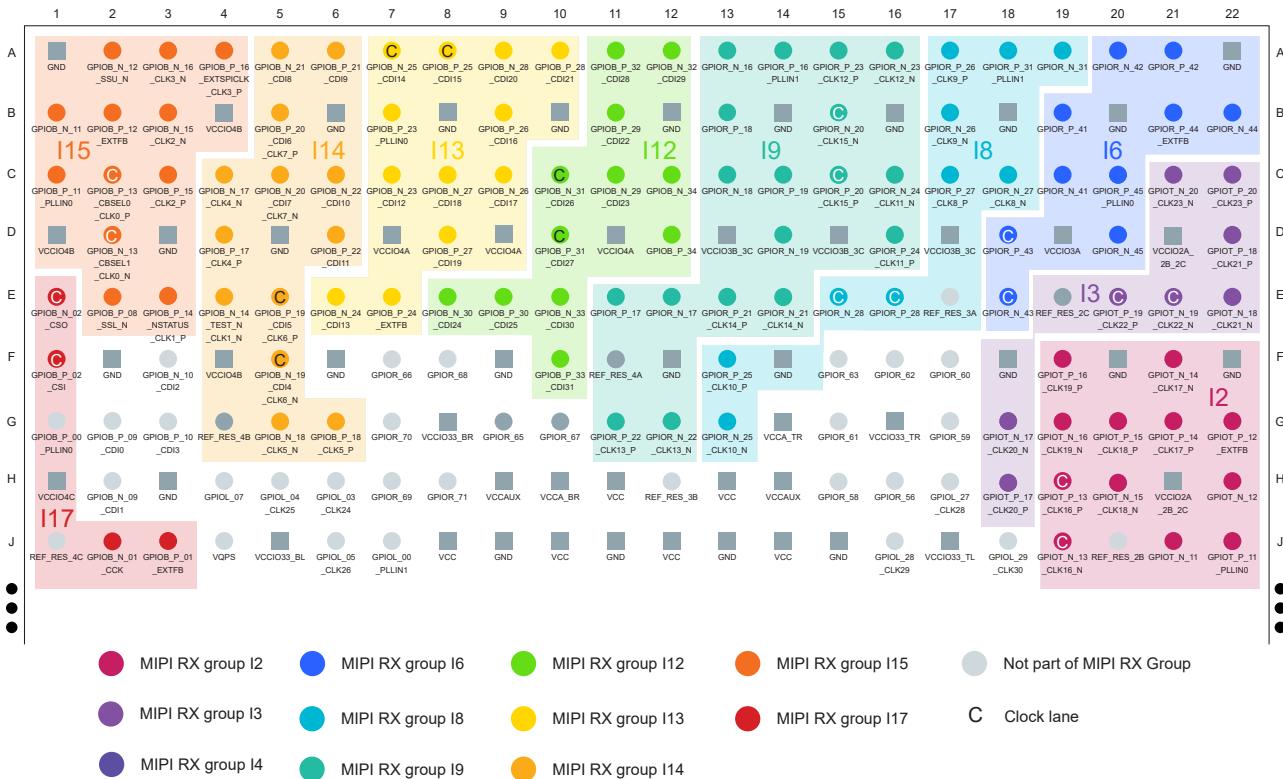


Figure 34: 484-Ball (J) FBGA Package Marking

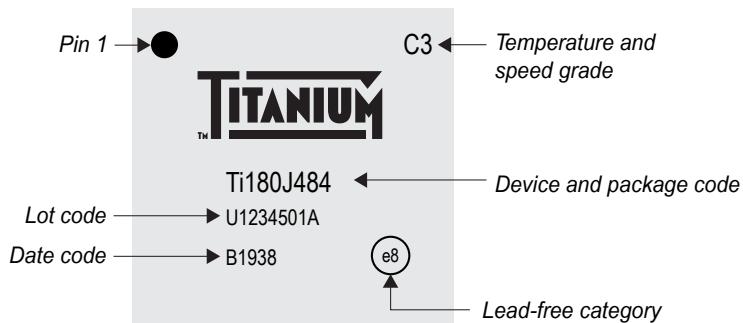
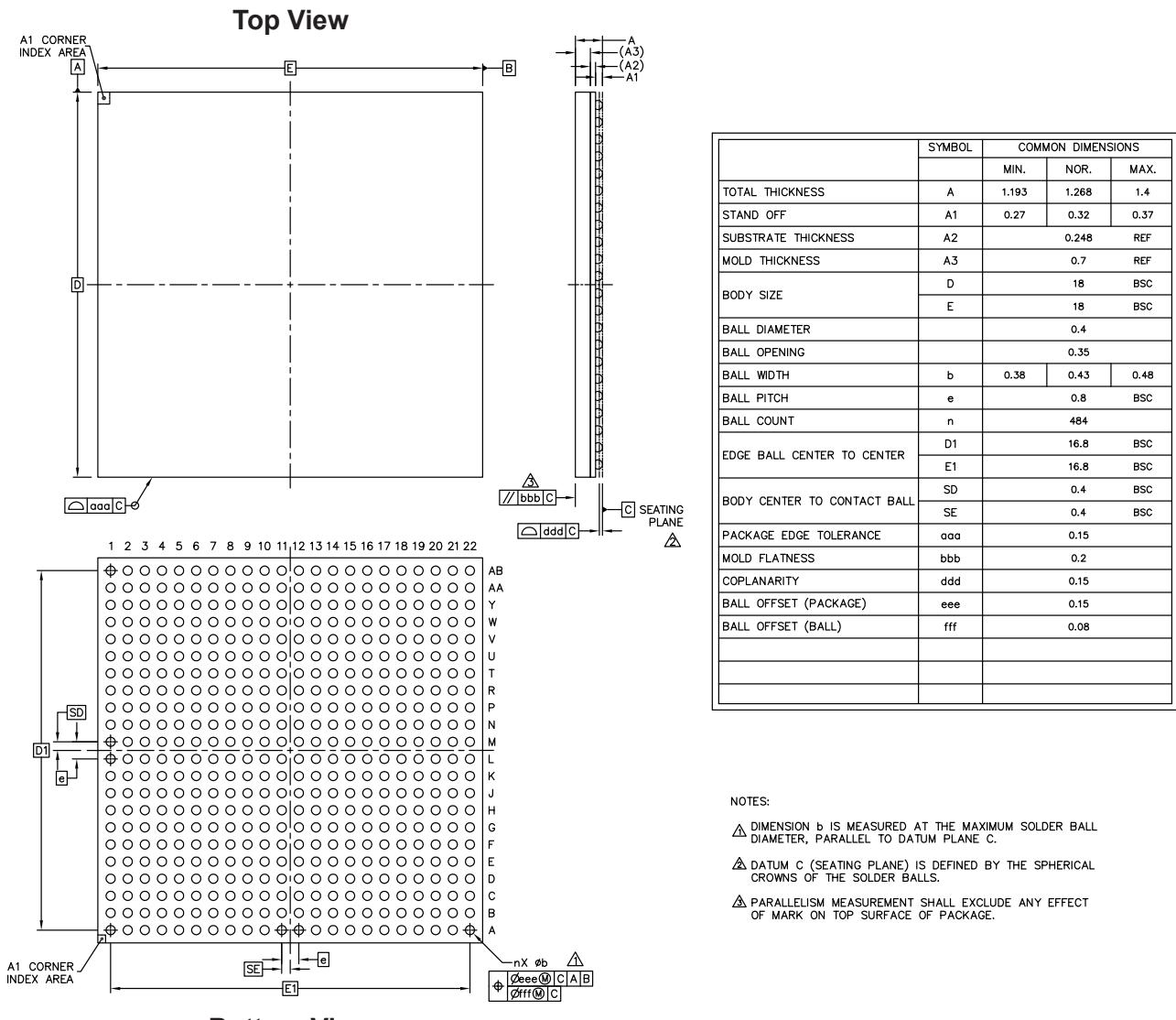


Figure 35: 484-Ball (J) FBGA Package Outline



484-Ball (L) FBGA Package Specifications

Figure 36: 484-Ball (L) FBGA Pinout Diagram

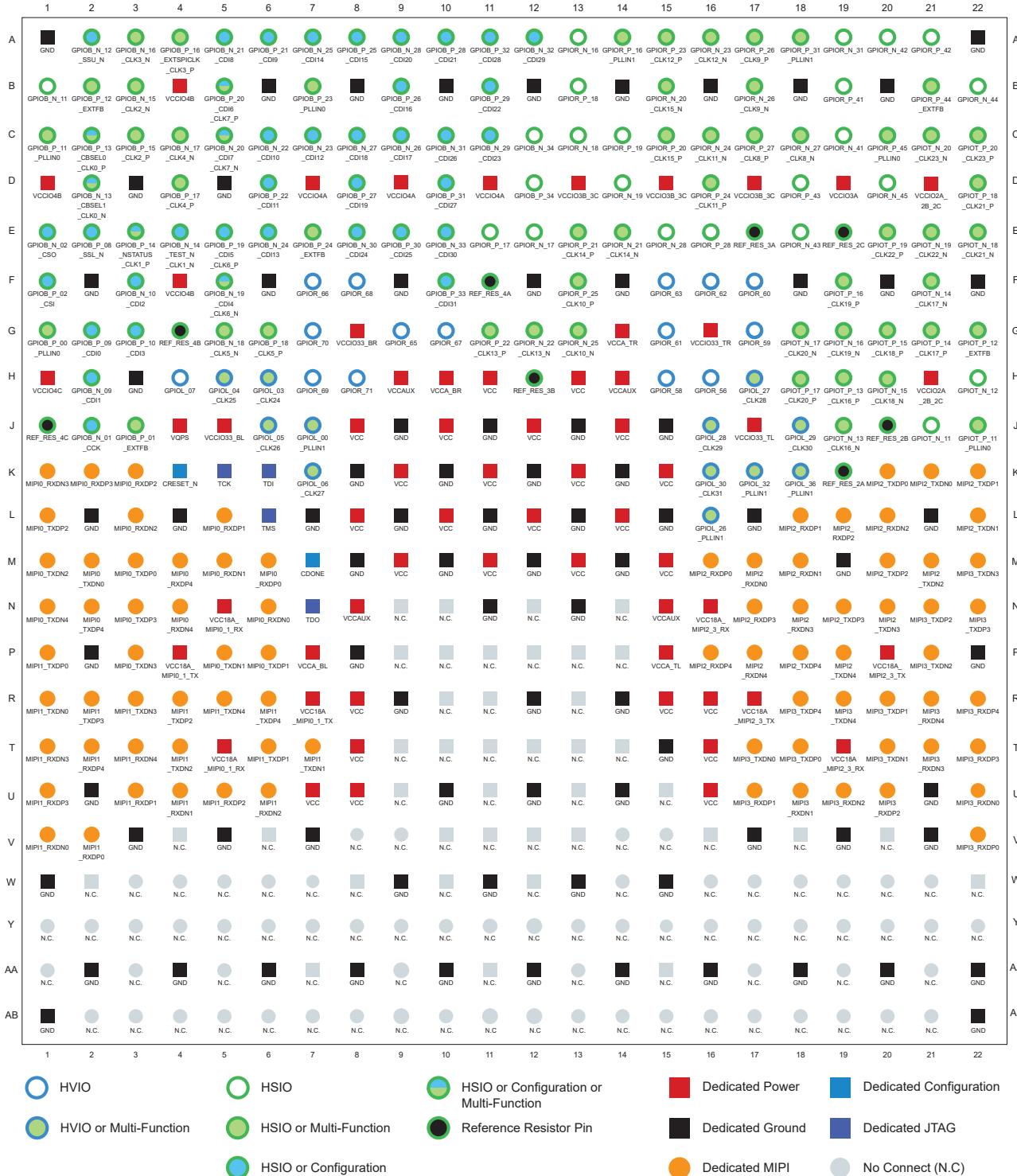


Figure 37: 484-Ball (L) FBGA I/O Bank Diagram

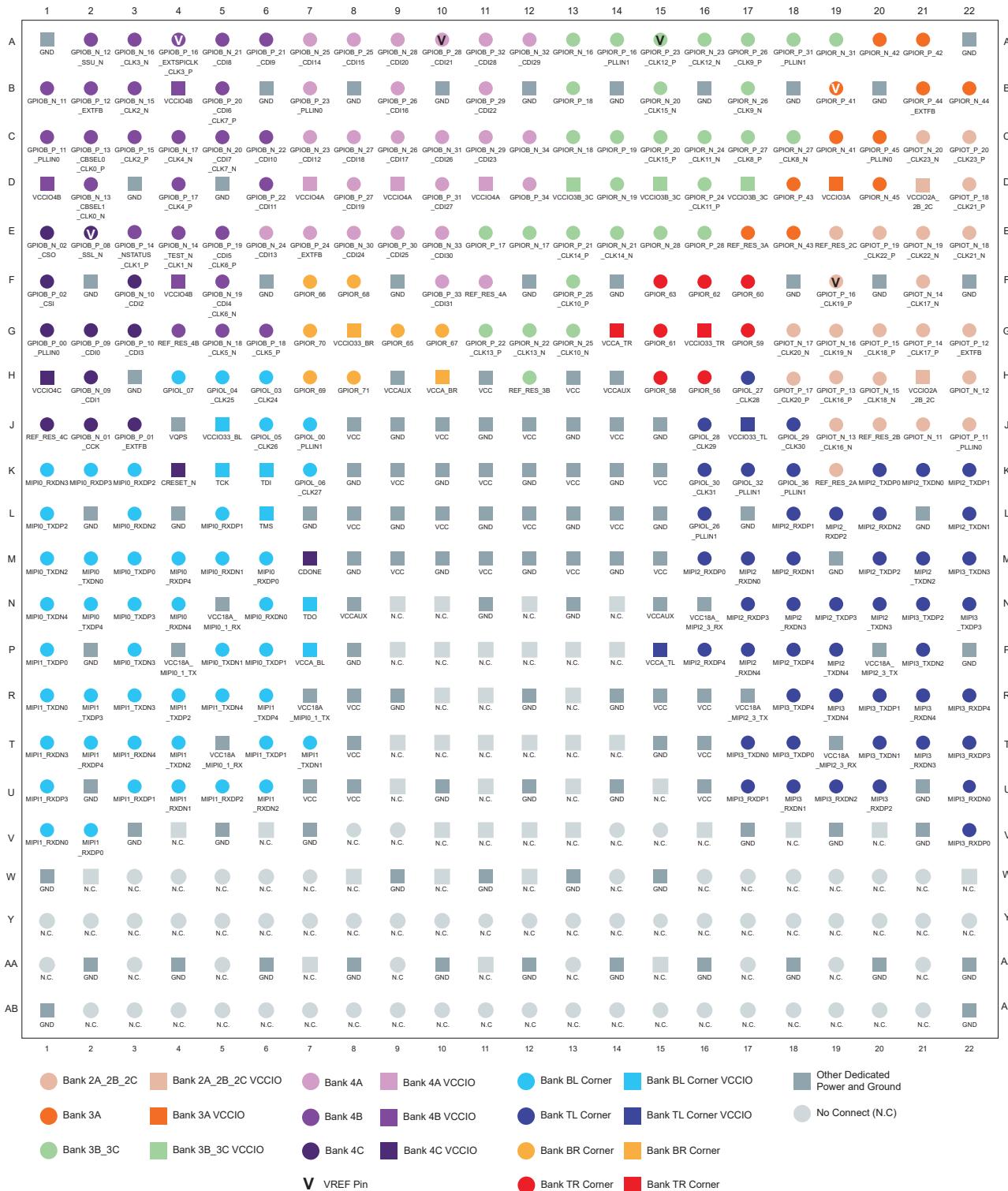


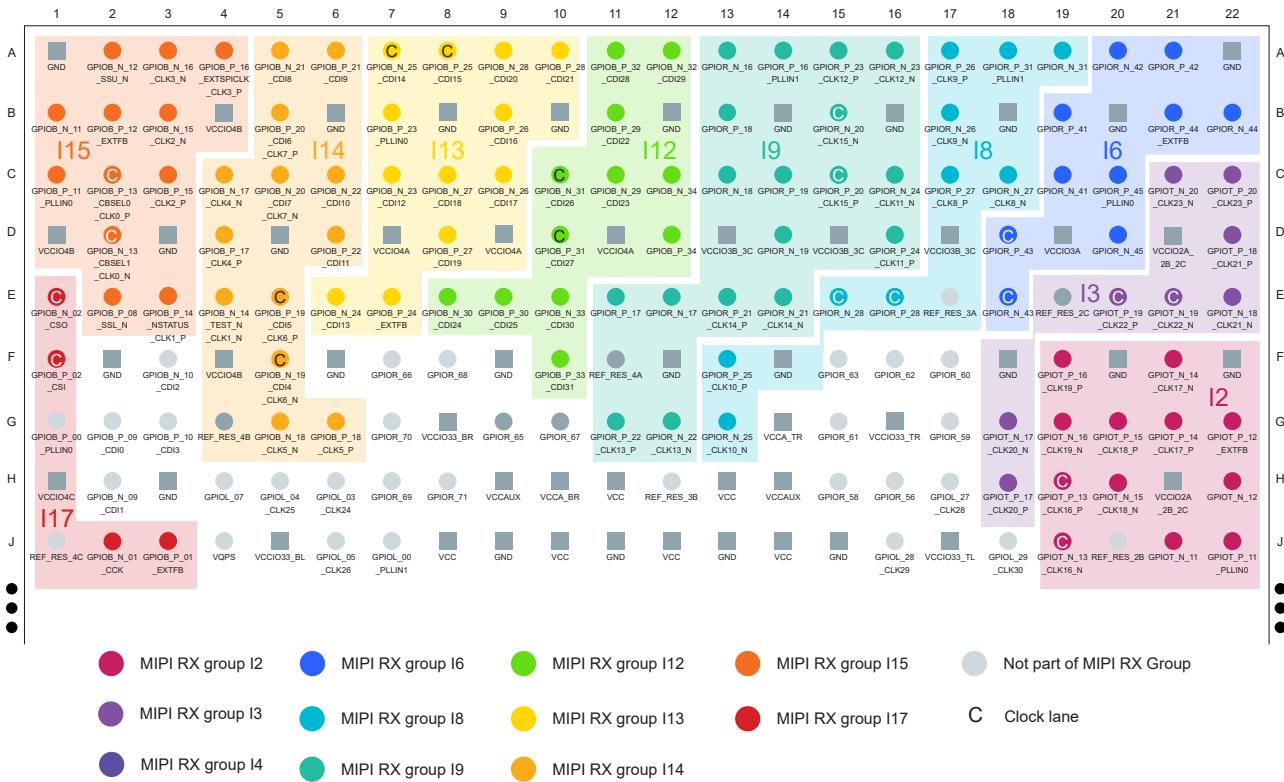
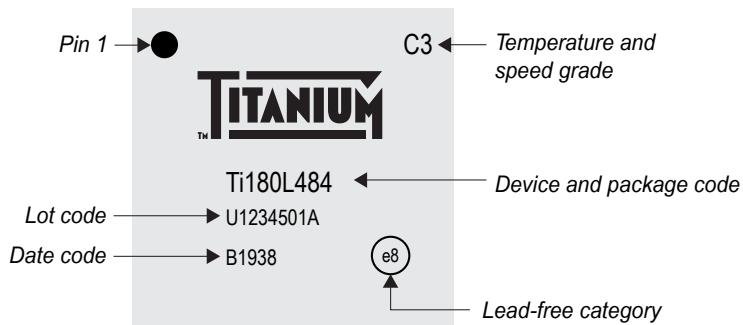
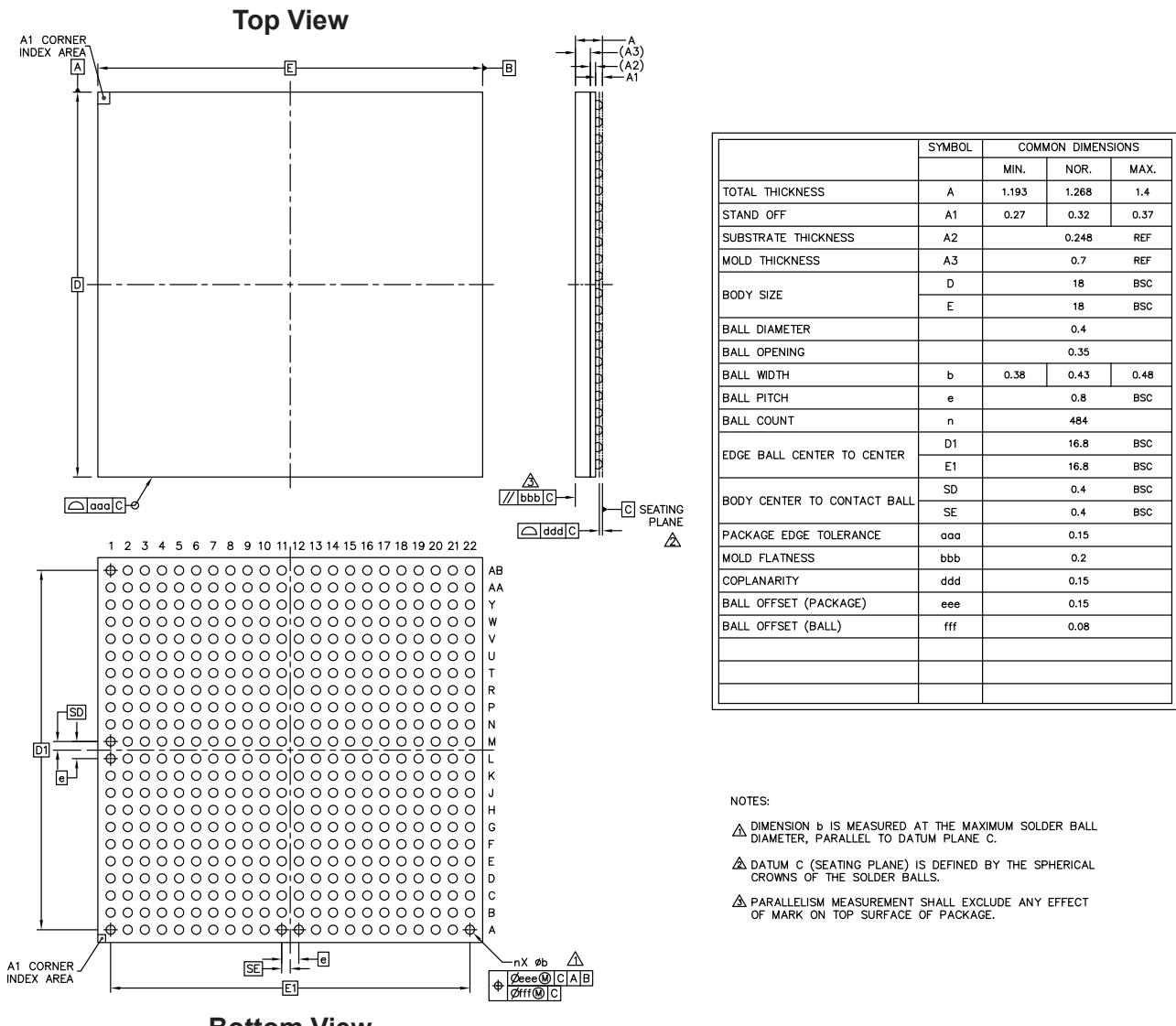
Figure 38: 484-Ball (L) FBGA Emulated MIPI RX Groups**Figure 39: 484-Ball (L) FBGA Package Marking**

Figure 40: 484-Ball (L) FBGA Package Outline



484-Ball (M) FBGA Package Specifications

Figure 41: 484-Ball (M) FBGA Pinout Diagram

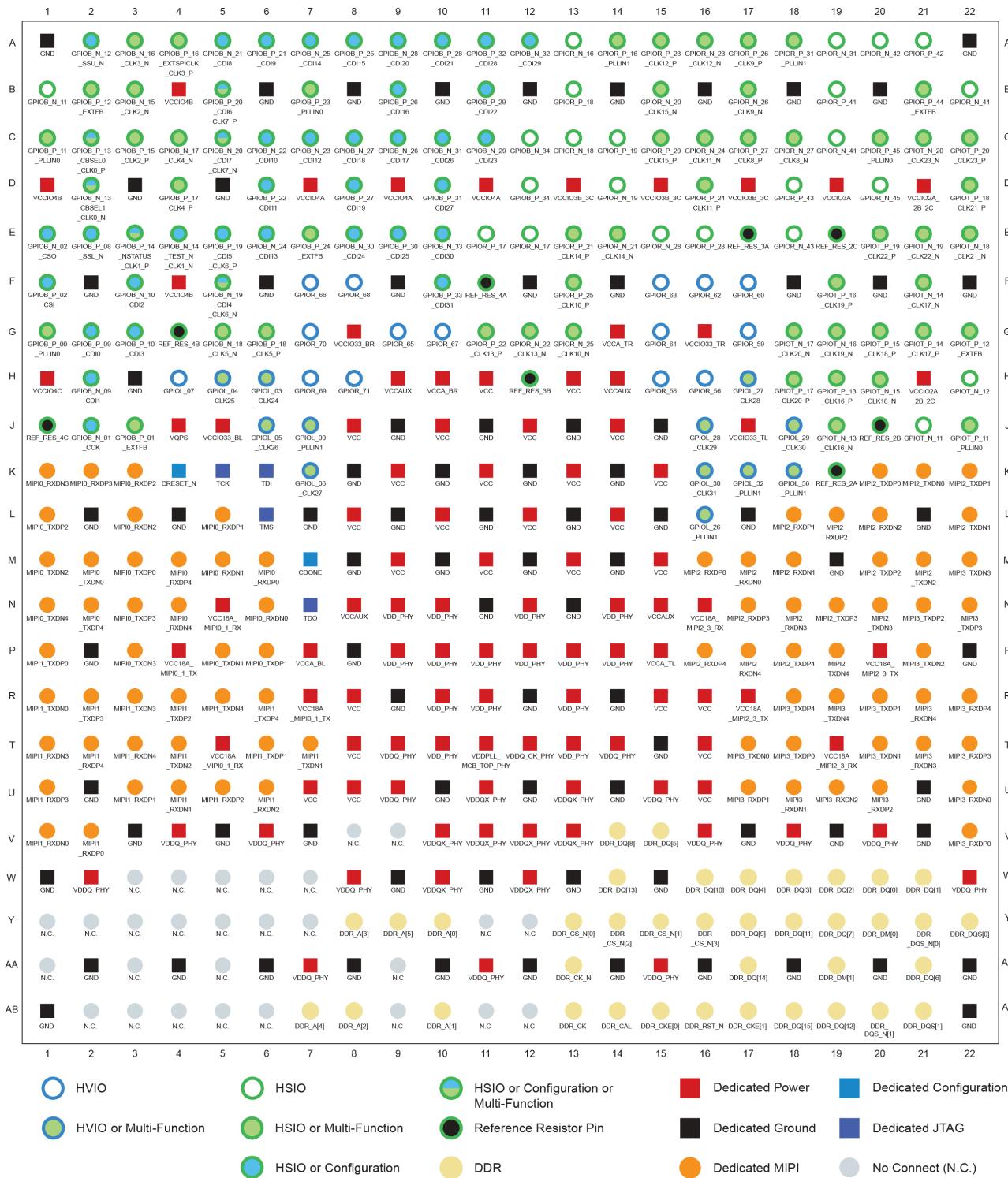


Figure 42: 484-Ball (M) FBGA I/O Bank Diagram

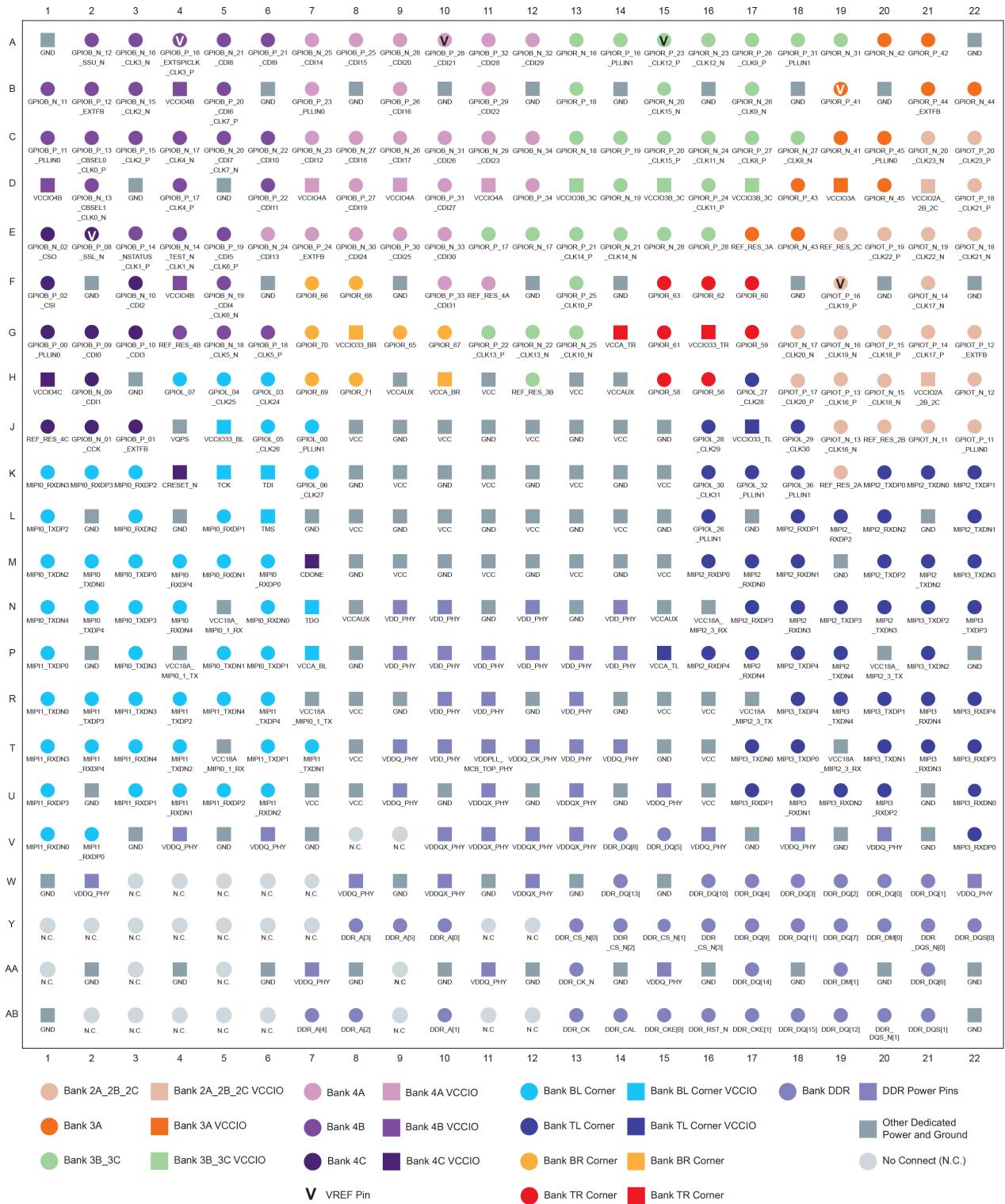


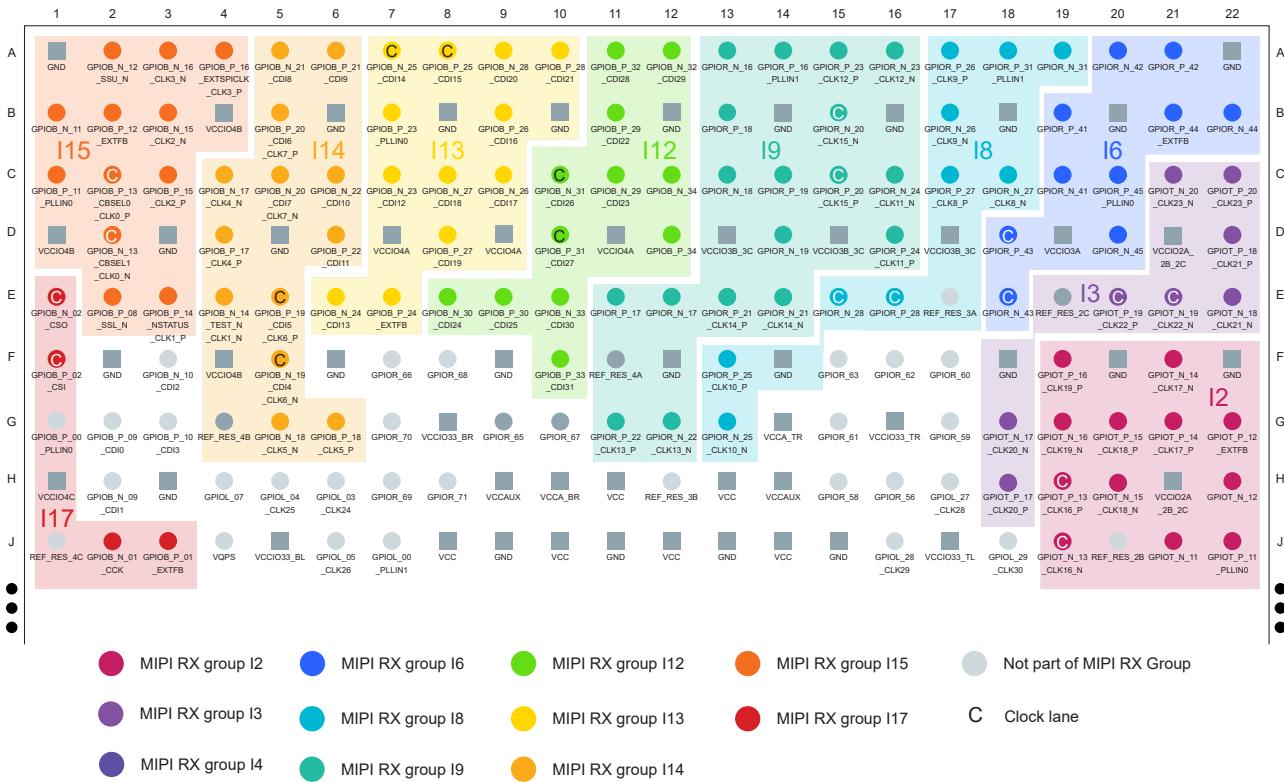
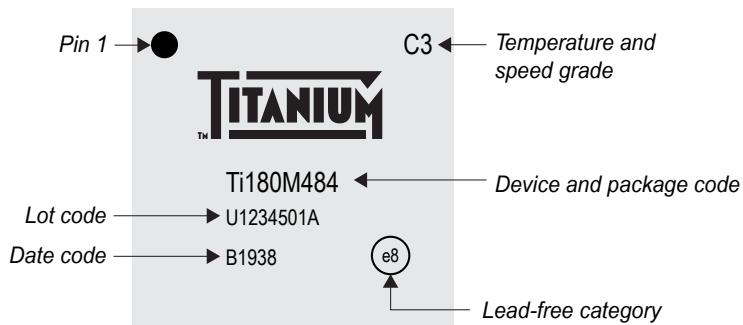
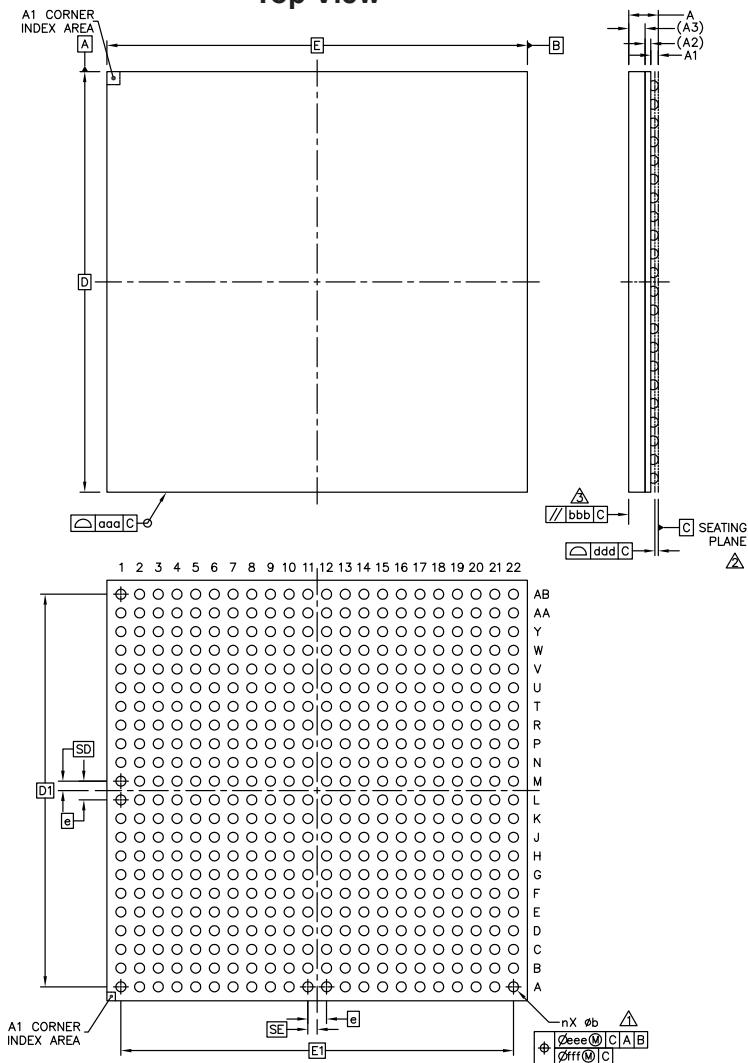
Figure 43: 484-Ball (M) FBGA Emulated MIPI RX Groups**Figure 44: 484-Ball (M) FBGA Package Marking**

Figure 45: 484-Ball (M) FBGA Package Outline

Top View

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2	0.248	REF	
MOLD THICKNESS	A3	0.7	REF	
BODY SIZE	D	18	BSC	
	E	18	BSC	
BALL DIAMETER		0.4		
BALL OPENING		0.35		
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e	0.8	BSC	
BALL COUNT	n	484		
EDGE BALL CENTER TO CENTER	D1	16.8	BSC	
	E1	16.8	BSC	
BODY CENTER TO CONTACT BALL	SD	0.4	BSC	
PACKAGE EDGE TOLERANCE	ooo	0.15		
MOLD FLATNESS	bbb	0.2		
COPLANARITY	ddd	0.15		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.08		

NOTES:

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.

△ DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

△ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Bottom View

529-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

529-Ball (F) FBGA Package Specifications

Figure 46: 529-Ball (F) FBGA Pinout Diagram

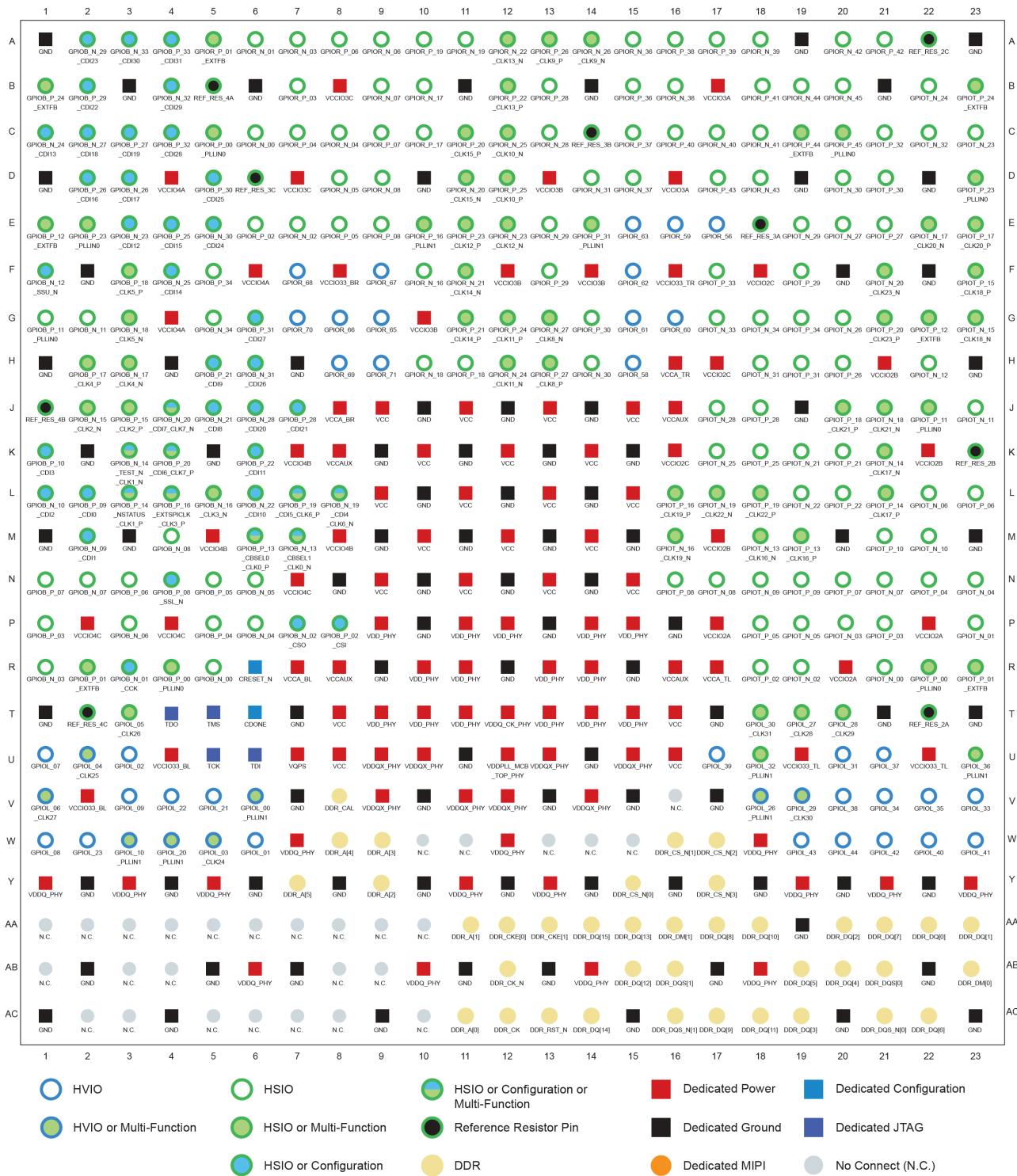


Figure 47: 529-Ball (F) FBGA I/O Bank Diagram

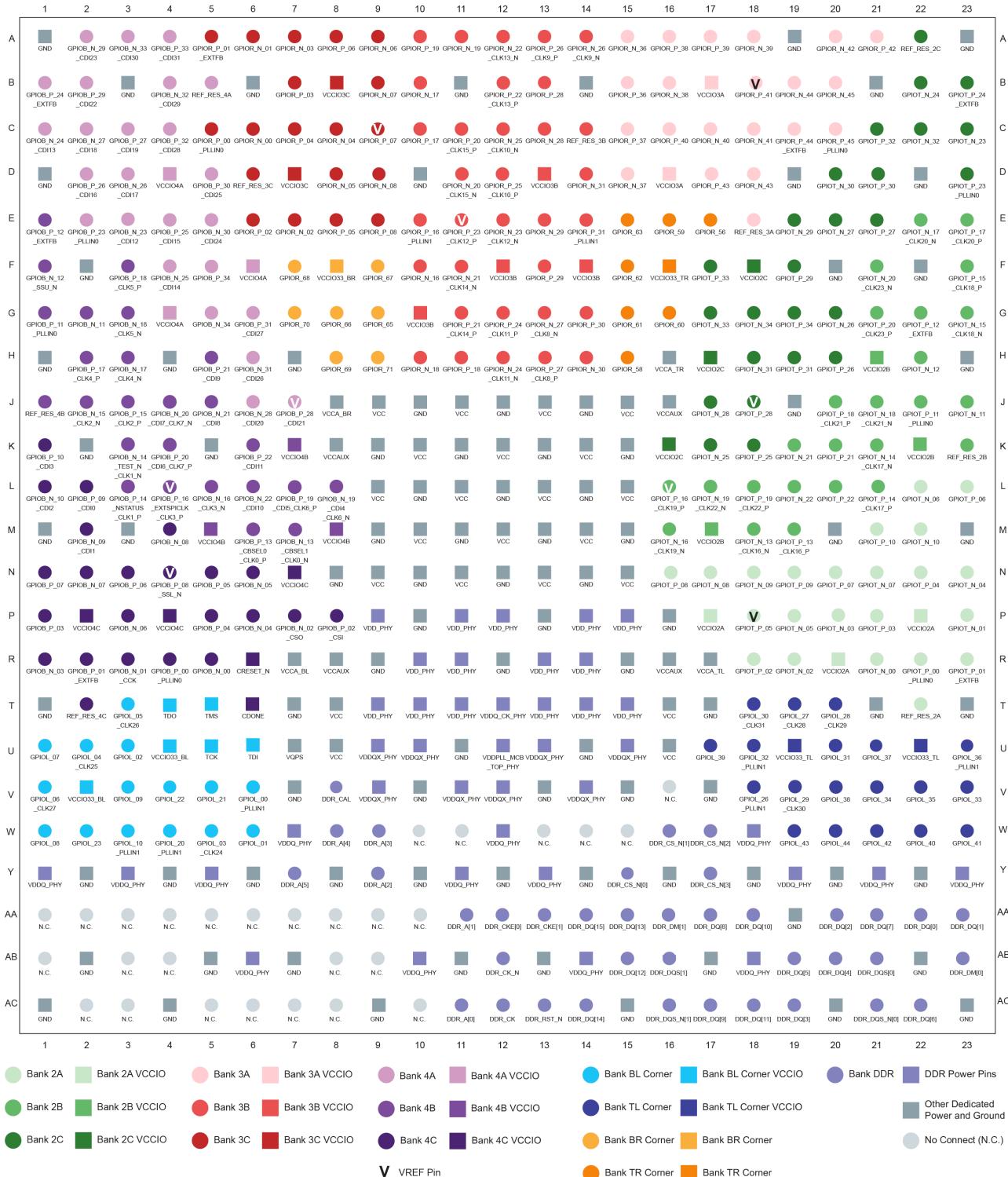


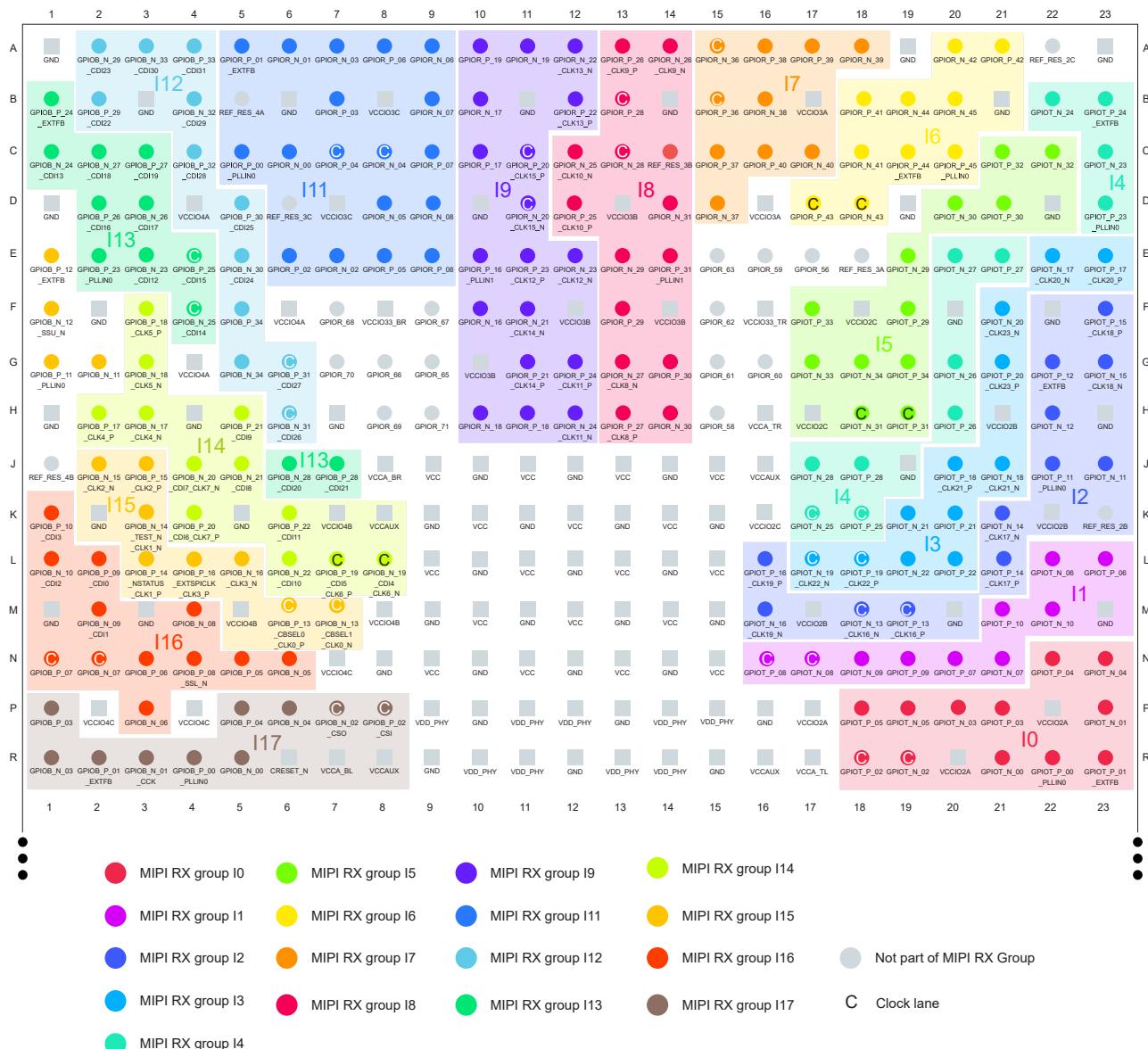
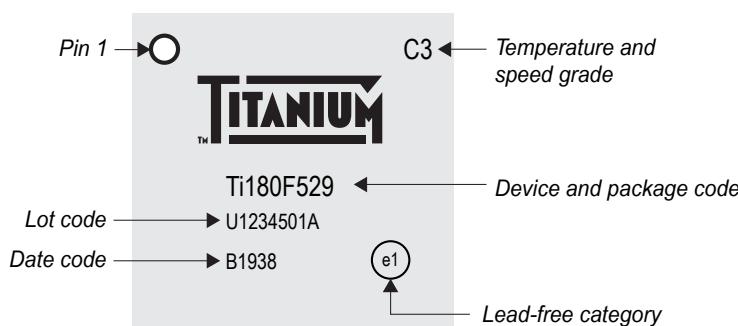
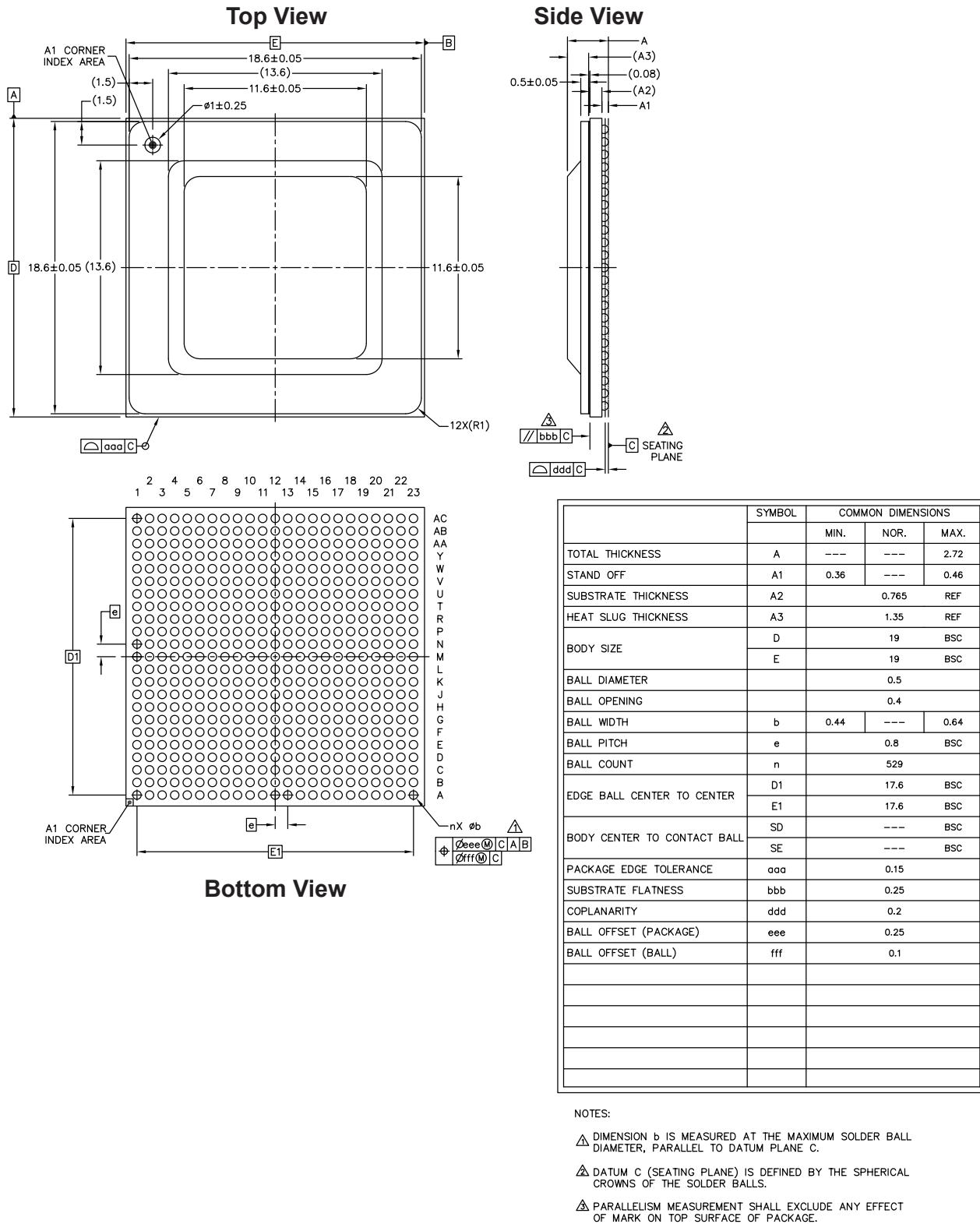
Figure 48: 529-Ball (F) FBGA Emulated MIPI RX Groups**Figure 49: 529-Ball (F) FBGA Package Marking**

Figure 50: 529-Ball (F) FBGA Package Outline



529-Ball (G) FBGA Package Specifications

Figure 51: 529-Ball (G) FBGA Pinout Diagram

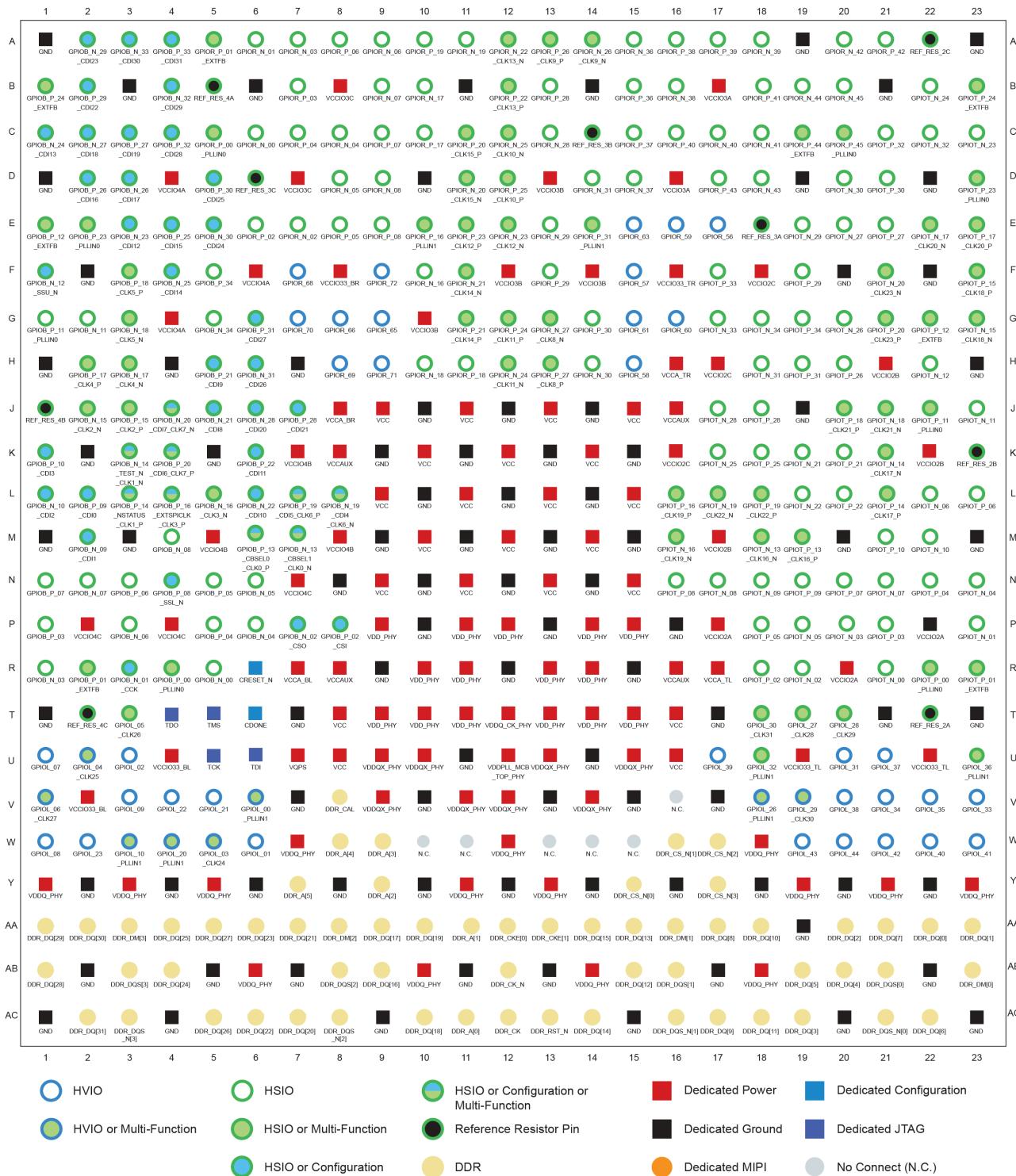


Figure 52: 529-Ball (G) FBGA I/O Bank Diagram

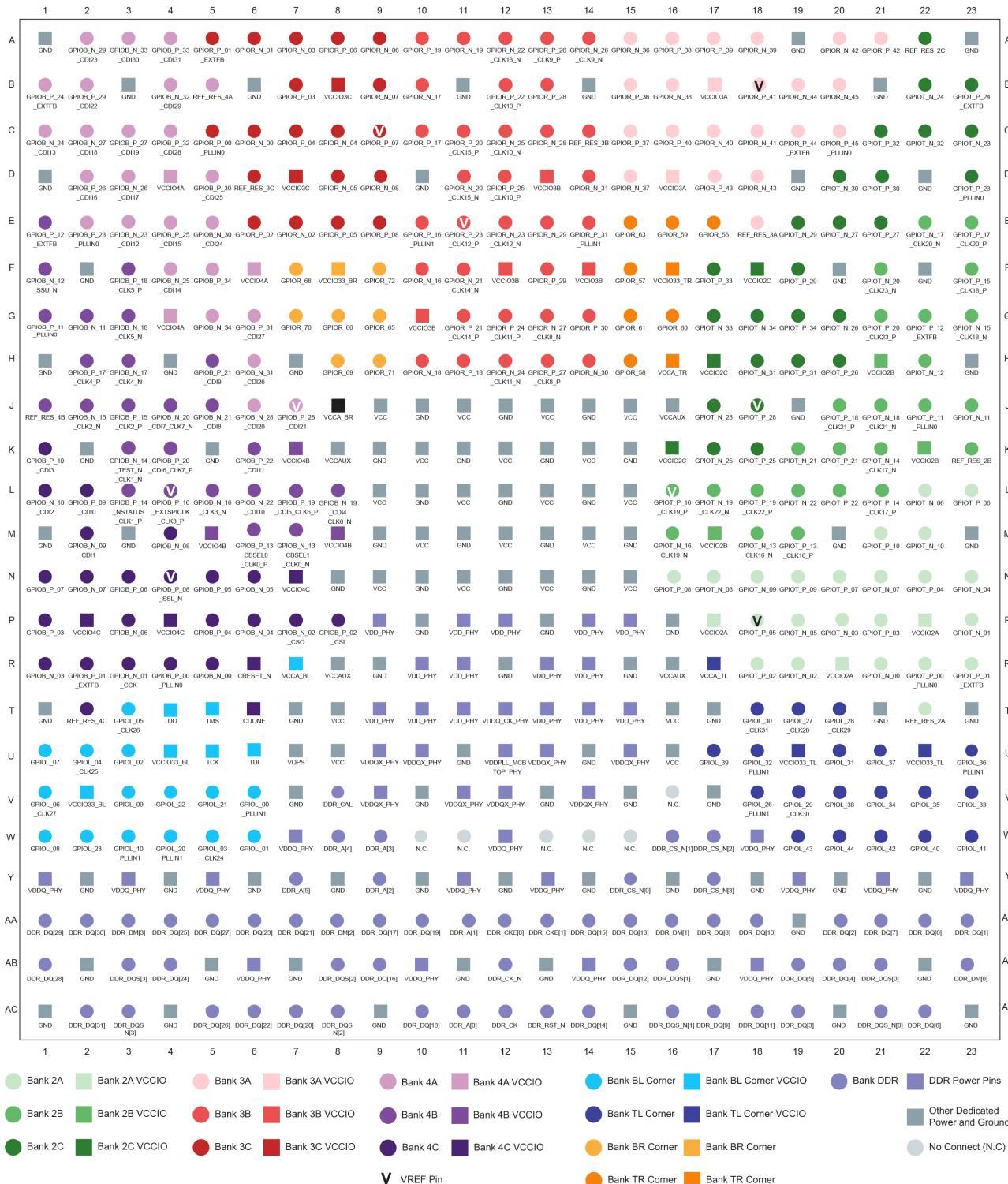


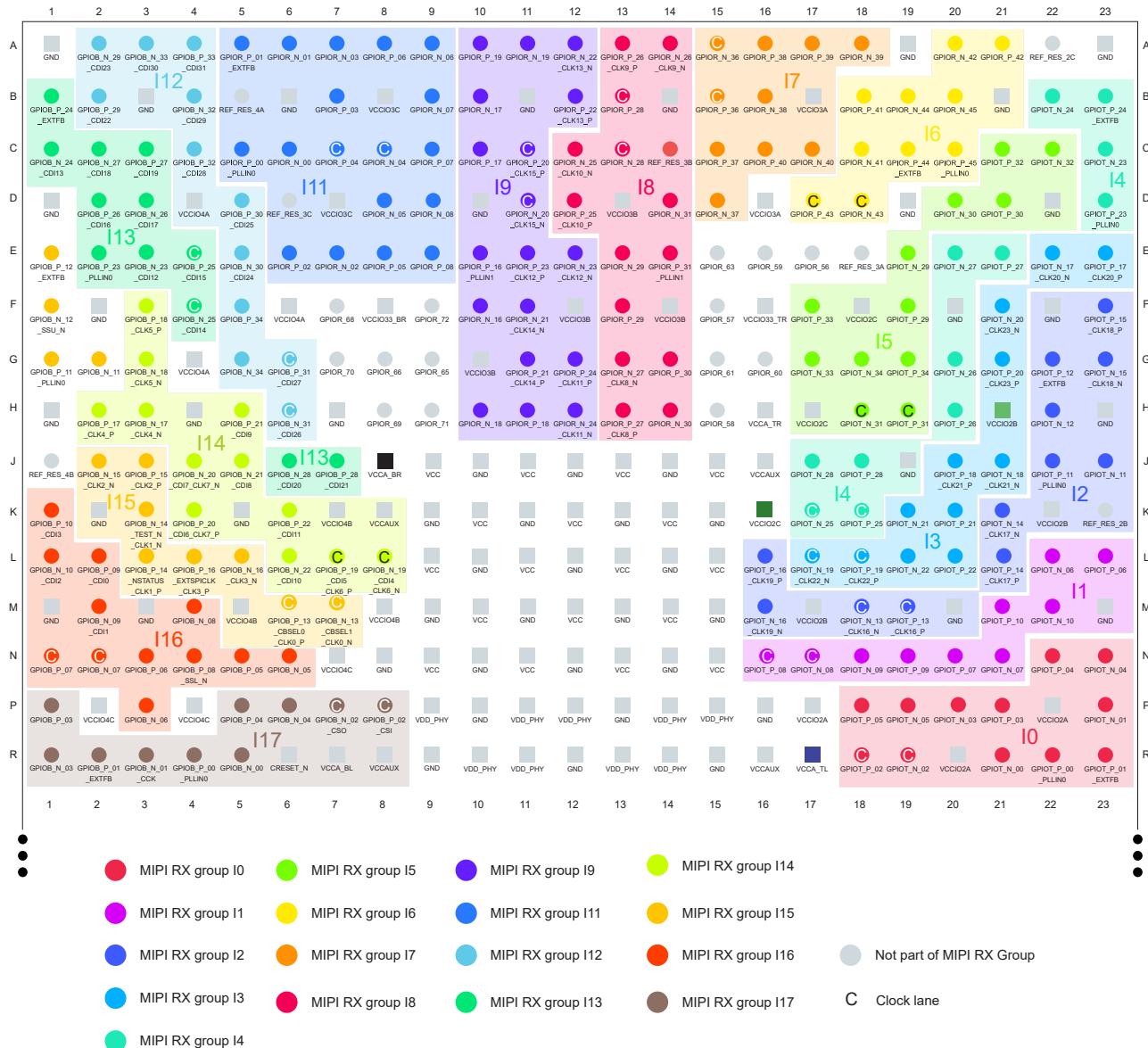
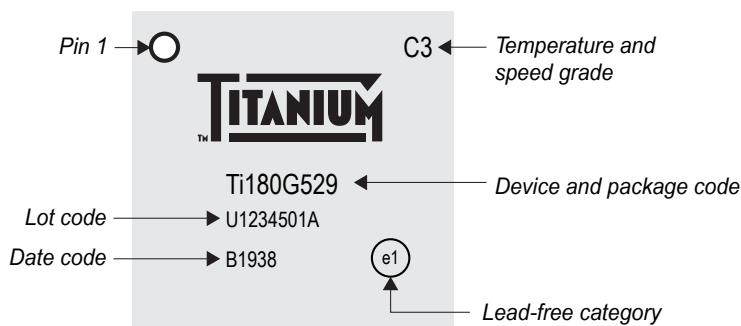
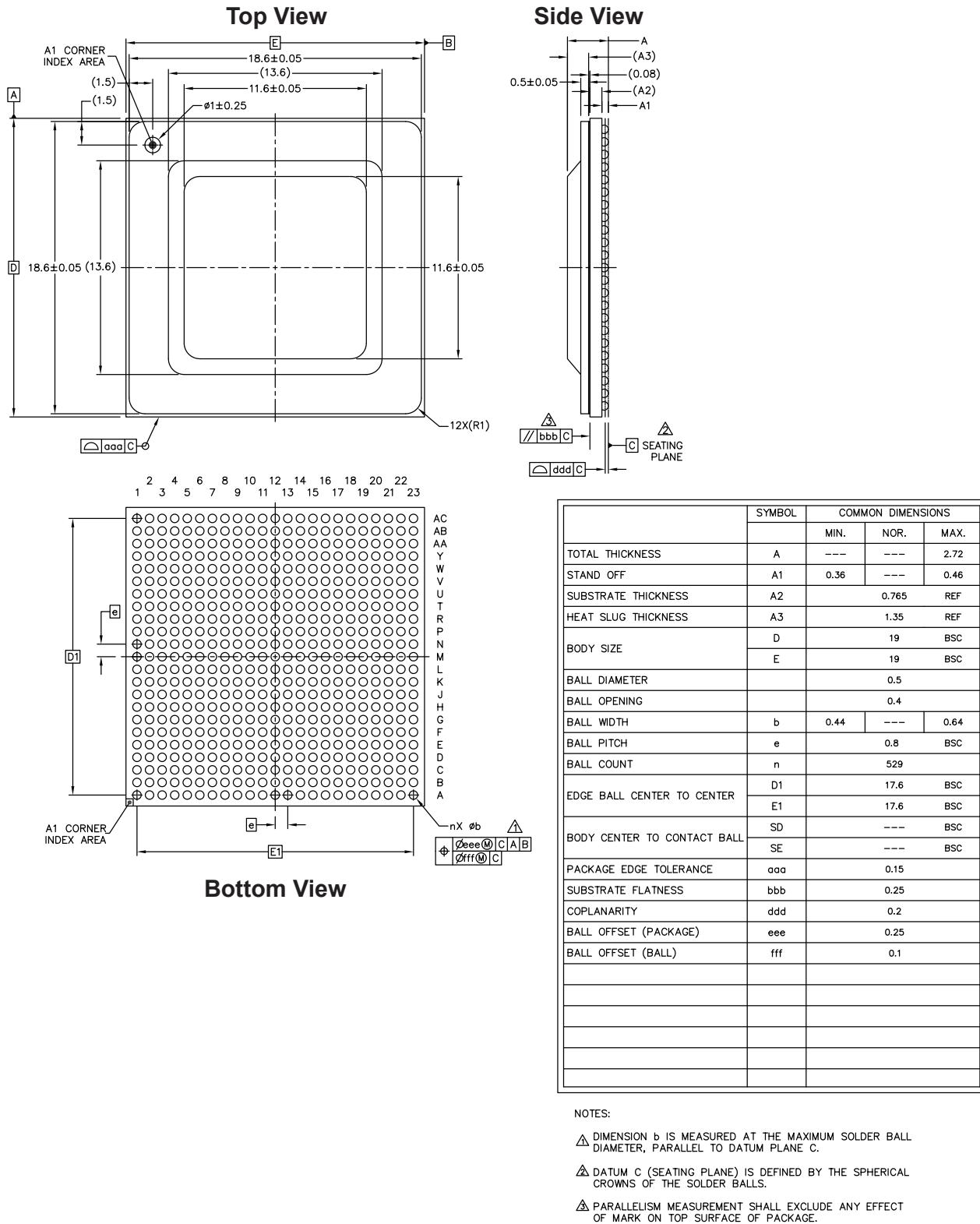
Figure 53: 529-Ball (G) FBGA Emulated MIPI RX Groups**Figure 54: 529-Ball (G) FBGA Package Marking**

Figure 55: 529-Ball (G) FBGA Package Outline



Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for 易灵思® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its profile, which depends upon the board design and the reflow equipment used. You must characterize each PCB to find a reliable profile.

Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

易灵思 does not recommend BGA reballing. Reballed BGA packages void the original 易灵思® specifications.

Peak Reflow Temperatures

Table 9: Peak Reflow Temperature (T_p) by Package

Package	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
WLCSP	1	260
FBGA	3	260



Note: These packages are "green" and RoHS compliant.

Reflow Profile for SMT Packages

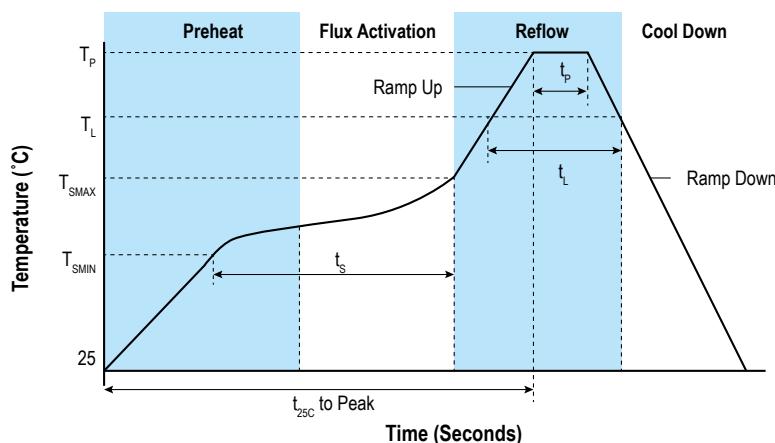
The reflow process usually includes four phases:

1. **Preheat Phase**—The preheat phase brings the assembly from 25 °C to T_S . During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
 - **Solder Ball Spattering**—Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
 - **Bridging**—Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase**—As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase**—The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase**—Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 10: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_p	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
$t_{25C} \text{ to } T_p$	Time from 25 °C to peak temperature	8 minutes maximum

Figure 56: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. 易灵思® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, the proximity of other devices, and user applications. Because of this, 易灵思 FPGAs do not come with preset thermal solutions.

Table 11: Device/Package Thermal Resistance

Measurements taken at 25 °C ambient temperature.

Package	Pitch	Dimensions (mm)	Θ_{JA} (°C/W) Still Air	Θ_{JA} (°C/W) 1 m/s	Θ_{JA} (°C/W) 2 m/s	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
WLCSP64	0.4	3.5 x 3.4	37.24	33.56	32.42	11.95	0.14
F100	0.5	5.5 x 5.5	45.62	41.53	40.14	26.13	20.35
F225	0.65	10 x 10	36.89	33.15	32.03	22.32	11.03
J361, M361	0.65	13 x 13	17.50	14.76	13.85	6.07	2.04
G400	0.8	16 x 16	(6)	(6)	(6)	(6)	(6)
J484, L484, M484	0.8	18 x 18	16.25	13.56	12.70	6.53	3.89
F529, G529	0.8	19 x 19	12.58	10.14	9.20	3.31	1.12

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance
- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

⁽⁶⁾ Pending characterization

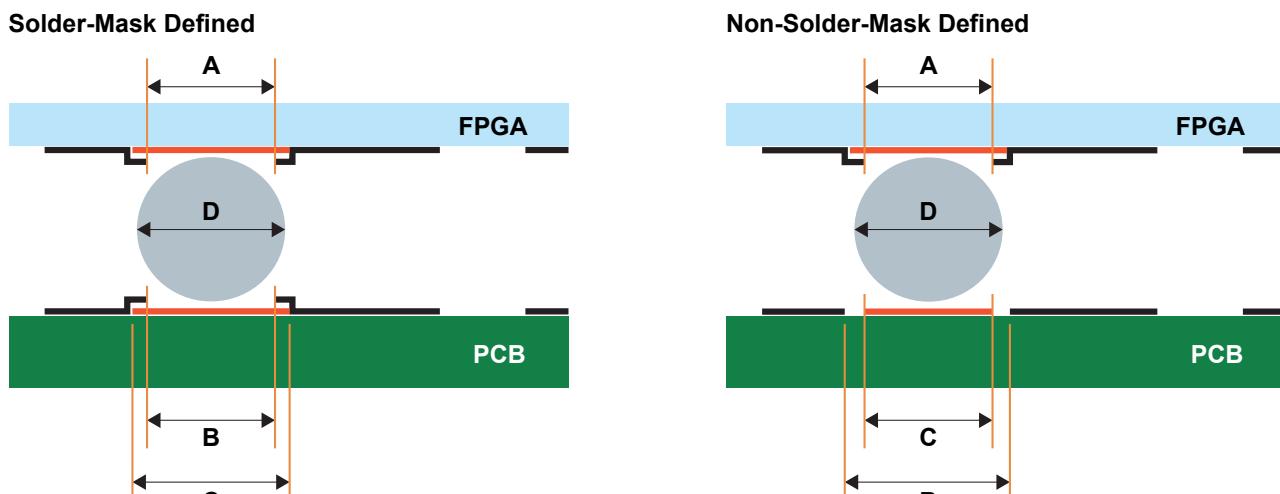
PCB Guidelines for BGA Packages

PCB Solder Pad Guidelines

易灵思 provides solder mask defined (SMD) and non-solder mask defined (NSMD) diameter information. Use this data when creating your board landing pads.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better “grip” area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball.

Figure 57: SMD and Non-SMD Pad Specification



Legend:

A: BGA package solder mask opening
B: Optimum PCB solder mask opening

C: Optimum PCB pad size
D: Solder ball diameter

Table 12: PCB Solder Pad Recommendations

Package	Pitch (mm)	A BGA Package Solder Mask Opening (mm)	SMD		Non-SMD		D Solder Ball Diameter (mm)
			B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	
W64	0.4	N/A	0.2	0.25	0.3	0.2	0.2
F100	0.5	0.25	0.25	0.3	0.35	0.2	0.25
F225	0.65	0.3	0.3	0.35	0.45	0.3	0.35
J361, M361	0.65	0.3	0.3	0.35	0.45	0.3	0.35
G400	0.8	0.35	0.35	0.4	0.5	0.35	0.4
J484, L484, M484	0.8	0.35	0.35	0.4	0.5	0.35	0.4
F529, G529	0.8	0.4	0.4	0.5	0.6	0.4	0.5

Routing between Pads on the Top Layer

You can route signal trace between solder pads on the top layer of the PCB while meeting the clearance requirement.

Figure 58: Routing Traces between Pads on the Top Layer

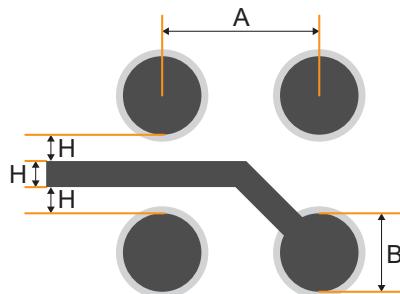


Table 13: Routing Measurements

Measurement	Description	Package							Unit
		W64	F100	F225	J361, M361	G400	J484, L484, M484	F529, G529	
A	Ball pitch.	0.4	0.5	0.65	0.65	0.8	0.8	0.8	mm
	Ball #.	0.2	0.25	0.35	0.35	0.4	0.4	0.5	mm
B	Width of the solder landing pad #. (SMD)	0.25	0.3	0.35	0.35	0.4	0.4	0.5	mm
	Width of the solder landing pad #. (NSMD)	0.2	0.2	0.3	0.3	0.35	0.35	0.4	mm
H (min.)	Minimum space between the trace and the landing pad. (SMD)	(7)	0.06	0.08	0.08	0.1	0.1	0.08	mm
	Minimum space between the trace and the landing pad. (NSMD)	(7)	0.08	0.08	0.08	0.1	0.1	0.08	mm

⁽⁷⁾ The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an “offset via,” is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 59: Via Dimensions

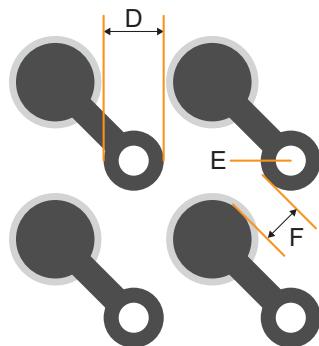


Table 14: Via Measurements

Measurement	Description	Package							Unit
		W64	F100	F225	J361, M361	G400	J484, L484, M484	F529, G529	
D	Via capture pad width.	0.25	0.25	0.3	0.3	0.45	0.45	0.45	mm
E	Finished via #.	0.127	0.127 ⁽⁸⁾	0.15	0.15	0.225	0.225	0.225	mm
F (min.)	Space between the landing pad and via.	(9)	0.072	0.1	0.1	0.1	0.1	0.08	mm

⁽⁸⁾ This is a laser via.

⁽⁹⁾ The via is under the pad, no traces between landing pads.

Routing through Different PCB Layers

You can route a trace between two solder pads, at the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 60: BGA Trace Routing for Top and Second Layers

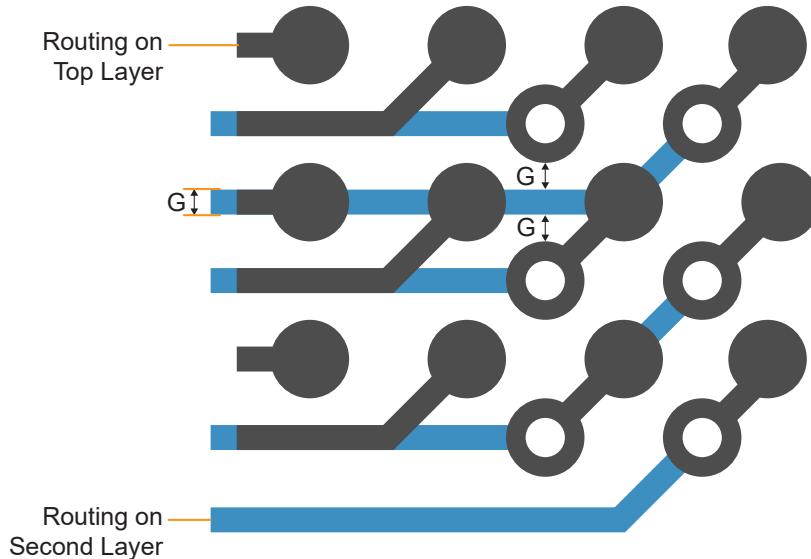


Table 15: Routing Measurements

Measurement	Description	Package							Unit
		W64	F100	F225	J361, M361	G400	J484, L484, M484	F529, G529	
G (min.)	Minimum space required between via and trace.	0.08	0.08	0.08	0.08	0.08	0.08	0.08	mm

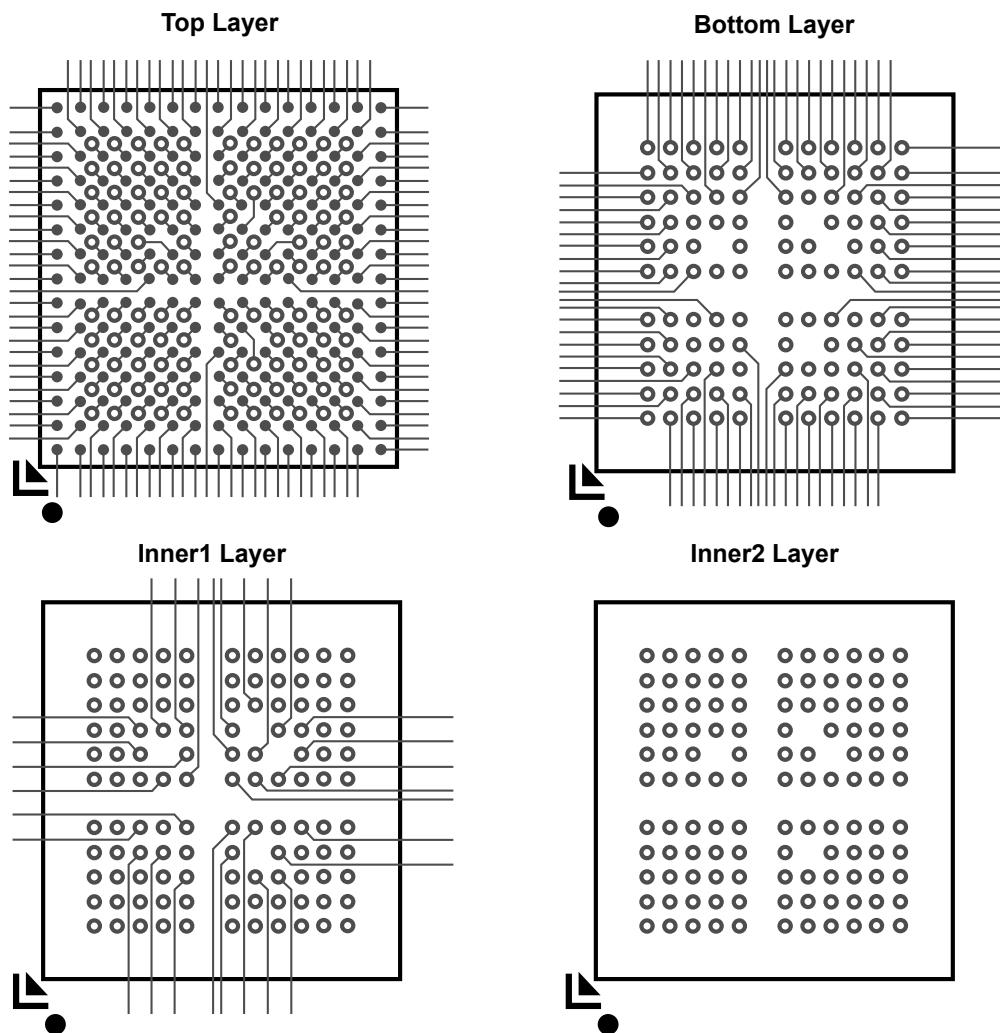
F225 Escape Routing

The following table and figure show how to perform escape routing for the F225 package. These guidelines are one example of acceptable routing using three PCB layers. You can do a different escape routing scheme with a different number of layers. The minimum number of PCB layers is four.

Table 16: 钛金系列 F225 PCB Escape Routing Parameter

Parameter	Specification	Unit
Width of the solder landing pad #	0.35	mm
Width of the solder mask opening #	0.45	mm
Trace width	0.08	mm
Clearance	0.08	mm
Via capture pad width	0.4	mm
Via drill diameter	0.2	mm

Figure 61: 4-Layer 钛金系列 F225 PCB Escape Routing Diagram



Green Packaging

易灵思 FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. 易灵思 refers to these products as "green" packaging.

Tape and Reel Packaging

易灵思 offers WLCSP devices in tape and reel packaging.

Table 17: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
WLCSP64	12	9.5	8	13	2,500

Figure 62: Pin 1 Location (WLCSP64 Packages)

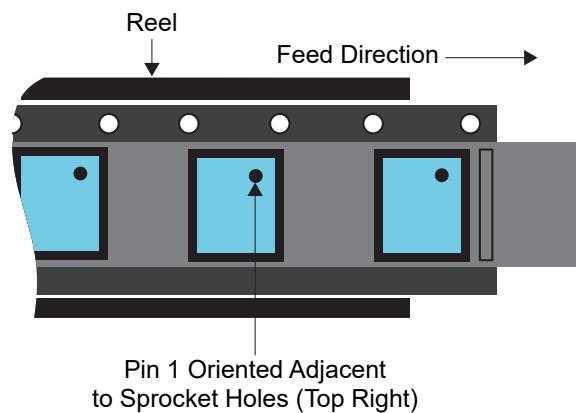
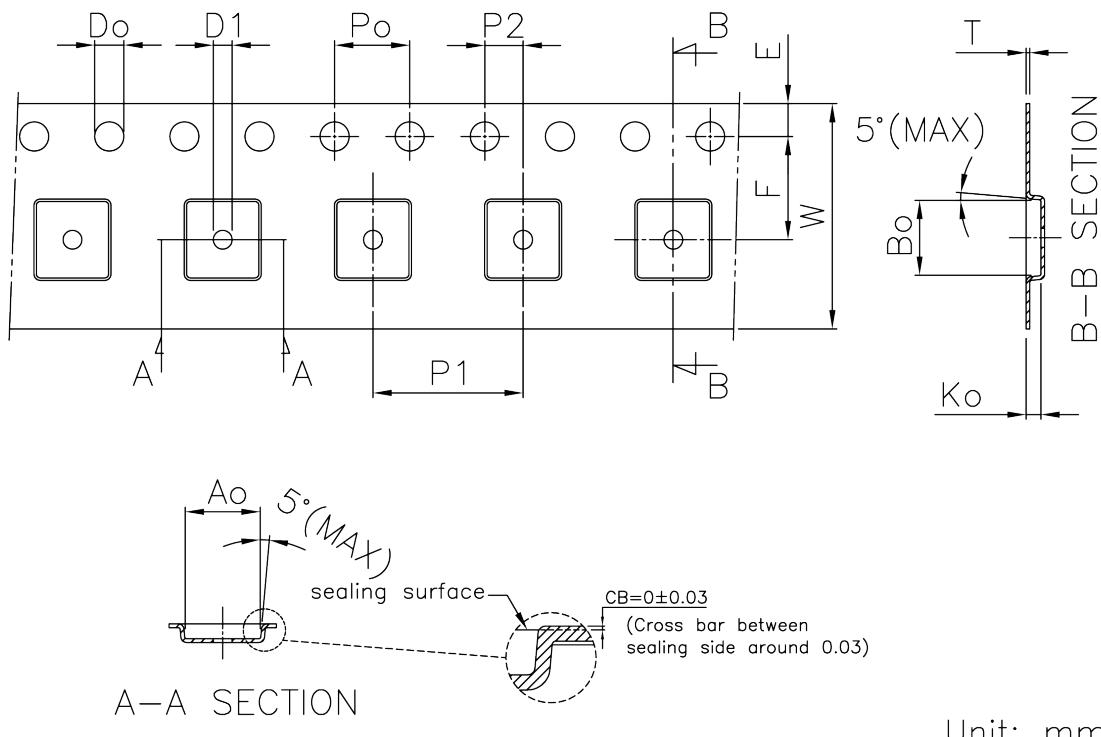


Figure 63: Tape Outline (WLCSP64 Packages)

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.59±0.05	3.75±0.05	0.67±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	1.50 ^{+0.10} ₋₀	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity $\geq 1.0 \times 10^5$ & $\leq 1.0 \times 10^8$ ohm/sq.
7. Tooling type : Male tooling.

Tray Packaging

易灵思 offers BGA devices in tray packaging.

Table 18: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Quantity per Stack
F100	490	14 x 35	10 + 1	4,900
F225	168	8 x 21	10 + 1	1,680
J361, M361	119	7 x 17	10 + 1	1,190
G400	84	6 x 14	10 + 1	840
J484, L484, M484	84	6 x 14	10 + 1	840
F529, G529	60	5 x 12	5 + 1	300

Revision History

Table 19: Revision History

Date	Version	Description
September 2023	5.2	<p>Added package specifications for Ti90, Ti120, and Ti180 G400 package. (DOC-1392)</p> <p>Corrected bank for TDO signal in I/O bank figures for J484, L484, and M484 packages. (DOC-1416)</p> <p>Added thermal resistance information for G529 and J529 packages. (DOC-1426)</p> <p>Updated the lead-free category for 100-ball and 225-ball FPGA Package Marking.</p> <p>Updated table Peak Reflow Temperature (T_p) by Package.</p>
April 2023	5.1	Update the package specification for Ti60 F225 package due to change of thickness. (DOC-1211)
February 2023	5.0	<p>Added J361, J484 and G529 packages. (DOC-1137)</p> <p>Updated REF_RES_3A pin connection requirement in the Pinout Description topic.</p>
December 2022	4.1	<p>Updated pinout and I/O bank figures for M484 and F529 packages. (DOC-1045)</p> <p>Updated configuration pins external weak pull-up requirements. (DOC-1035)</p>
September 2022	4.0	<p>Added F529 package.</p> <p>Updated PCB guidelines.</p> <p>Updated tray packaging.</p>
July 2022	3.0	<p>Added M361 package.</p> <p>Added L484 package.</p> <p>F484 package renamed as M484.</p>
February 2022	2.0	<p>Added F484 package.</p> <p>Updated available package options table.</p>
December 2021	1.2	<p>Updated PCB Solder Pad Recommendations, Routing Measurements, and added PCB Routing Example. (DOC-649)</p> <p>Updated A7 pin name in 64-Ball WLCSP diagrams.</p>
September 2021	1.1	<p>Updated PCB guidelines. (DOC-504)</p> <p>Updated W64 package outline. (DOC-504)</p> <p>Updated available package options.</p>
June 2021	1.0	Initial release.