Trion® T20 MIPI Development Kit User Guide

T20MIPI-DK-UG-v1.9
October 2023
www.elitestek.com

Contents

Introduction

Thank you for choosing the Trion® T20 MIPI Development Kit (part number: YLS_T20MIPI-DK), which allows you to explore the features of the T20 FPGA with a MIPI CSI-2 interface. The kit comes with 3 daughter cards that let you connect MIPI cameras and extend the GPIO.

Warning: The board can be damaged without proper anti-static handling.

What's in the Box?

The Trion® T20 MIPI Development Kit includes:

- Trion® T20 MIPI Development Board preloaded with a demonstration design
- MIPI and LVDS Expansion Daughter Card
- 2 Raspberry Pi Camera Connector Daughter Cards
- 15-pin FFC/FPC cable
- 10 standoffs, 10 screws, and 6 nuts for development board and daughter cards
- 3 foot USB cable (type A to micro type B)

Register Your Kit

When you purchase an 易灵思 development kit, you also receive a license for the Efinity® software plus one year of software upgrades and patches. After the first year you can request a free maintenance renewal. The Efinity® software is available for download from the Support Center.

To download the software, first register at our Support Center (**http://www.elitestek.com/register**) and then register your development kit.

Download the Efinity® Software

To develop your own designs for the T20 device on the board, you must install the Efinity® software. You can obtain the software from the Support Center.

The Efinity® software includes tools to program the device on the board. Refer to the Efinity® Software User Guide for information about how to program the device.

Learn more: Efinity® documentation is installed with the software (see **Help** > **Documentation**) and is also available in the Support Center under Documentation.

Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
```

Note: If your board was connected to your computer before you executed these commands, you need to disconnect and re-connect it.

Installing the Windows USB Drivers

Note: If you have another 易灵思 board and are using the Trion® T20 MIPI Development Board, you must manage drivers accordingly. Refer to AN 050: Managing Windows Drivers for more information.

On Windows, you use software from Zadig to install drivers. Download the Zadig software (version 2.7 or later) from **zadig.akeo.ie**. (You do not need to install it; simply run the downloaded executable.)

To install the driver:

1. Connect the board to your computer with the appropriate cable and power it up.
2. Run the Zadig software.

   Note: To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

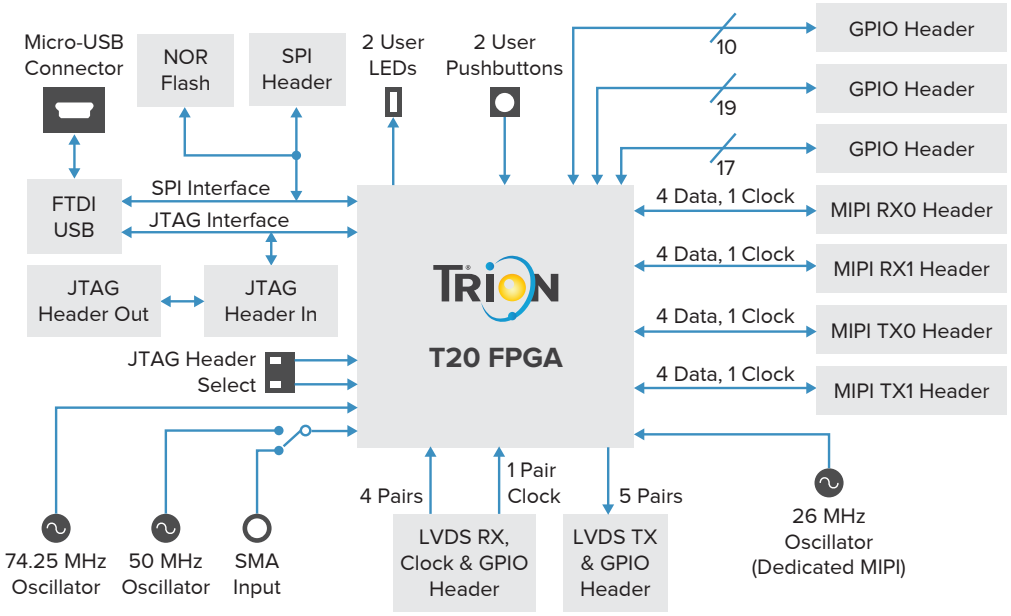
3. Choose **Options** > **List All Devices**.
4. Repeat the following steps for each interface. The interface names end with (Interface N), where N is the channel number.
   - Select **libusb-win32** in the **Driver** drop-down list.
   - Click **Replace Driver**.
5. Close the Zadig software.

Note: This section describes how to install the libusb-win32 driver for each interface separately. If you have previously installed a composite driver or installed using libusbK drivers, you do not need to update or reinstall the driver. They should continue to work correctly.

Board Functional Description

The Trion® T20 MIPI Development Board contains a variety of components to help you build designs for the Trion® T20 device.

Figure 1: Trion® T20 MIPI Development Board Block Diagram



Features

- 易灵思® T20F169C4 device in an 169-ball FineLine BGA package with MIPI CSI-2 interface
- FTDI FT2232H dual-channel chipset with USB controller
- Winbond 32 Mbit SPI NOR flash memory
- Micro-USB type B receptacle
- Designed to accommodate up to 6 daughter cards
  - Four MIPI high-speed connectors to attach 易灵思 camera connector daughter cards
  - Two LVDS high-speed headers to attach the 易灵思 GPIO daughter card
- Two 22-pin GPIO headers that support user functions or an off-the-shelf SDRAM module
- One 12-pin GPIO header
- User inputs:
  - 2 LEDs on T20F169C4 bank 1B for user outputs
  - 2 pushbutton switches (connected to bank 1B I/O pins)
- 50 MHz and 74.25 MHz oscillators for T20F169C4 PLL input
- Optional 3.3 V external clock source available through SMA input to drive the T20F169C4 PLL input or clock input pin
- Power:
  - Power source: 5 V 4 A power supply or USB 5 V, 500 mA USB (for low-power consumption designs)
  - Two on-board switching regulators (maximum at 1.2 A) source 3.3 V and 1.2 V components; three on-board dropout regulators (maximum at 500 mA) source 2.8 V, 2.5 V, and 1.8 V components
  - Fixed 3.3 V VCCIO for T20F169C4 I/O banks 1B, 3A, 3C, 3E, 4A, and 4B

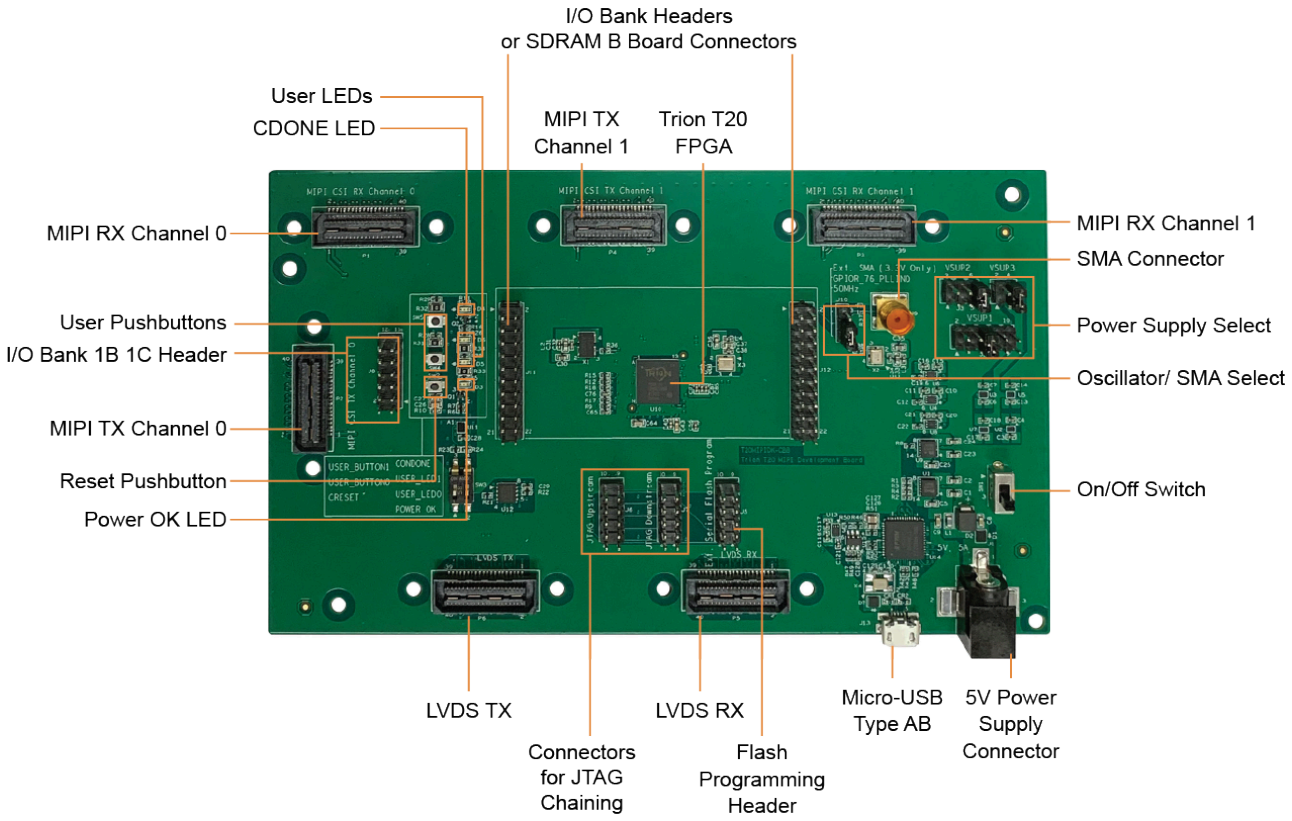
  - Fixed 1.8 V VCCIO for T20F169C I/O banks 1E
  - Optional header for camera power supply with power on sequence
  - Optional header for daughter card power supply
- Power good and T20F169C4 configuration done LEDs

Overview

The board features the 易灵思® T20 programmable device in a 169-ball FBGA package, which is fabricated using 易灵思® Quantum® technology. The Quantum®-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. T20 devices also include embedded memory blocks and multiplier blocks (or DSP blocks). You create designs for the T20 device in the Efinity® software, and then download the resulting configuration bitstream to the board using the USB connection.

Learn more: For more information on T20 FPGAs, refer to the T20 Data Sheet.

Figure 2: Trion® T20 MIPI Development Board Components



The Trion® T20 MIPI Development Board provides four 0.8 mm high-speed ground plane sockets for the MIPI CSI-2 interface and two 0.8 mm high-speed ground plane sockets for the LVDS transmitters and receivers. Additionally, you can connect an SDRAM board (B) module to the two 22-pin GPIO headers to add a 200 MHz, 64 MB SDRAM memory.

The FTDI FT2232H module has two channels to support SPI (FTDI interface 0) and JTAG (FTDI interface 1) configuration. It receives the T20 configuration bitstream from a USB host and writes to the on-board SPI NOR flash memory. After a reset in SPI passive mode, the FTDI controller can also write the configuration bitstream directly to the FPGA. Additionally, it supports direct JTAG programming mode in which it writes the configuration bitstream directly to the FPGA through the JTAG interface.

Learn more: Refer to AN 006 Configuring Trion FPGAs for more information.

The SPI NOR flash memory stores the configuration bitstream it receives from the FTDI FT2232H module. The T20 device accesses this configuration bitstream when it is in active configuration mode (default).

You can chain multiple Trion® T20 MIPI Development Board together using the board's JTAG headers. Refer to **Connecting Multiple Boards in a JTAG Chain** on page 28 for more information.

Note: Although the Trion® T20 MIPI Development Board has a different power-up sequence, you should follow the power-up sequence in the T20 Data Sheet when designing your own board. For improved reliability, 易灵思® recommends that you use supervisor IC at `CRESET_N` explained in AN 006 Configuring Trion FPGAs.

The board's main power supply is the 5 V DC input. You must use your own DC power supply to provide the board with power through the 5 V input jack. The recommended power input is a 5 V (4 A minimum) DC power source. You can also power the board through the micro USB port for designs with low power consumption (< 500 mA).

The board regulates down the 5 V DC input using on-board switching regulators to provide the necessary voltages for the T20 device, MIPI camera, SPI flash memory, SDRAM and on-board oscillator.

Learn more: Refer to the Trion® T20 MIPI Development Board Schematics and BOM for more information about the components used in the Trion® T20 MIPI Development Board.

Power On

To turn on the development board, turn on switch SW1. Upon power-up, the 5 V DC power supply or micro-USB power is input to the on-board regulators through 5 V input jack (CON1) to generate the required 3.3 V, 2.8 V, 2.5 V, 1.8 V, and 1.2 V for components on the board. When these voltages are up and stable, the board asserts a **POWER OK** signal (pulled high) from the components' respective regulators. When the board asserts the **POWER OK** signal, a green LED (D3) turns on, giving you a visual confirmation that the power supplies on the board are up and stable.

Note: The micro-USB power supply powers up the board with limited current. 易灵思 recommends that you use an external DC 5 V DC supply if your user design requires high power.

Reset

The T20F169C4 device is typically brought out of reset with the CRESET signal. Upon power up, the T20F169C4 device is held in reset until CRESET toggles high-low-high.

Note: You can manually assert the high-low-high transition with pushbutton switch SW2.

CRESET has a pull-up resistor. When you press SW2, the board drives CRESET low; when you release SW2, the board drives CRESET high. Thus, a single press of SW2 provides the required high-low-high transition.

After toggling CRESET, the T20F169C4 device goes into configuration mode and reads the device configuration bitstream from the flash memory. When configuration completes successfully, the device drives the CDONE signal high. CDONE is connected to a green LED (D4), which turns on when the T20F169C4 device enters user mode.

Clock Sources

Three on-board oscillators, 26 MHz, 50 MHz, and 74.25 MHz, are available to drive the T20F169C4 PLL input pin and clock input. Alternatively, you can disable the 50 MHz oscillator and use an external clock source through the SMA input (J9). Set jumper J10 to use the 50 MHz or SMA input as the clock source.

Table 1: Oscillator Clock Sources

Clock Source	PLL Input Pin
26 MHz oscillator (dedicated MIPI clock source)	GPIOR_81_MREFCLK
50 MHz oscillator or 3.3 V SMA input	GPIOR_76_PLLIN0
74.25 MHz oscillator	GPIOL_75_PLLIN1

You can supply a clock to the PLL or clock network in the FPGA through a board header.

Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 2: Trion® T20 MIPI Development Board Headers

Reference Designator	Description
J1	5 V DC power supply input jack
J13	Micro-USB Type-AB receptacle
P1	40-pin connector for MIPI CSI-2 channel 0 receiver, 1.8 V GPIO, and power supply
P2	40-pin connector for MIPI CSI-2 channel 0 transmitter, 1.8 V and 3.3 V GPIO, and power supply
P3	40-pin connector for MIPI CSI-2 channel 1 receiver, 1.8 V GPIO, and power supply
P4	40-pin connector for MIPI CSI-2 channel 1 transmitter, 1.8 V and 3.3 V GPIO, and power supply
P5	40-pin high-speed connector for LVDS receiver (RX) and GPIO
P6	40-pin high-speed connector for LVDS transmitter (TX) and GPIO
J2	User selectable supply with or without power up sequence (5.0 V, 3.3 V, and 2.8 V)
J3	User selectable supply with or without power up sequence (3.3 V and 1.8 V)
J4	User selectable supply with or without power up sequence (1.2 V)
J5	External SPI NOR flash programming header
J6	JTAG header in (to T20 FPGA)
J7	JTAG header out (from T20 FPGA)
J8	12-pin header for I/O banks 1B and 1E
J9	SMA connector for external 3.3 V clock source input
J10	3-pin header to select whether to use the on-board 50 MHz oscillator or SMA input from external clock source
J11, J12	22-pin I/O bank headers

Header J1 (5 V Power)

J1 is a 5 V DC power supply input jack. J1 supplies power to regulators on the board that power the T20F169C4 FPGA. The maximum current supply to this input jack is 4 A.

Header J13 (USB Power)

J13, a micro-USB type B socket, is the interface between the board and your computer for power and communication. Connect the micro-USB cable for configuring T20F169C4 FPGA and NOR flash. The board supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode. The USB cable provides a maximum of 500 mA.

Headers P1 and P3 (MIPI Receiver Channels 0 and 1)

P1 and P3 are dedicated MIPI CSI-2 receiver high-speed interface connectors that support 1 clock lane and 4 data lanes. P1 and P3 also include optional supply pins VSUP1, VSUP2, VSUP3, as well as five 1.8 V GPIO pins. You can use these connectors to attach a camera connector daughter card.

Table 3: MIPI Receiver Channel 0 (P1) and Channel 1 (P3)

where x is 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPIx_RXD_P0	Differential MIPI Receiver Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPIx_RXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPIx_RXD_P1	Differential MIPI Receiver Channel Lane 1
9	NC		10	MIPIx_RXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPIx_RXD_P2	Differential MIPI Receiver Channel Lane 2
15	NC		16	MIPIx_RXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPIx_RXD_P3	Differential MIPI Receiver Channel Lane 3
21	NC		22	MIPIx_RXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPIx_RXD_P4	Differential MIPI Receiver Channel 0 Lane 4
27	NC		28	MIPIx_RXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	GPIOL_69_1V8_SCL[1]	1.8 V GPIO
33	NC		34	GPIOL_70_1V8_SDA[1]	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	GPIOL_71_1V8	1.8 V GPIO
39	GPIOL_73_REFCLK(P1) GPIOL_74_REFCLK(P3)	1.8 V GPIO	40	GPIOL_72_1V8	1.8 V GPIO

[1] The SCL and SDA pins are used for MIPI Camera Command Set (CSS) transactions.

Headers P2 and P4 (MIPI Transmitter Channels 0 and 1)

P2 and P4 are dedicated MIPI CSI-2 transmitter high-speed interface connectors that support 1 clock lane and 4 data lanes. P2 and P4 also include optional supply pins VSUP1, VSUP2, VSUP3, as well as one 3.3 V GPIO pin and four 1.8 V GPIO pins. You can use these connectors to attach a camera connector daughter card.

Table 4: MIPI Transmitter Channel 0 (P2) and Channel 1 (P4)

where x is 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPIx_TXD_P0	Differential MIPI Transmitter Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPIx_TXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPI1_TXD_P1	Differential MIPI Transmitter Channel Lane 1
9	NC		10	MIPI1_TXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPI1_TXD_P2	Differential MIPI Transmitter Channel Lane 2
15	NC		16	MIPI1_TXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPI1_TXD_P3	Differential MIPI Transmitter Channel Lane 3
21	NC		22	MIPI1_TXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPI1_TXD_P4	Differential MIPI Transmitter Channel Lane 4
27	NC		28	MIPI1_TXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	GPIOL_69_1V8_SCL(1)	1.8 V GPIO
33	NC		34	GPIOL_70_1V8_SDA(1)	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	GPIOL_71_1V8	1.8 V GPIO
39	GPIOL_12_3V3(P2) GPIOL_13_3V3(P4)	3.3 V GPIO	40	GPIOL_72_1V8	1.8 V GPIO

Headers P5 and P6 (LVDS)

P5 and P6 contain the LVDS signals. P5 has 4 dedicated LVDS RX channels, and one dedicated LVDS RX clock with 3.3 V and 1.8 V GPIO. P6 has 5 dedicated LVDS TX channels with 3.3 V and 1.8 V GPIO. You can also use LVDS pins as GPIO.

Learn more: Refer to the Trion Interfaces User Guide for instructions on using the LVDS pins as GPIO.

Table 5: P5 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOB_CLKP0	Dedicated LVDS RX clock	2	NC	No Connect
3	GPIOB_CLKN0		4	NC	
5	GND	Ground	6	GND	Ground
7	GPIOB_RXP00	Dedicated LVDS RX Channel 00	8	NC	No Connect
9	GPIOB_RXN00		10	NC	
11	GND	Ground	12	GND	Ground
13	GPIOB_RXP01	Dedicated LVDS RX Channel 01	14	NC	No Connect
15	GPIOB_RXN01		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOB_RXP02	Dedicated LVDS RX Channel 02	20	NC	No Connect
21	GPIOB_RXN02		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOB_RXP03	Dedicated LVDS RX Channel 03	26	NC	No Connect
27	GPIOB_RXN03		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOL_12	3.3 V GPIO	32	VSUP1	User selectable supply 1
33	GPIOL_13	3.3 V GPIO	34	VSUP2	User selectable supply 2
35	GND	Ground	36	GND	Ground
37	GPIOL_20	3.3 V GPIO	38	GPIOL_73	1.8 V GPIO
39	GPIOL_21	3.3 V GPIO	40	GPIOL_74	1.8 V GPIO

Table 6: P6 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	User selectable supply 1	2	GPIOL_69	1.8 V GPIO
3	VSUP2	User selectable supply 2	4	GPIOL_70	1.8 V GPIO
5	GND	Ground	6	GND	Ground
7	GPIOB_TXP00	Dedicated LVDS TX Channel 00	8	NC	No Connect
9	GPIOB_TXN00		10	NC	
11	GND	Ground	12	GND	Ground
13	GPIOB_TXP01	Dedicated LVDS TX Channel 1	14	NC	No Connect
15	GPIOB_TXN01		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOB_TXP02	Dedicated LVDS TX Channel 02	20	NC	No Connect
21	GPIOB_TXN02		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOB_TXP03	Dedicated LVDS TX Channel 03	26	NC	No Connect
27	GPIOB_TXN03		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOL_12	3.3 V GPIO	32	GPIOL_71	1.8 V GPIO
33	GPIOL_13	3.3 V GPIO	34	GPIOL_72	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	GPIOB_TXP05	Dedicated LVDS TX Channel 05	38	NC	No Connect
39	GPIOB_TXN05		40	NC	

Header J2 (Voltage Supply 1)

J2, J3, and J4 are headers you use to select the voltage and/or power up sequence option. Use a jumper across 2 pins to make your selection.

- J2 controls the voltage (5.0, 3.3, and 2.8) for the 4 MIPI headers and 2 LVDS headers
- J3 controls the voltage (3.3 and 1.8) for the 4 MIPI headers and 2 LVDS headers
- J4 controls the voltage (1.2) for the four MIPI headers

Table 7: Voltage Selection for J2, J3, and J4

Jumper	VSUP1 (J2)	VSUP2 (J3)	VSUP3 (J4)
Connect pins 1 and 2	5.0 V	3.3 V	1.2 V
Connect pins 3 and 4	3.3 V	1.8 V	1.2 V with power up sequence (default)
Connect pins 5 and 6	3.3 V with power up sequence	1.8 V with power up sequence (default)	–
Connect pins 7 and 8	2.8 V	–	–
Connect pins 9 and 10	2.8 V with power up sequence (default)	–	–

Warning: For each header, only select one voltage at a time; otherwise you may damage the board.

Header J5 (SPI)

J5 is a SPI interface that you can use to configure the on-board NOR flash or T20F169C4 FPGA.

Table 8: J5 Pin Assignments

Pin Number	Signal Name	Description	Signal Name
1	SPI_CLK	SPI configuration clock	GPIOL_01_CCK
2	CRESET	Configuration reset pin (active low)	CRESET_B
3	SPI_MOSI	SPI serial data output	GPIOL_08_CDI0
4	CDONE	Configuration done status pin	CONDONE
5	SPI_MISO	SPI serial data input	GPIOL_09_CDI1
6	HOLD	SPI hold pin (active low)	–
7	SPI_SS	SPI slave select pin (active low)	GPIOL_00_SS
8	3V3	3.3 V power supply	–
9	FTDI_RST	Reset pin for on board FTDI FT2232 chipset (active low)	–
10	GND	Ground	–

Headers J6 and J7 (JTAG)

Headers J6 and J7 are the JTAG interfaces for configuration or boundary scan testing.

- J6 is the JTAG connection to the T20F169C4 FPGA.
- J7 is the JTAG connection from the T20F169C4.

Note: Refer to **Connecting Multiple Boards in a JTAG Chain** on page 28 for information on how to chain multiple boards using the JTAG headers.

Table 9: J6 and J7 Pin Assignments

Pin Number	J6 Signal Name	Description	J7 Signal Name	Description
1	TDO_FTDI	JTAG data output signal	TDO_FTDI	JTAG data input signal
2	3.3V	3.3 V power supply	3.3V	3.3 V power supply
3	TCK	JTAG data clock	TCK	JTAG data clock
4	TDI	JTAG data input	TDO_EXT	JTAG data output
5	TMS	JTAG TMS mode select	TMS	JTAG TMS mode select
6	FTDI_RST	Reset pin for on-board FTDI FT2232 module (active low)	GND	Ground
7	SPI_SS	Slave select signal	SPI_SS	Slave select signal
8	CRESET	Configuration reset pin (active low)	CRESET	Configuration reset pin (active low)
9	GND	Ground	GND	Ground
10	GND	Ground	GND	Ground

Headers J8, J11, and J12 (GPIO)

The board headers J8, J11, and J12 contain GPIO pins.

- J8 is a 12-pin header that connects to GPIO pins in banks 1B and 1E.
- J11 and J12 are 22-pin headers that connect to GPIO pins in banks 1B, 3A, 3C, 3E, 4A, and 4B. The VCCIO is fixed at 3.3 V.

J11 and J12 also allow you to connect an SDRAM board (B) accessory board. Refer to **Attaching Camera Connector Daughter Cards** on page 26 for more information.

Table 10: J8 Pin Assignments

Pin Number	Signal Name	DDIO Mode Supported	Pin Number	Signal Name	DDIO Mode Supported
1	GPIOL_12	Yes	2	GPIOL_13	Yes
3	GPIOL_20	Yes	4	GPIOL_21	Yes
5	GPIOL_69	–	6	GPIOL_70	–
7	GPIOL_71	–	8	GPIOL_72	–
9	GPIOL_73	–	10	GPIOL_74	–
11	GND	–	12	GND	–

Table 11: J11 Pin Assignments

Pin Number	Signal Name	DDIO Mode Supported	Pin Number	Signal Name	DDIO Mode Supported
1	TXP06	–	2	TXP09	–
3	TXN09	–	4	TXN06	–
5	TXP08	–	6	TXN08	–
7	RXN04	–	8	GPIOR_157	Yes
9	GND	–	10	GPIOR_85	–
11	GPIOR_78	–	12	GPIOR_77	–
13	RXP04	–	14	GPIOR_88	–
15	RXP05	–	16	RXN06	–
17	RXN07	–	18	RXN05	–
19	RXP06	–	20	RXP07	–
21	GND	–	22	3V3	–

Table 12: J12 Pin Assignments

Pin Number	Signal Name	DDIO Mode Supported	Pin Number	Signal Name	DDIO Mode Supported
1	GPIOL_25	Yes	2	NC	–
3	GPIOR_119	Yes	4	GPIOL_24	Yes
5	GPIOR_151	Yes	6	GPIOR_120	Yes
7	GPIOR_150	Yes	8	GPIOR_121	Yes
9	GND	–	10	GPIOR_155	Yes
11	GPIOR_158	Yes	12	RXP12	–
13	RXP08	–	14	GND	–
15	RXN08	–	16	RXN12	–
17	RXN09	–	18	RXN10	–
19	RXP09	–	20	RXP10	–
21	3V3	–	22	GND	–

Header J10

J10 is a 3-pin header used to select the source for the T20F169C4 clock input and PLL input. Drive a 3.3 V clock source input into the SMA connector, J9, if you are using the external clock source option.

Table 13: Clock Selection Pin Assignments

Pin Number	Signal	Notes
1 (default)	50 MHz on-board oscillator	Connect pins 1 and 2 to select the oscillator (default)
2	GPIOR_76_PLLIN0	
3	External clock source from SMA input J9	Connect pins 2 and 3 to select the SMA input

User Outputs

The board has 2 green user LEDs that are connected to I/O pins in T20F169C4 banks 2F. By default, the T20F169C4 I/O connected to these LEDs have a pull-up resistor that turns the LEDs off; to turn a given LED on, pull the corresponding I/O signal low.

Note: When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

Table 14: User Outputs

Reference Designator	T20F169C4 Pin Name	Active
D5	GPIOL_20	Low
D6	GPIOL_21	Low

User Inputs

The board has 2 pushbutton switches that you can use as inputs to the T20F169C4 device. The T20F169C4 bank 1B I/O signals connected to these switches have a pull-up resistor. When you press the switch, the signal drives low, indicating user input.

Table 15: User Pushbuttons

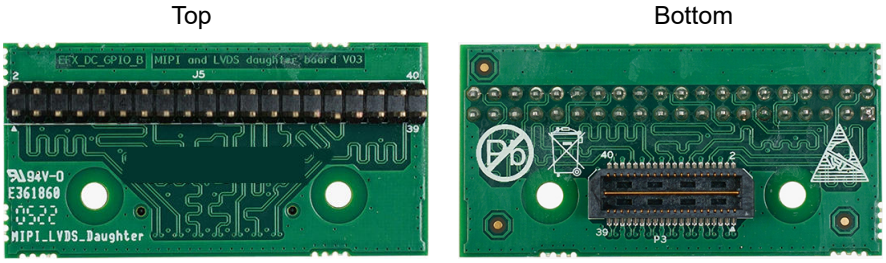
Reference Designator	T20F169C4 Pin Name	Active
SW4	GPIOL_12	Low
SW5	GPIOL_13	Low

MIPI and LVDS Expansion Daughter Card

The MIPI and LVDS Expansion Daughter Card (part number: EFX_DC_GPIO_B) converts the signals from the development board's QSE connector.

Learn more: Refer to the MIPI and LVDS Expansion Daughter Card Schematics and BOM for the part details and schematics.

Figure 3: MIPI and LVDS Expansion Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin QSE connector on the development board to a 40-pin header
- Power supplied from the development board; no external power required
  - Each pin supports up to 3 A

Headers

Table 16: MIPI and LVDS Expansion Daughter Card Headers

Reference Designator	Description
P3	40-pin QTE connector bringing MIPI or LVDS signals, power, and 1.8 V GPIO pins from the development board.
J5	40-pin header.

Headers P3 (QTE Connector) and J5 (40-Pin Header)

P3 is a 40-pin QTE connector to connect the daughter card to the QSE connector on the development board. J5 is a 40-pin header.

Table 17: P3 and J5 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO_H01	User I/O	2	GPIO_H02	User I/O
3	GPIO_H03	User I/O	4	GPIO_H04	User I/O
5	GND	Ground	6	GND	Ground
7	GPIO_H07	User I/O	8	GPIO_H08	User I/O
9	GPIO_H09	User I/O	10	GPIO_H10	User I/O
11	GND	Ground	12	GND	Ground
13	GPIO_H13	User I/O	14	GPIO_H14	User I/O
15	GPIO_H15	User I/O	16	GPIO_H16	User I/O
17	GND	Ground	18	GND	Ground
19	GPIO_H19	User I/O	20	GPIO_H20	User I/O
21	GPIO_H21	User I/O	22	GPIO_H22	User I/O
23	GND	Ground	24	GND	Ground
25	GPIO_H25	User I/O	26	GPIO_H26	User I/O
27	GPIO_H27	User I/O	28	GPIO_H28	User I/O
29	GND	Ground	30	GND	Ground
31	GPIO_H31	User I/O	32	GPIO_H32	User I/O
33	GPIO_H33	User I/O	34	GPIO_H34	User I/O
35	GND	Ground	36	GND	Ground
37	GPIO_H37	User I/O	38	GPIO_H38	User I/O
39	GPIO_H39	User I/O	40	GPIO_H40	User I/O

Signal Mapping

MIPI Signal Mapping

This table shows the pin mapping from the MIPI headers (P1, P2, P3, and P4) to the daughter card headers.

Table 18: MIPI Signal Mapping

Where x is 0 or 1 and y is TXD or RXD

Pin Number	Daughter Card Pin	MIPI Pin	Pin Number	Daughter Card Pin	MIPI Pin
1	GPIO_H01	VSUP1	2	GPIO_H02	MIPIx_y_P0
3	GPIO_H03	VSUP2	4	GPIO_H04	MIPIx_y_N0
5	GND	GND	6	GND	GND
7	NC	No Connect	8	GPIO_H08	MIPIx_y_P1
9	NC		10	GPIO_H10	MIPIx_y_N1
11	GND	GND	12	GND	GND
13	NC	No Connect	14	GPIO_H14	MIPIx_y_P2
15	NC		16	GPIO_H16	MIPIx_y_N2
17	GND	GND	18	GND	GND
19	NC	No Connect	20	GPIO_H20	MIPIx_y_P3
21	NC		22	GPIO_H22	MIPIx_y_N3
23	GND	GND	24	GND	GND
25	NC	No Connect	26	GPIO_H26	MIPIx_y_P4
27	NC		28	GPIO_H28	MIPIx_y_N4
29	GND	GND	30	GND	GND
31	NC	No Connect	32	GPIO_H32	GPIOL_69_1V8_SCL
33	NC		34	GPIO_H34	GPIOL_70_1V8_SD
35	GND	GND	36	GND	GND
37	GPIO_H37	VSUP3	38	GPIO_H38	GPIOL_71_1V8
39	GPIO_H39	GPIOL_73_REFCLK (RX) GPIOL_12_3V3 (TX)	40	GPIO_H40	GPIOL_72_1V8

LVDS Signal Mapping

This table shows the pin mapping from the LVDS headers (P5 and P6) to the daughter card headers.

Table 19: LVDS Signal Mapping

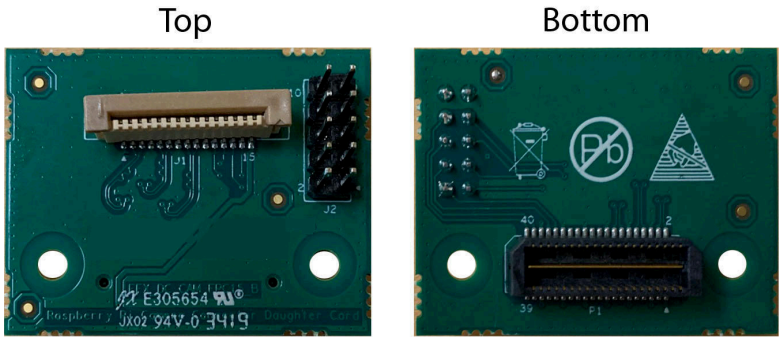
Pin #	Daughter Card Pin	LVDS P5 Pin	LVDS P6 Pin	Pin #	Daughter Card Pin	LVDS P5 Pin	LVDS P6 Pin
1	GPIO_H01	GPIOB_CLKP0	VSUP1	2	GPIO_H02	NC	GPIOL_71
3	GPIO_H03	GPIOB_CLKN0	VSUP2	4	GPIO_H04	NC	GPIOB_72
5	GND	GND	GND	6	GND	GND	GND
7	GPIO_H07	GPIOB_RXP00	GPIOB_TXP00	8	GPIO_H08	NC	NC
9	GPIO_H09	GPIOB_RXN00	GPIOB_TXN00	10	GPIO_H10	NC	NC
11	GND	GND	GND	12	GND	GND	GND
13	GPIO_H13	GPIOB_RXP01	GPIOB_TXP01	14	GPIO_H14	NC	NC
15	GPIO_H15	GPIOB_RXN01	GPIOB_TXN01	16	GPIO_H16	NC	NC
17	GND	GND	GND	18	GND	GND	GND
19	GPIO_H19	GPIOB_RXP02	GPIOB_TXP02	20	GPIO_H20	NC	NC
21	GPIO_H21	GPIOB_RXN02	GPIOB_TXN02	22	GPIO_H22	NC	NC
23	GND	GND	GND	24	GND	GND	GND
25	GPIO_H25	GPIOB_RXP03	GPIOB_TXP03	26	GPIO_H26	NC	NC
27	GPIO_H27	GPIOB_RXN03	GPIOB_TXN03	28	GPIO_H28	NC	NC
29	GND	GND	GND	30	GND	GND	GND
31	GPIO_H31	GPIOL_12	GPIOL_12	32	GPIO_H32	VSUP1	GPIOL_71
33	GPIO_H33	GPIOL_13	GPIOL_13	34	GPIO_H34	VSUP2	GPIOL_72
35	GND	GND	GND	36	GND	GND	GND
37	GPIO_H37	GPIOL_20	GPIOB_TXP05	38	GPIO_H38	GPIOL_73	NC
39	GPIO_H39	GPIOL_21	GPIOB_TXN05	40	GPIO_H40	GPIOB_74	NC

Raspberry Pi Camera Connector Daughter Card

The Raspberry Pi Camera Connector Daughter Card (part number: EFX_DC_CAM_FPC15_B) bridges between the development board and a Raspberry Pi camera module. The daughter card connects to a Raspberry Pi computer or any Raspberry Pi camera using a 15 pin flat cable. Additionally, the board has a 10 pin header for optional camera control pins.

Learn more: Refer to the Raspberry Pi Camera Connector Daughter Card Schematics and BOM for the part details and schematics.

Figure 4: Raspberry Pi Camera Connector Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin MIPI CSI-2 interface on a Trion® T20 MIPI Development Board to a 15-pin interface
- Pin to pin compatible with Raspberry Pi cameras
- Supports up to 1.5 Gbps on MIPI interface
- User selectable pins for optional camera functions
- Power supplied from the Trion® T20 MIPI Development Board; no external power required; each pin supports up to 3 A

Note: For technical support using Raspberry Pi cameras, please refer to their web site at **www.raspberrypi.org**.

Headers

Table 20: Raspberry Pi Camera Connector Daughter Card Headers

Reference Designator	Description
P1	40-pin QTE header bringing MIPI signals, power, and 1.8 V GPIO pins from the Trion® T20 MIPI Development Board.
J1	15-pin flexible printed cable (FPC) connector for Raspberry Pi MIPI camera modules.
J2	10-pin header for optional Raspberry Pi MIPI camera module signals.

Header P1 (Development Board Connector)

P1 is a 40-pin QTE header to connect the daughter card to the development board. The header provides MIPI signals and power to the camera module.

- Raspberry Pi computer—When using this daughter card with a Raspberry Pi computer, connect header P1 to a MIPI TX socket on the development board.
- Raspberry Pi camera—When using this daughter card with a Raspberry Pi camera, connect header P1 to a MIPI RX socket on the development board.

Table 21: Development Board Connector (P1)

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	3V3_15FPC	3.3V Supply	2	MIPI_P0_15FPC	Differential MIPI lane 0
3	NC	No connect	4	MIPI_N0_15FPC	
5	GND	Ground	6	GND	Ground
7	NC	No connect	8	MIPI_P1_15FPC	Differential MIPI lane 1
9	NC		10	MIPI_N1_15FPC	
11	GND	Ground	12	GND	Ground
13	NC	No connect	14	MIPI_P2_15FPC	Differential MIPI lane 2
15	NC		16	MIPI_N2_15FPC	
17	GND	Ground	18	GND	Ground
19	NC	No connect	20	NC	No connect
21	NC		22	NC	
23	GND	Ground	24	GND	Ground
25	NC	No connect	26	NC	No connect
27	NC		28	NC	
29	GND	Ground	30	GND	Ground
31	NC	No connect	32	GPIO0	1.8 V GPIO
33	NC		34	GPIO1	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	NC	No connect	38	GPIO2	1.8 V GPIO
39	NC		40	GPIO3	1.8 V GPIO

Header J1 (Raspberry Pi FPC15 Connector)

J1 is a 15-pin flexible flat cable header for connecting to a Raspberry Pi MIPI camera module.

- Raspberry Pi computer—When using this daughter card with a Raspberry Pi computer, these pins are TX.
- Raspberry Pi camera—When using this daughter card with a Raspberry Pi camera, these pins are RX.

Table 22: Raspberry Pi FPC15 Connector (J1)

where n is RXD or TXD, depending on whether you are connecting to a camera or Raspberry Pi computer.

Pin Number	Pin Name	Description
1	GND	Ground
2	MIPI_N0_15FPC	Differential MIPI lane 0
3	MIPI_P0_15FPC	
4	GND	Ground
5	MIPI_N1_15FPC	Differential MIPI lane 1
6	MIPI_P1_15FPC	
7	GND	Ground
8	MIPI_N2_15FPC	Differential MIPI lane 2
9	MIPI_P2_15FPC	
10	GND	Ground
11	GPIO2_15FPC	GPIO for Raspberry Pi MIPI camera module
12	GPIO3_15FPC	
13	GPIO0_15FPC	Serial clock for Raspberry Pi MIPI camera module
14	GPIO1_15FPC	Serial data for Raspberry Pi MIPI camera module
15	3V3_15FPC	3.3 V power supply

Header J2 (Optional Camera Signals)

The J2 header has optional pins (SCL and SDA) that are used for MIPI Camera Command Set (CSS) transactions. These signals are routed to the Trion® FPGA on the board. You can control these pins with an external device by removing the jumpers and connecting wires from the header to an external device.

Note: If you connect jumpers to any pins in J2, do not use the corresponding GPIO in your design. For example, if you use jumpers on pins 1-2 and 3-4, do not use `GPIO_69` or `GPIO_70`.

Table 23: Optional Camera Signals (J2)

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO0	1.8 V I/O from development board	2	GPIO0_15FPC	I^2C bus SCL signal
3	GPIO1		4	GPIO1_15FPC	I^2C bus SDA signal
5	GPIO2		6	GPIO2_15FPC	Camera GPIO
7	GPIO3		8	GPIO3_15FPC	Camera clock
9	GND	Ground	10	GND	Ground

Setting up the Board

Installing Standoffs

Before using the board, attach the standoffs with the screws (M3 size) provided in the kit.

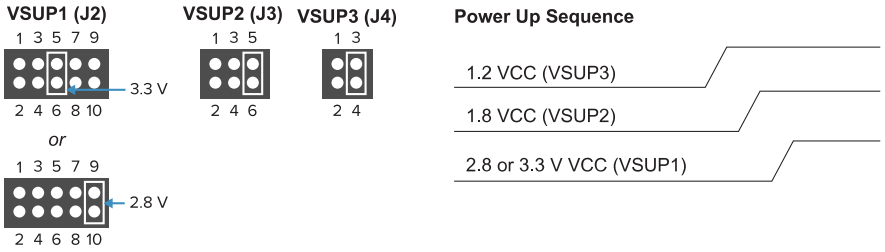
Warning: You can damage the board if you over tighten the screws. Tighten all screws to a torque between 4 ± 0.5 kgf/cm and 5 ± 0.5 kgf/cm.

Setting the Power-Up Sequence for MIPI Cameras

Trion® T20 MIPI Development Board has a built-in power-up sequence circuit for the MIPI transmitter and receiver interfaces (P1, P2, P3, and P4) that is compatible with MIPI camera sensor power requirements. To enable the power-up sequence, you connect jumpers on the power supply headers J2, J3, and J4.

1. Remove power from the board.
2. Choose your camera voltage for VSUP1 (J2) by connecting pins 5 and 6 for 3.3 V or pins 9 and 10 for 2.8 V.
3. Connect pins 5 and 6 for VSUP2 (J3).
4. Connect pins 3 and 4 for VSUP3 (J4).
5. Attach the camera connector daughter card for the camera you want to use to the board.
6. Attach the camera to the daughter card.
7. Turn on power to the board.

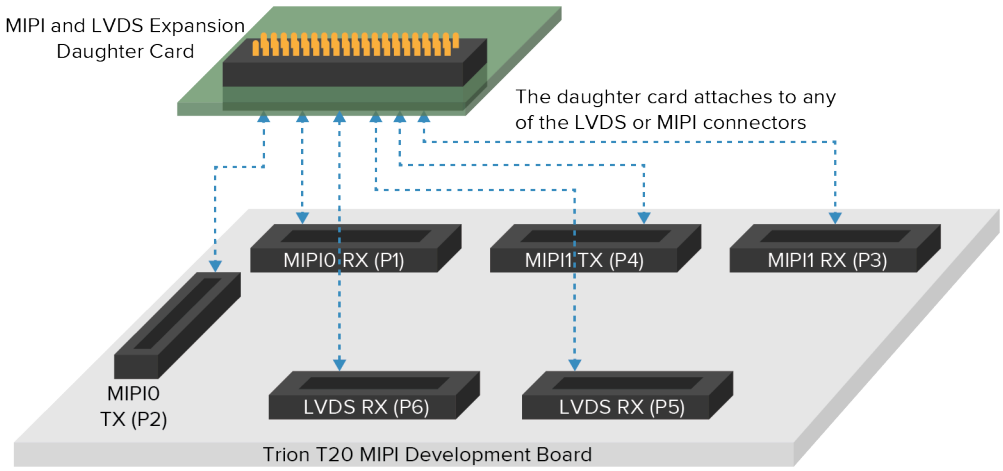
Figure 5: Setting the Power Sequence Jumpers



Attaching the MIPI and LVDS Expansion Daughter Card

The Trion® T20 MIPI Development Board supports an expansion daughter card that fans out the GPIO.

Figure 6: Attaching MIPI and LVDS Expansion Daughter Card



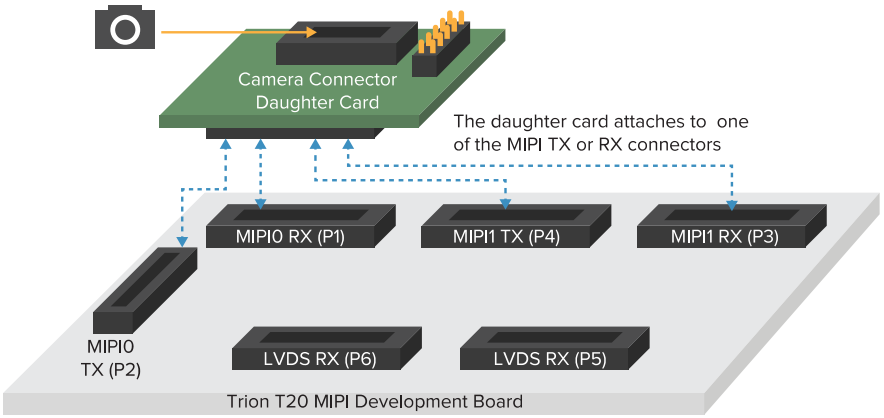
To connect the daughter card:

1. Remove power from the Trion® T20 MIPI Development Board.
2. Attach standoffs to the MIPI and LVDS Expansion Daughter Card.
3. Attach the MIPI and LVDS Expansion Daughter Card to one of the LVDS or MIPI 40-pin headers on the Trion® T20 MIPI Development Board.
4. Connect any cables to the GPIO as needed for your application.
5. Power up the Trion® T20 MIPI Development Board.

Attaching Camera Connector Daughter Cards

The camera connector daughter card attaches to the high-speed MIPI TX or RX headers.

Figure 7: Attaching Camera Connector Daughter Cards (T20 MIPI Board)



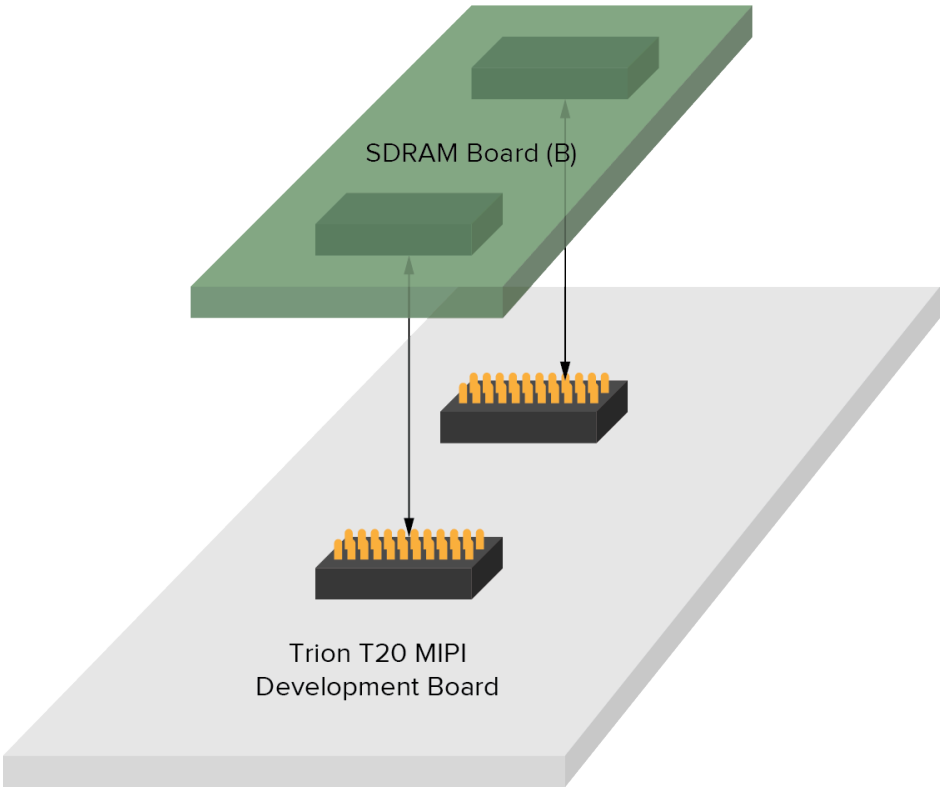
To connect a daughter card:

1. Remove power from the Trion® T20 MIPI Development Board.
2. Attach standoffs to the daughter card.
3. Attach the daughter card to the 40-pin header on the board.
4. Connect the camera module or computer to the daughter card using a ribbon cable.
5. Power up the board.

Attaching an SDRAM Accessory Board

You can attach the Waveshare SDRAM board (B) accessory board to the two 22-pin GPIO headers, adding 8M x 16 bits of SDRAM. Refer to **https://www.waveshare.com/sdram-board-b.htm** for information about this SDRAM accessory board.

Figure 8: Attaching SDRAM Board



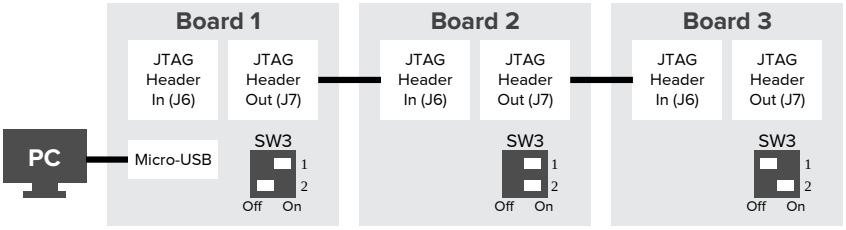
To connect the SDRAM board:

1. Remove power from the Trion® T20 MIPI Development Board.
2. Connect the SDRAM board to J11 and J12.
3. Power up the board.

Connecting Multiple Boards in a JTAG Chain

The Trion® T20 MIPI Development Board has headers and switches that make it easy for you to connect multiple boards together in a JTAG chain. Then, you can program the chained boards or perform JTAG debugging or scanning.

Figure 9: Boards in a JTAG Chain



To chain boards together:

1. Connect a 10-pin cable from JTAG header out (J7) on the first board to JTAG header in (J6) on the second board.
2. For the first board in the chain, turn on switch 1 and turn off switch 2.
3. For the middle board(s) in the chain, turn on switches 1 and 2.
4. For the last board in the chain, turn off switch 1 and turn on switch 2.

Note: Connect three or more boards similarly: connect J7 to J6.

Table 24: JTAG Chain Select (SW3) Settings

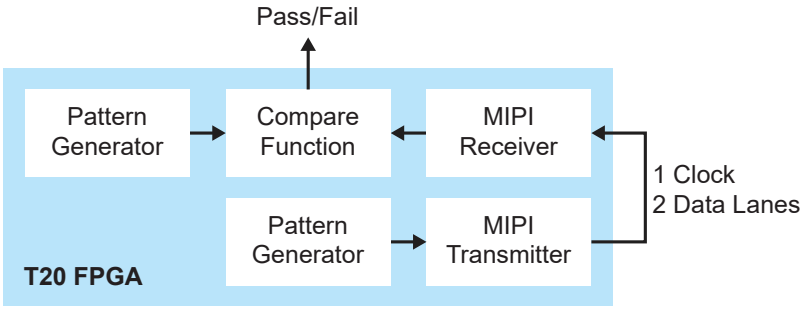
Switch	Position	Description
1	On	The TDO signal is connected to the TDI signal of the next board.
	Off (default)	The TDO signal is connected to the on-board FTDI chip.
2	On	The CRESET_N signal is connected to the on-board FTDI chip. Turn this switch on only when you want to program the board.
	Off (default)	The CRESET_N signal is not connected.

Note: If the board is not in a JTAG chain turn off both switches in SW3.

Running the Loopback Design

易灵思® preloads the Trion® T20 MIPI Development Board with a loopback design that helps you verify the functionality of the MIPI RX and TX interfaces.

Figure 10: Loopback Design Block Diagram



The loopback design uses the following hardware:

- Trion® T20 MIPI Development Board
- 2 Raspberry Pi Camera Connector Daughter Cards
- 15-pin FFC/FPC cable
- Optional: Raspberry Pi VGA666 DPI dtoverlays module (also called a Gert-VGA-666 module) to view output on a VGA monitor (available from vendors online)

Set Up the Hardware

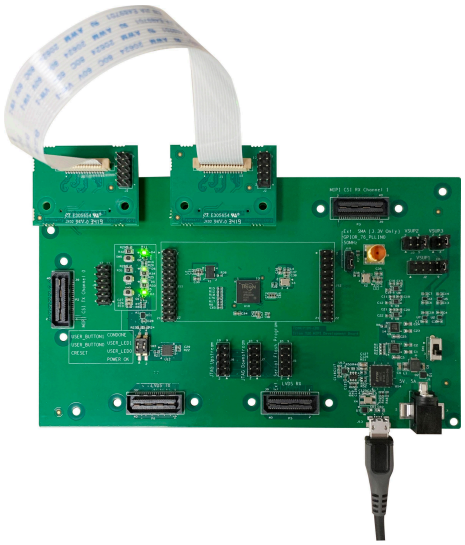
1. Attach standoffs to the board and daughter cards.
2. Connect a Raspberry Pi Camera Connector Daughter Card to P1 (MIPI CSI-2 channel 0 receiver).
3. Connect a Raspberry Pi Camera Connector Daughter Card to P4 (MIPI CSI-2 channel 1 transmitter).
4. Connect the 2 daughter cards with the 15-pin flat cable.
5. Connect the USB cable to your computer and to the Trion® T20 MIPI Development Board. The board receives power through the cable.

Note: Alternatively, you can connect a power cable to the board's 5 V DC connector and to a power source.

Run the Loopback Design

1. Turn on the Trion® T20 MIPI Development Board's power switch (SW1). The FPGA generates a video pattern and transmits it out MIPI TX channel 1 (P4) and receives the data at MIPI RX channel 0 (P1). LEDs D5 and D6 blink alternately to indicate the received data is correct.

Figure 11: Running the Demonstration Design



Optional: Display the Loopback Results on a VGA Monitor

To show the test video pattern on a VGA monitor, you can connect the board to a VGA 666 module using the 22-pin header J11.

1. Turn off the Trion® T20 MIPI Development Board power switch.
2. Attach connectors from J11 to the module as shown in the following table:

J11 Pin	Signal Name	Module Pin	J11 Pin	Signal Name	Module Pin
1	vga_b[0]	29	2	vga_b[1]	31
3	vga_b[2]	26	4	vga_b[3]	24
5	vga_b[4]	21	6	vga_g[0]	19
7	vga_g[1]	23	8	vga_g[2]	32
9	GND	6	10	vga_g[3]	33
11	vga_g[4]	8	12	vga_g[5]	10
13	vga_r[0]	11	14	vga_r[1]	12
15	vga_r[2]	35	16	vga_r[3]	38
17	vga_r[4]	40	18	NC	NC
19	vga_hs	5	20	vga_vs	3
21	NC	NC	22	NC	NC

3. Attach a VGA cable from the module to a VGA monitor.
4. Turn on power to the board and monitor.
5. Press SW4 to change to a different video pattern. You can cycle through 4 patterns.

Creating Your Own Design

The Trion® T20 MIPI Development Board allows you to create and explore designs for the T20 device. 易灵思® provides example code and designs to help you get started:

- Our Support Center includes examples targeting the board.
- The Efinity software includes also example designs that you can use as a starting point for your own project, and includes a step-by-step tutorial.
- AN 027: Using the Raspberry Pi to HDMI Example Designs (T120 BGA576) includes example designs with additional features for Trion® T20 MIPI Development Board.

Appendix 1: Shared Resources

Some of the resources available on the Trion® T20 MIPI Development Board are connected to more than one I/Os. You need to ensure there are no overlapping assignments when using these resources. The following table lists the resources shared by more than one I/Os. You can refer to this table to help you plan the resources available in the Trion® T20 MIPI Development Board

Note: Resources that are not listed are only available from one I/O (see **Headers** on page 9).

Table 25: Trion® T20 MIPI Development Board Shared Resources

<header name>.<pin name/number>

Resource	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
GPIOL_20	J8.3	P5.37	LED.D5	–	–	–
GPIOL_21	J8.4	P5.39	LED.D6	–	–	–
GPIOL_12	J8.1	P2.39	P4.39	P5.31	P6.31	Pushbutton.SW4
GPIOL_13	J8.2	P5.33	P6.33	Pushbutton.SW5	–	–
GPIOL_73	J8.9	P1.39	P3.39	P5.38	–	–
GPIOL_74	J8.10	P5.40	–	–	–	–
GPIOL_69	J8.5	P1.32	P2.32	P3.32	P4.32	P6.2
GPIOL_70	J8.6	P1.34	P2.34	P3.34	P4.34	P6.4
GPIOL_71	J8.7	P1.38	P2.38	P3.38	P4.38	P6.32
GPIOL_72	J8.8	P1.40	P2.40	P3.40	P4.40	P6.34

Revision History

Table 26: Revision History

Date	Version	Description
October 2023	1.9	Correct Boards in a JTAG Chain figure and updated JTAG Chain Select (SW3) Settings descriptions. (DOC-1521)
November 2022	1.8	Added link to AN 050: Managing Windows Drivers in Installing the Windows USB Drivers topic.
September 2022	1.7	Updated Installing Windows Driver.
June 2022	1.6	Corrected P1, P2, P3, P4, J10 header signals numbers. Added Appendix 1: Shared resources.
December 2021	1.5	Corrected the MIPI and LVDS Expansion Card headers.
September 2021	1.4	Added USB driver installation topics. (DOC-463)
February 2021	1.3	Added note about referring to the power-up sequence in the data sheet when designing a board and recommending supervisor IC for `CRESET_N` (DOC-388).
April 2020	1.2	Corrected the pin names for the Raspberry Pi camera connector daughter card. Corrected signal names for J12 pins 21 and 22.
March 2020	1.1	Corrected reset pushbutton; it is SW2. Corrected Figure 9 switch settings. Corrected Table 24 switch descriptions.
October 2019	1.0	Initial release.