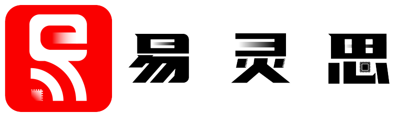

Trion® Packaging User Guide

UG-TRION-PKG-v5.2
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Introduction

Elitestek offers Trion® FPGAs in packages that are designed for the devices' maximum number of user's I/O pins. This document describes the Trion® FPGAs' pin and package specifications as well as solder reflow guidelines.

Learn more: Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

Available Package Options

Table 1: Available Packages

Package	Dimensions (mm x mm)	Pitch (mm)
T4/T8 FPGAs		
49-ball FBGA[(1)]	3 x 3	0.4
81-ball FBGA	5 x 5	0.5
T20 FPGAs		
80-ball WLCSP	4.5 x 3.6	0.4
T8/T20 FPGAs		
144-pin LQFP	20 x 20	0.5
T13/T20 FPGAs		
100-pin LQFP	14 x 14	0.5
169-ball FBGA	9 x 9	0.65
T13/T20/T35 FPGAs		
256-ball FBGA	13 x 13	0.8
T20/T35 FPGAs		
324-ball FBGA	12 x 12	0.65
400-ball FBGA	16 x 16	0.8
T55/T85/T120 FPGAs		
324-ball FBGA	12 x 12	0.65
484-ball FBGA	18 x 18	0.80
576-ball FBGA	16 x 16	0.65

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

(1) This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

Device Pinout File

Elitestek provides pinout files for Trion® FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates the location.
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location.
VCCIO*xx_yy_zz*	Power	–	I/O pin power supply. Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations.
GND	Ground	–	Ground.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock.
GNDA_PLL	Ground	–	PLL ground pin.
MREFCLK	Alternate	Input	MIPI TX PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single-ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: (T4) Indicates the bank; left (L) or right (R). *x*: (T13/T20) Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.

Table 3: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

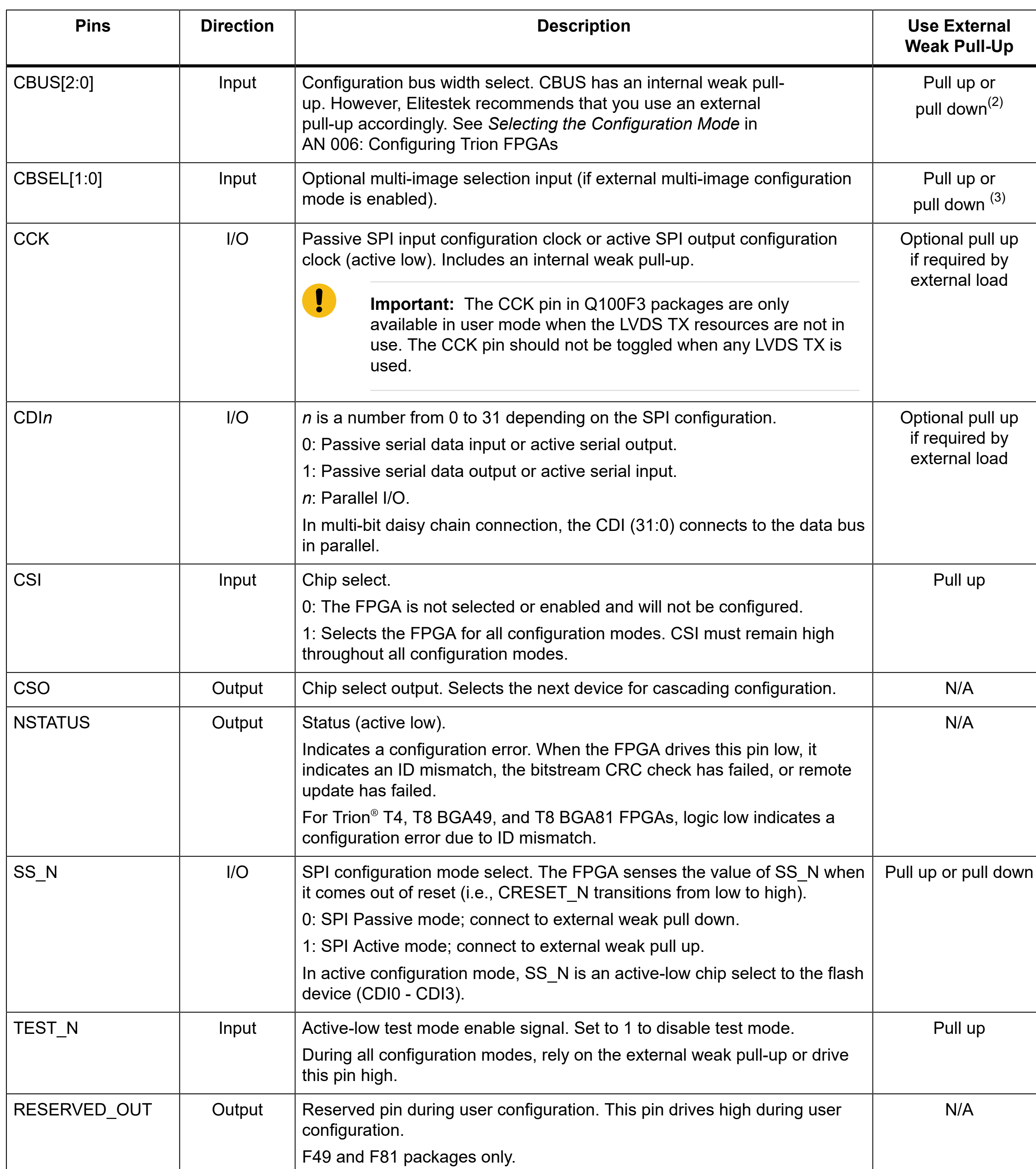
All the pins are in internal weak pull-up during configuration except for `TCK` and `TDO`.

Pins	Direction	Description	External Weak Pull- Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

Note: All dedicated configuration pins have Schmitt Trigger buffer. Refer to the respective Trion FPGAs datasheet for the Schmitt Trigger buffer specifications in **Single Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer** table.

Table 4: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.



Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. CBUS has an internal weak pull-up. However, Elitestek recommends that you use an external pull-up accordingly. See *Selecting the Configuration Mode* in AN 006: Configuring Trion FPGAs	Pull up or pull down[2]
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	Pull up or pull down [3]
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up. **Important:** The CCK pin in Q100F3 packages are only available in user mode when the LVDS TX resources are not in use. The CCK pin should not be toggled when any LVDS TX is used.	Optional pull up if required by external load
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI (31:0) connects to the data bus in parallel.	Optional pull up if required by external load
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for all configuration modes. CSI must remain high throughout all configuration modes.	Pull up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed. For Trion® T4, T8 BGA49, and T8 BGA81 FPGAs, logic low indicates a configuration error due to ID mismatch.	N/A
SS_N	I/O	SPI configuration mode select. The FPGA senses the value of SS_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: SPI Passive mode; connect to external weak pull down. 1: SPI Active mode; connect to external weak pull up. In active configuration mode, SS_N is an active-low chip select to the flash device (CDI0 - CDI3).	Pull up or pull down
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. F49 and F81 packages only.	N/A

[2] Optional for x1 mode.
[3] Not applicable to single-image or remote update.

Table 5: MIPI Pinouts (Dedicated)

n Indicates the number. *L* indicates the lane

Function	Group	Direction	Description
VCC25A_MIPI0 VCC25A_MIPI1	Power	–	MIPI 2.5 V analog power supply.
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	Power	–	MIPI 1.2 V TX analog power supply.
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	Power	–	MIPI 1.2 V RX analog power supply.
GNDA_MIPI	Ground	–	Ground for MIPI analog power supply.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	MIPI	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	MIPI	I/O	MIPI differential receive data lane.
MREFCLK	Clock	Input	MIPI PLL reference clock source.

Table 6: DDR Pinouts (Dedicated)

n indicates the number.

Function	Direction	Description
VCCIO_DDR	–	DDR power supply.
DDR_A[*n*]	Output	Address signals to the memories.
DDR_BA[*n*]	Output	Bank signals to the memories.
DDR_CAS_N	Output	Active-low column address strobe signal to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	Output	Active-high data-mask signals to the memories.
DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_DQS[*n*]	I/O	Differential data strobes to/from the memories.
DDR_ODT	Output	ODT signal to the memories.
DDR_RAS_N	Output	Active-low row address strobe signal to the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_WE_N	Output	Active-low write enable strobe signal to the memories.
DDR_VREF	I/O	Reference voltage.
DDR_ZQ	I/O	ZQ calibration pin.

Table 7: SPI Flash Memory Pin

Function	Direction	Description
SPI_CS_N	Input	Active-low internal SPI flash memory chip select. Available in QFP100F3 packages only.

49-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 49-Ball FBGA Pinout Diagram

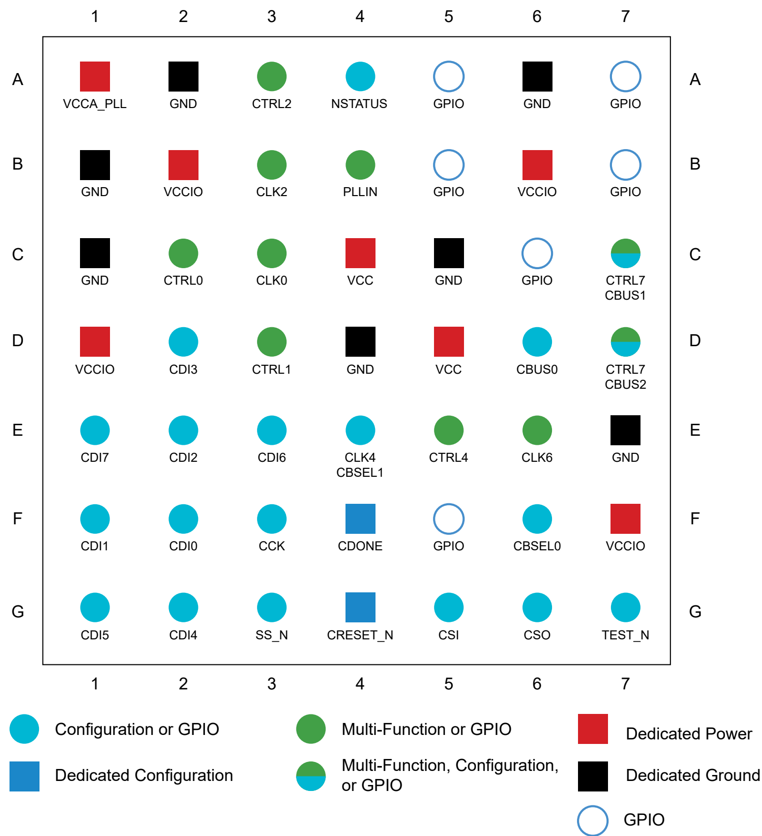


Figure 2: 49-Ball FBGA I/O Bank Diagram

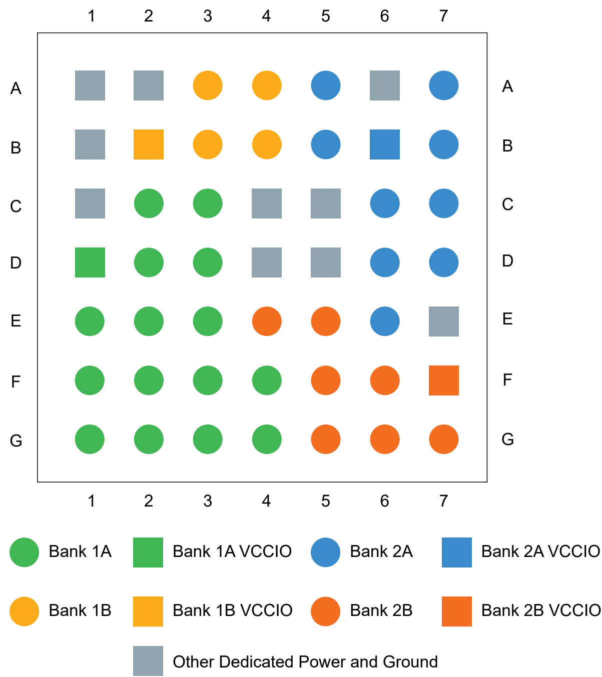


Figure 3: 49-Ball FPGA Package Marking

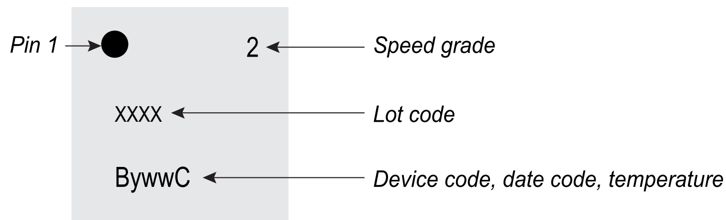
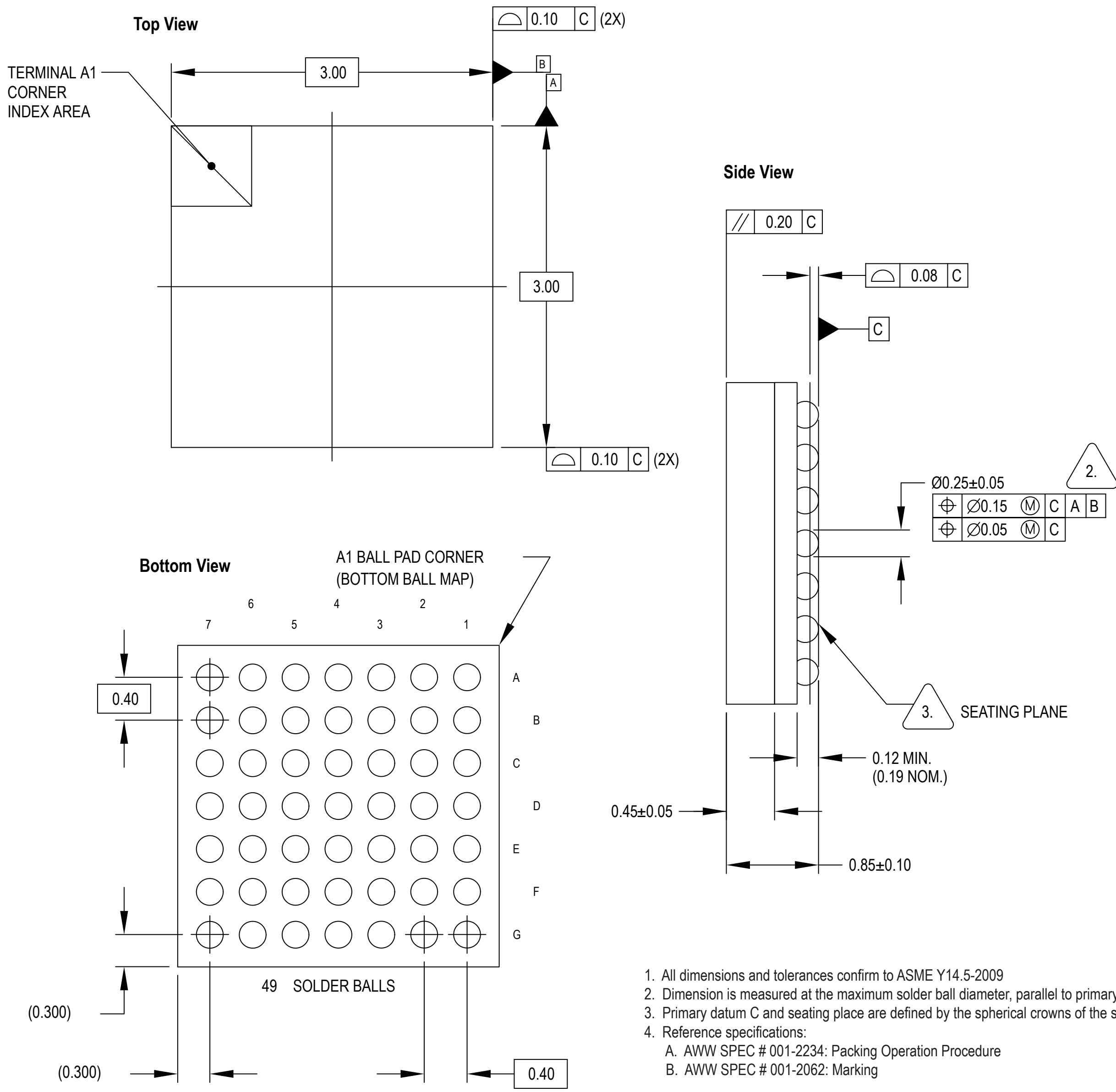


Figure 4: 49-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AWW SPEC # 001-2234: Packing Operation Procedure
   B. AWW SPEC # 001-2062: Marking

80-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 5: 80-Ball WLCSP Pinout Diagram

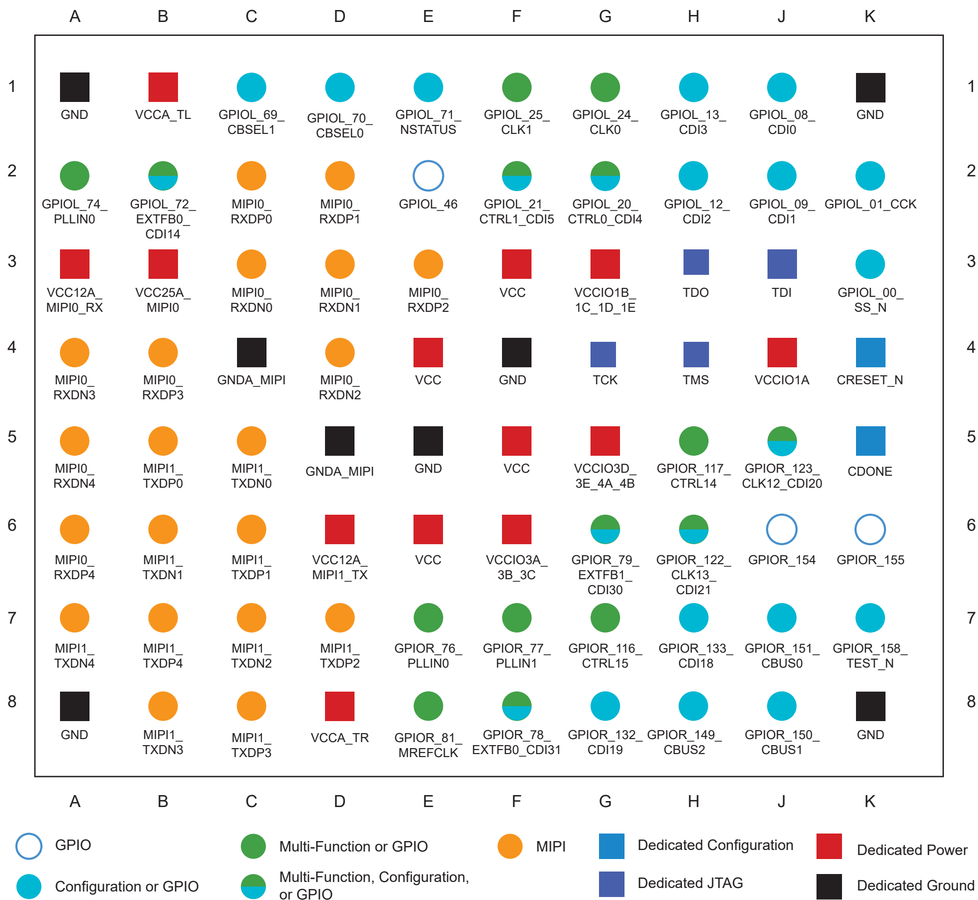


Figure 6: 80-Ball WLCSP I/O Bank Diagram

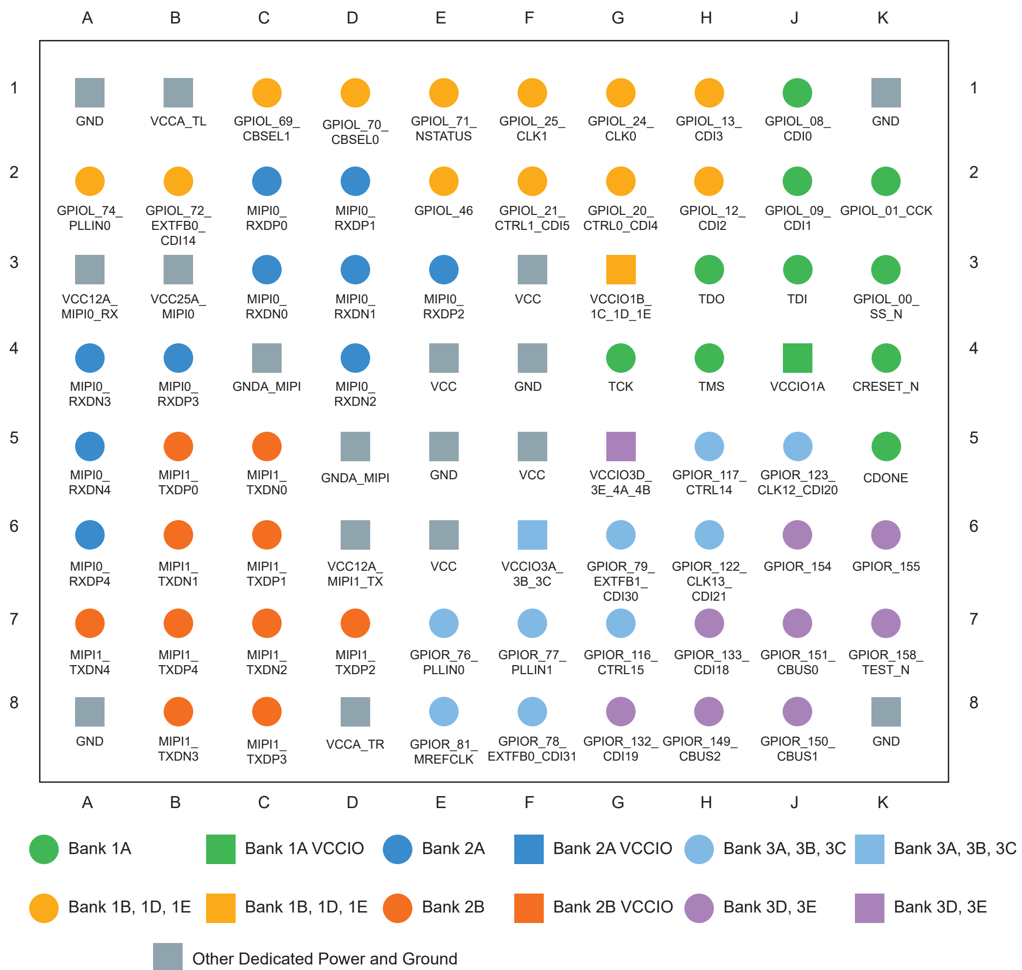


Figure 7: 80-Ball WLCSP Package Marking

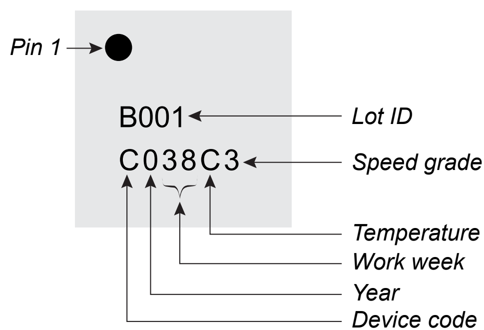
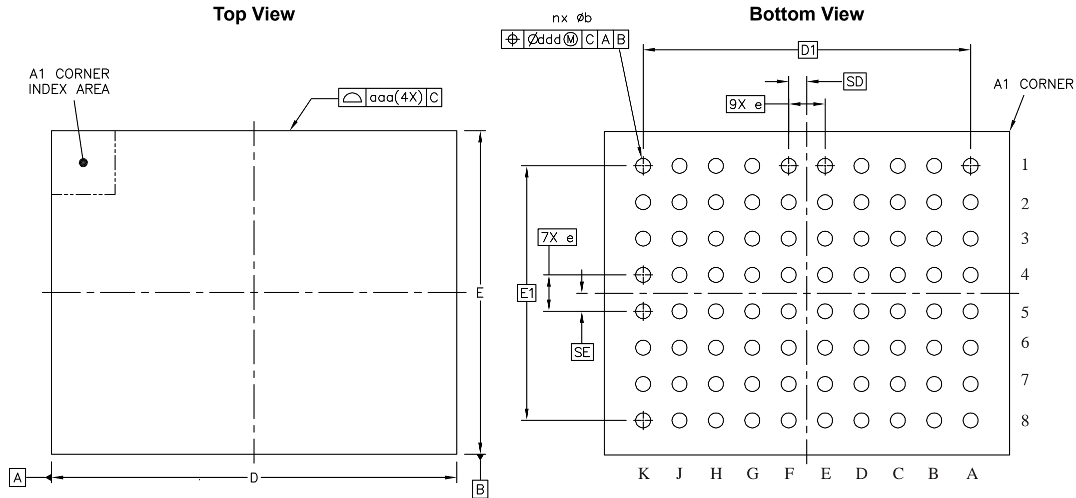
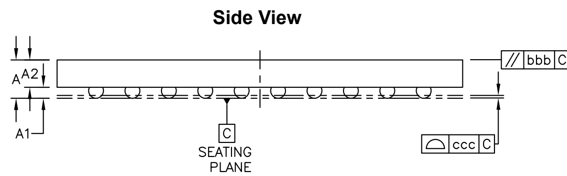


Figure 8: 80-Ball WLCSP Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.4	0.455	0.51
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.275	0.3	0.325
FILM THICKNESS		A3	---	---	---
BODY SIZE	Y	D	4.4567		
	X	E	3.5569		
BALL/BUMP PITCH	Y	SD	0.2		BSC
	X	SE	0.2		BSC
EDGE BALL CENTER TO CENTER	Y	D1	3.6		BSC
	X	E1	2.8		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	80		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.03		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		



81-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 9: 81-Ball FBGA Pinout Diagram

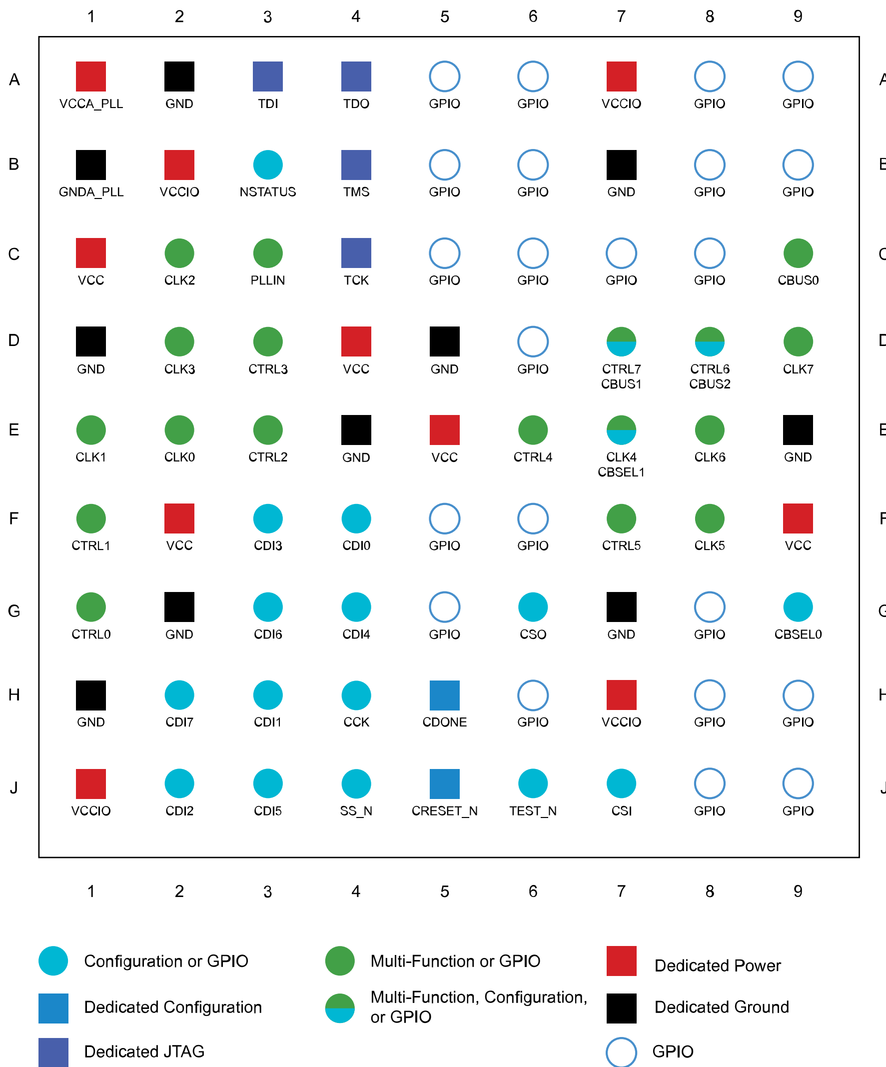


Figure 10: 81-Ball FBGA I/O Bank Diagram

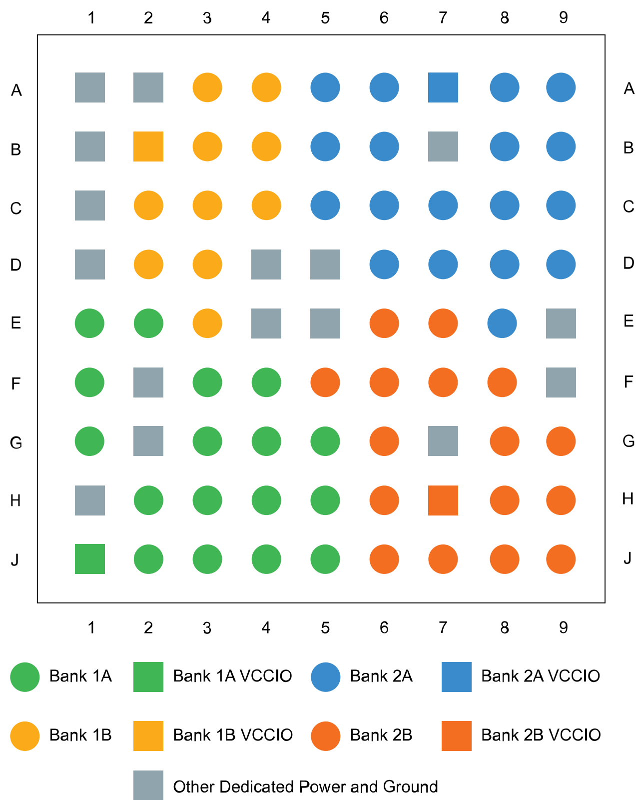


Figure 11: 81-Ball FPGA Package Marking

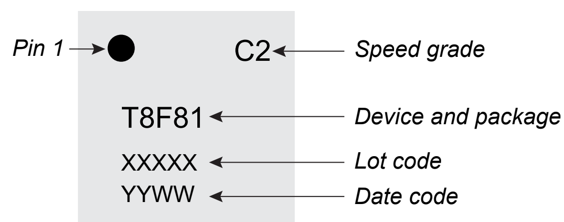
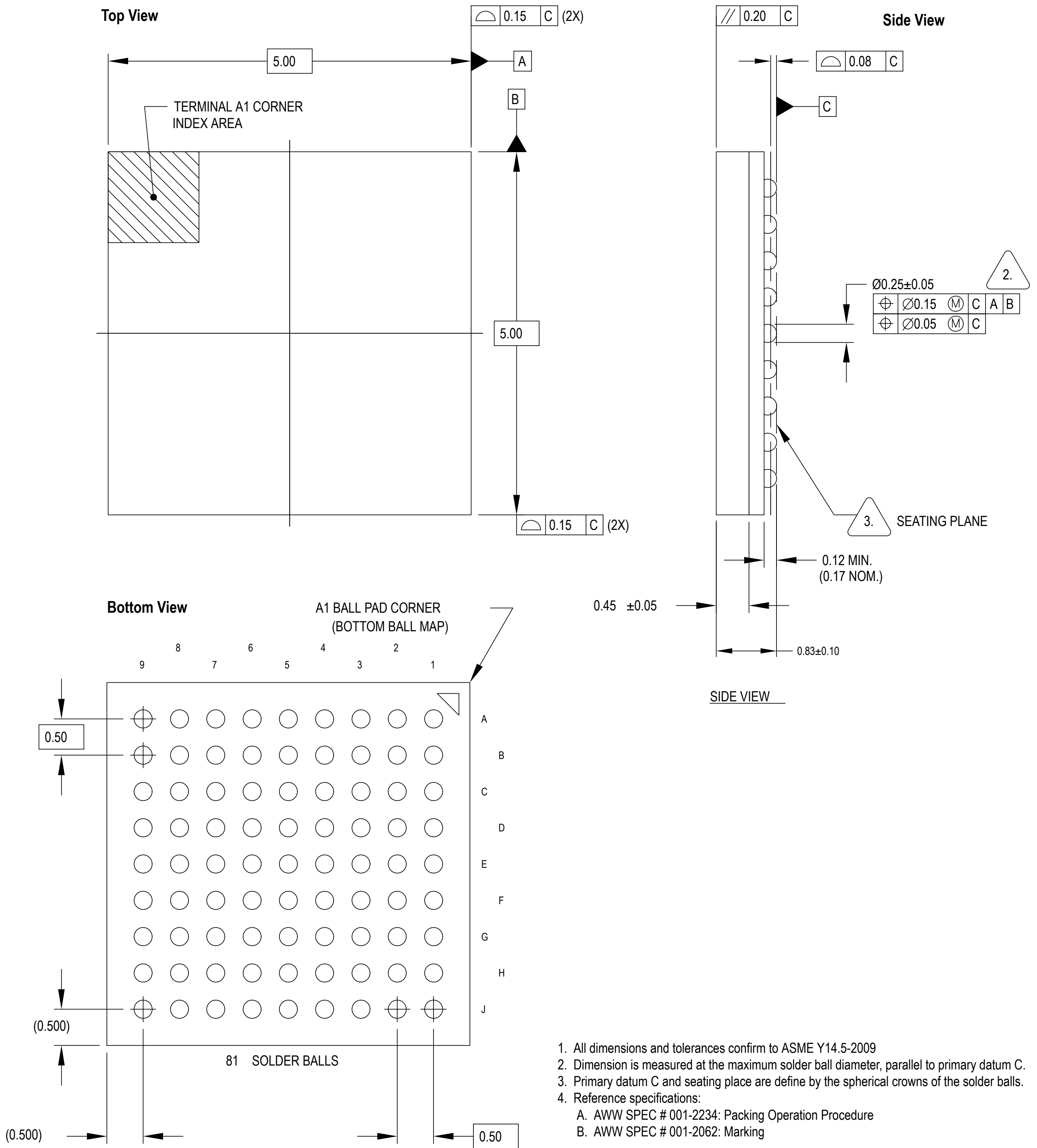


Figure 12: 81-Ball FBGA Package Outline



100-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

Figure 13: 100-Lead LQFP Pinout Diagram

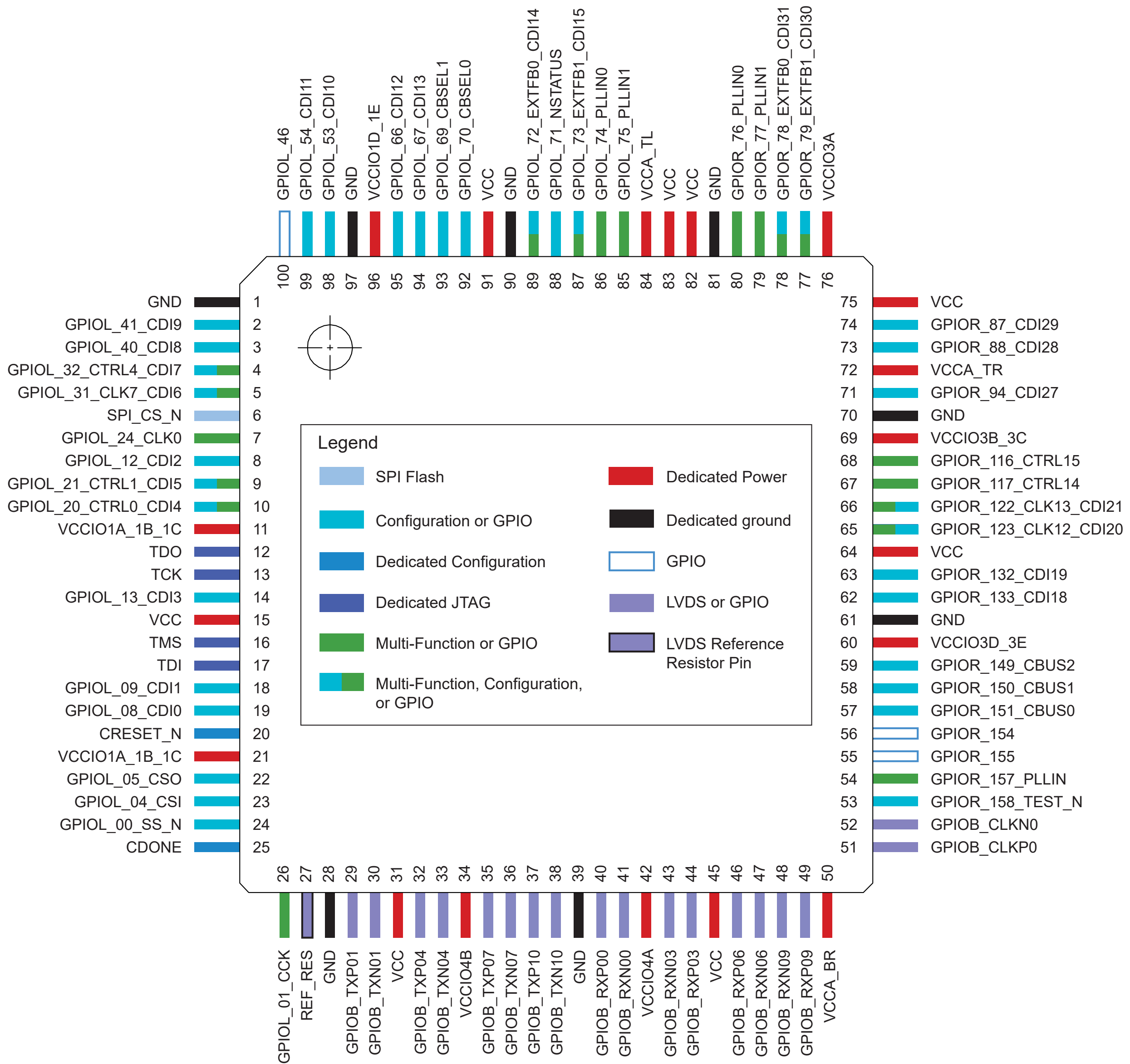


Figure 14: 100-Lead LQFP I/O Bank Diagram

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	26	GPIOL_01_CCK	51	GPIOB_CLKP0	76	VCCIO3A
2	GPIOL_41_CDI9	27	REF_RES	52	GPIOB_CLKN0	77	GPIOR_79_EXTFB1_CDI30
3	GPIOL_40_CDI8	28	GND	53	GPIOR_158_TEST_N	78	GPIOR_78_EXTFB0_CDI31
4	GPIOL_32_CTRL4_CDI7	29	GPIOB_TXP01	54	GPIOR_157_PLLIN	79	GPIOR_77_PLLIN1
5	GPIOL_31_CLK7_CDI6	30	GPIOB_TXN01	55	GPIOR_155	80	GPIOR_76_PLLIN0
6	SPI_CS_N	31	VCC	56	GPIOR_154	81	GND
7	GPIOL_24_CLK0	32	GPIOB_TXP04	57	GPIOR_151_CBUS0	82	VCC
8	GPIOL_12_CDI2	33	GPIOB_TXN04	58	GPIOR_150_CBUS1	83	VCC
9	GPIOL_21_CTRL1_CDI5	34	VCCIO4B	59	GPIOR_149_CBUS2	84	VCCA_TL
10	GPIOL_20_CTRL0_CDI4	35	GPIOB_TXP07	60	VCCIO3D_3E	85	GPIOL_75_PLLIN1
11	VCCIO1A_1B_1C	36	GPIOB_TXN07	61	GND	86	GPIOL_74_PLLIN0
12	TDO	37	GPIOB_TXP10	62	GPIOR_133_CDI18	87	GPIOL_73_EXTFB1_CDI15
13	TCK	38	GPIOB_TXN10	63	GPIOR_132_CDI19	88	GPIOL_71_NSTATUS
14	GPIOL_13_CDI3	39	GND	64	VCC	89	GPIOL_72_EXTFB0_CDI14
15	VCC	40	GPIOB_RXP00	65	GPIOR_123_CLK12_CDI20	90	GND
16	TMS	41	GPIOB_RXN00	66	GPIOR_122_CLK13_CDI21	91	VCC
17	TDI	42	VCCIO4A	67	GPIOR_117_CTRL14	92	GPIOL_70_CBSEL0
18	GPIOL_09_CDI1	43	GPIOB_RXN03	68	GPIOR_116_CTRL15	93	GPIOL_69_CBSEL1
19	GPIOL_08_CDI0	44	GPIOB_RXP03	69	VCCIO3B_3C	94	GPIOL_67_CDI13
20	CRESET_N	45	VCC	70	GND	95	GPIOL_66_CDI12
21	VCCIO1A_1B_1C	46	GPIOB_RXP06	71	GPIOR_94_CDI27	96	VCCIO1D_1E
22	GPIOL_05_CSO	47	GPIOB_RXN06	72	VCCA_TR	97	GND
23	GPIOL_04_CSI	48	GPIOB_RXN09	73	GPIOR_88_CDI28	98	GPIOL_53_CDI10
24	GPIOL_00_SS_N	49	GPIOB_RXP09	74	GPIOR_87_CDI29	99	GPIOL_54_CDI11
25	CDONE	50	VCCA_BR	75	VCC	100	GPIOL_46

Legend
- Bank 1A, 1B, 1C
- Bank 1A_1B_1C VCCIO
- Bank 1D, 1E
- Bank 1D_1E VCCIO
- Bank 3A
- Bank 3A VCCIO
- Bank 3B, 3C
- Bank 3B_3C VCCIO
- Bank 3D, 3E
- Bank 3D_3E VCCIO
- Bank 4A
- Bank 4A VCCIO
- Bank 4B
- Bank 4B VCCIO
- Other dedicated Power and Ground

Figure 15: 100-Lead LQFP FPGA Package Marking

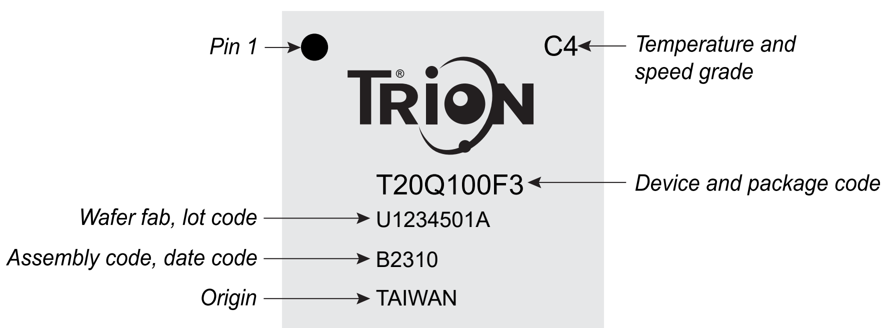
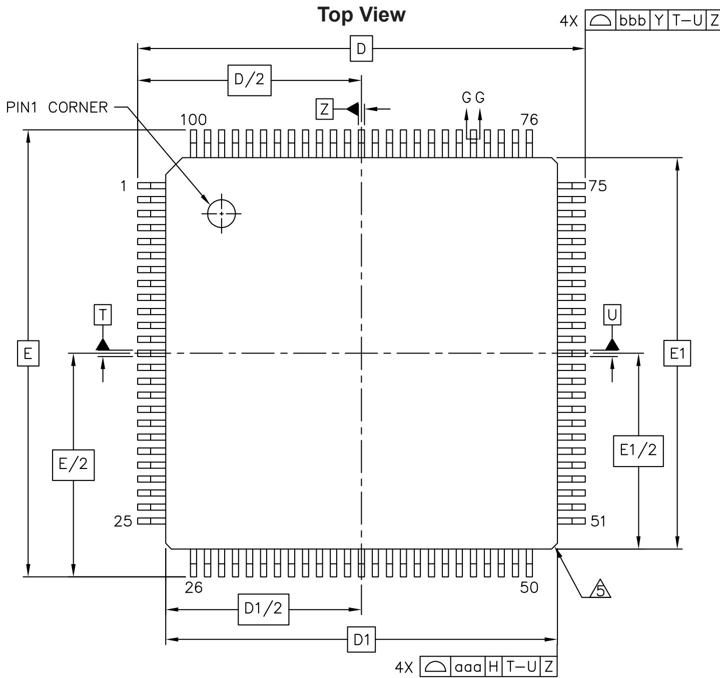
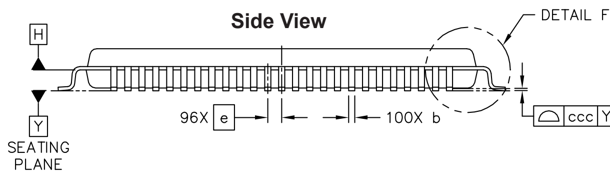
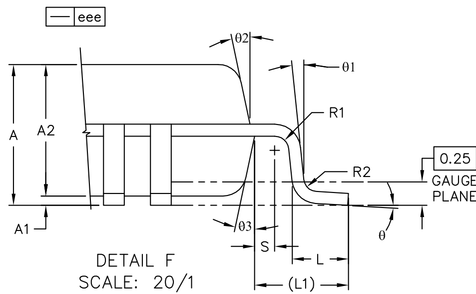


Figure 16: 100-Lead LQFP FPGA Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.2	0.27
LEAD WIDTH		b1	0.17	---	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.5 BSC		
FOOTPRINT		L	0.45	0.6	0.75
		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

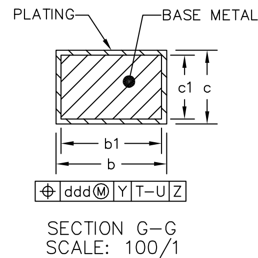




NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.



144-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

Figure 17: 144-Lead LQFP Pinout Diagram

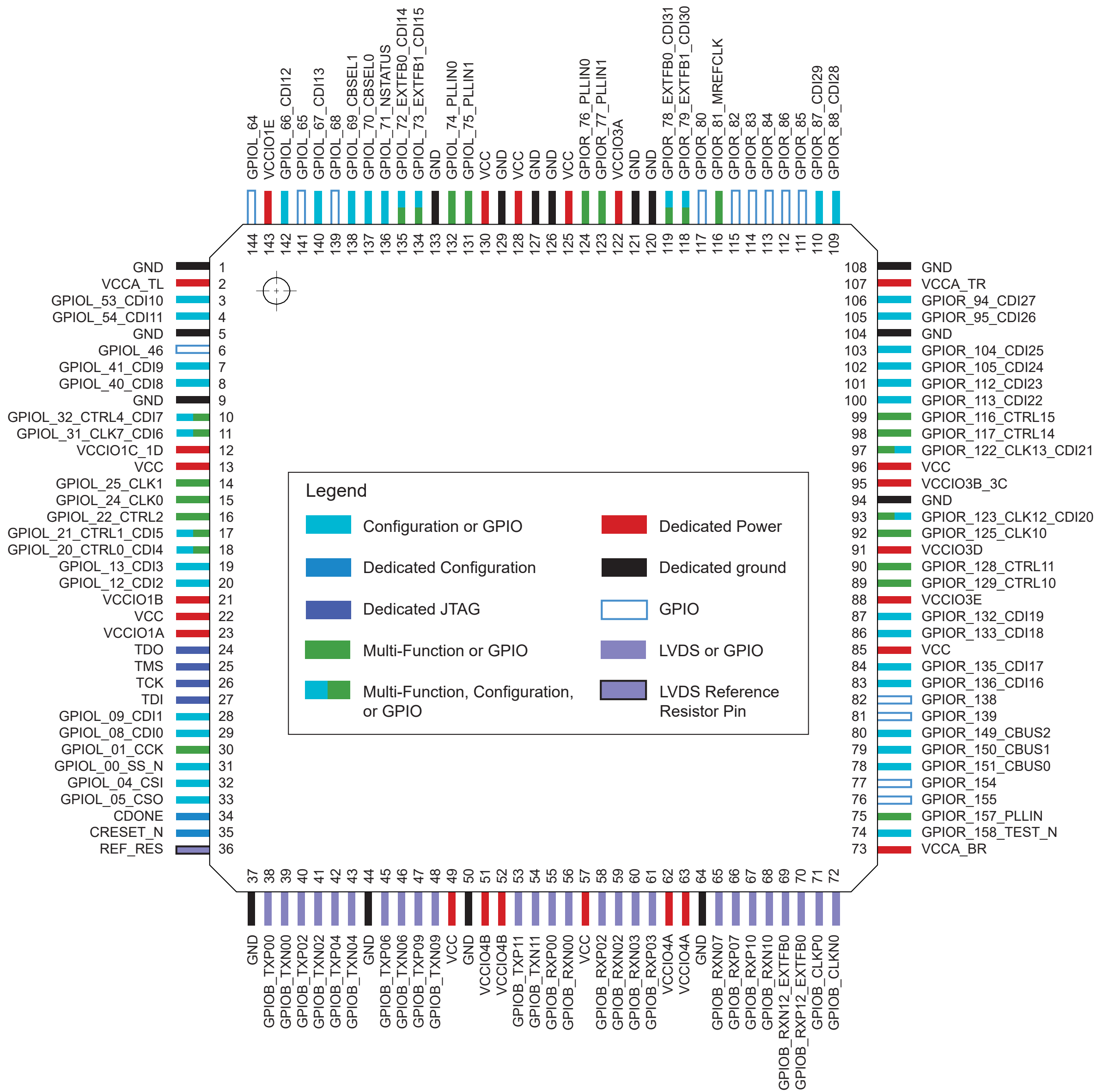


Figure 18: 144-Lead LQFP I/O Bank Diagram

Left side (pins 1–36):

Pin	Name
1	GND
2	VCCA_TL
3	GPIOL_53_CDI10
4	GPIOL_54_CDI11
5	GND
6	GPIOL_46
7	GPIOL_41_CDI9
8	GPIOL_40_CDI8
9	GND
10	GPIOL_32_CTRL4_CDI7
11	GPIOL_31_CLK7_CDI6
12	VCCIO1C_1D
13	VCC
14	GPIOL_25_CLK1
15	GPIOL_24_CLK0
16	GPIOL_22_CTRL2
17	GPIOL_21_CTRL1_CDI5
18	GPIOL_20_CTRL0_CDI4
19	GPIOL_13_CDI3
20	GPIOL_12_CDI2
21	VCCIO1B
22	VCC
23	VCCIO1A
24	TDO
25	TMS
26	TCK
27	TDI
28	GPIOL_09_CDI1
29	GPIOL_08_CDI0
30	GPIOL_01_CCK
31	GPIOL_00_SS_N
32	GPIOL_04_CSI
33	GPIOL_05_CSO
34	CDONE
35	CRESET_N
36	REF_RES

Bottom side (pins 37–72):

Pin	Name
37	GND
38	GPIOB_TXP00
39	GPIOB_TXN00
40	GPIOB_TXP02
41	GPIOB_TXN02
42	GPIOB_TXP04
43	GPIOB_TXN04
44	GND
45	GPIOB_TXP06
46	GPIOB_TXN06
47	GPIOB_TXP09
48	GPIOB_TXN09
49	VCC
50	GND
51	VCCIO4B
52	VCCIO4B
53	GPIOB_TXP11
54	GPIOB_TXN11
55	GPIOB_RXP00
56	GPIOB_RXN00
57	VCC
58	GPIOB_RXP02
59	GPIOB_RXN02
60	GPIOB_RXN03
61	GPIOB_RXP03
62	VCCIO4A
63	VCCIO4A
64	GND
65	GPIOB_RXN07
66	GPIOB_RXP07
67	GPIOB_RXP10
68	GPIOB_RXN10
69	GPIOB_RXN12_EXTFB0
70	GPIOB_RXP12_EXTFB0
71	GPIOB_CLKP0
72	GPIOB_CLKN0

Right side (pins 73–108):

Pin	Name
73	VCCA_BR
74	GPIOR_158_TEST_N
75	GPIOR_157_PLLIN
76	GPIOR_155
77	GPIOR_154
78	GPIOR_151_CBUS0
79	GPIOR_150_CBUS1
80	GPIOR_149_CBUS2
81	GPIOR_139
82	GPIOR_138
83	GPIOR_136_CDI16
84	GPIOR_135_CDI17
85	VCC
86	GPIOR_133_CDI18
87	GPIOR_132_CDI19
88	VCCIO3E
89	GPIOR_129_CTRL10
90	GPIOR_128_CTRL11
91	VCCIO3D
92	GPIOR_125_CLK10
93	GPIOR_123_CLK12_CDI20
94	GND
95	VCCIO3B_3C
96	VCC
97	GPIOR_122_CLK13_CDI21
98	GPIOR_117_CTRL14
99	GPIOR_116_CTRL15
100	GPIOR_113_CDI22
101	GPIOR_112_CDI23
102	GPIOR_105_CDI24
103	GPIOR_104_CDI25
104	GND
105	GPIOR_95_CDI26
106	GPIOR_94_CDI27
107	VCCA_TR
108	GND

Top side (pins 109–144):

Pin	Name
109	GPIOR_88_CDI28
110	GPIOR_87_CDI29
111	GPIOR_85
112	GPIOR_86
113	GPIOR_84
114	GPIOR_83
115	GPIOR_82
116	GPIOR_81_MREFCLK
117	GPIOR_80
118	GPIOR_79_EXTFB1_CDI30
119	GPIOR_78_EXTFB0_CDI31
120	GND
121	GND
122	VCCIO3A
123	GPIOR_77_PLLIN1
124	GPIOR_76_PLLIN0
125	VCC
126	GND
127	GND
128	VCC
129	GND
130	VCC
131	GPIOL_75_PLLIN1
132	GPIOL_74_PLLIN0
133	GND
134	GPIOL_73_EXTFB1_CDI15
135	GPIOL_72_EXTFB0_CDI14
136	GPIOL_71_NSTATUS
137	GPIOL_70_CBSEL0
138	GPIOL_69_CBSEL1
139	GPIOL_68
140	GPIOL_67_CDI13
141	GPIOL_65
142	GPIOL_66_CDI12
143	VCCIO1E
144	GPIOL_64

Legend

- Bank 1A
- Bank 1A VCCIO
- Bank 1B
- Bank 1B VCCIO
- Bank 1C, 1D
- Bank 1C_1D VCCIO
- Bank 1E
- Bank 1E VCCIO
- Bank 3A
- Bank 3A VCCIO
- Bank 3B, 3C
- Bank 3B_3C VCCIO
- Bank 3D
- Bank 3D VCCIO
- Bank 3E
- Bank 3E VCCIO
- Bank 4A
- Bank 4A VCCIO
- Bank 4B
- Bank 4B VCCIO
- Other dedicated Power and Ground

Figure 19: 144-Lead LQFP FPGA Package Marking

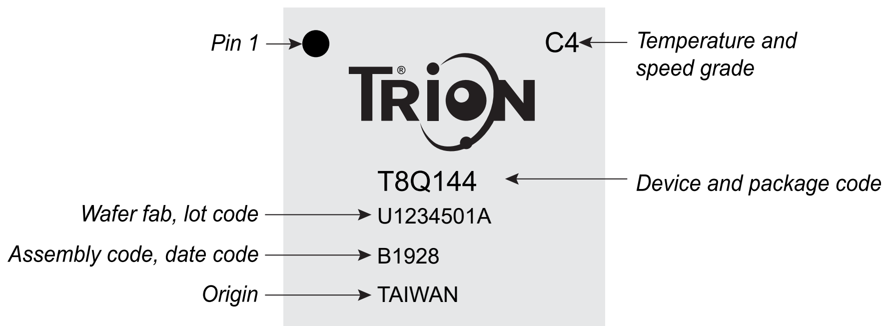
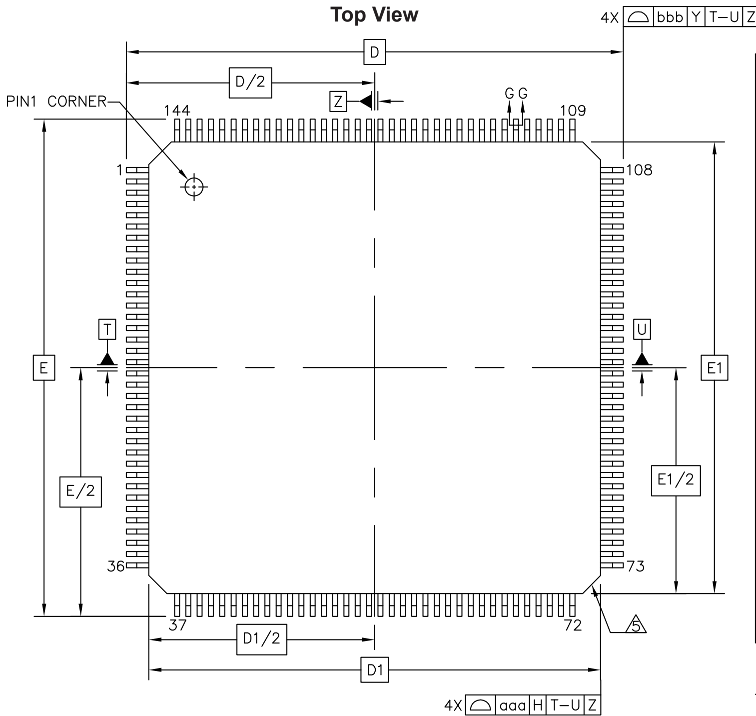
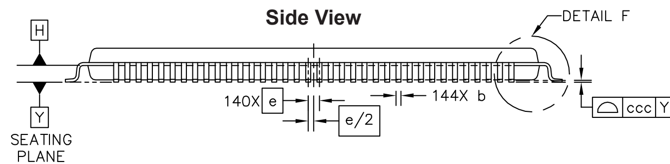
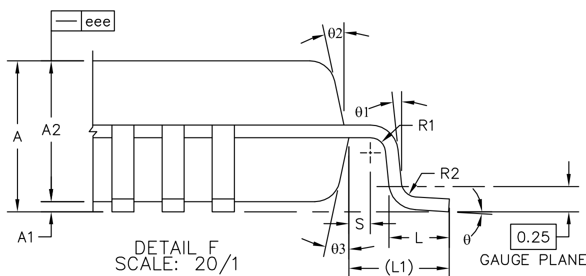


Figure 20: 144-Lead LQFP FPGA Package Outline





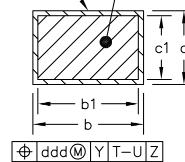


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	22 BSC		
	Y	E	22 BSC		
BODY SIZE	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

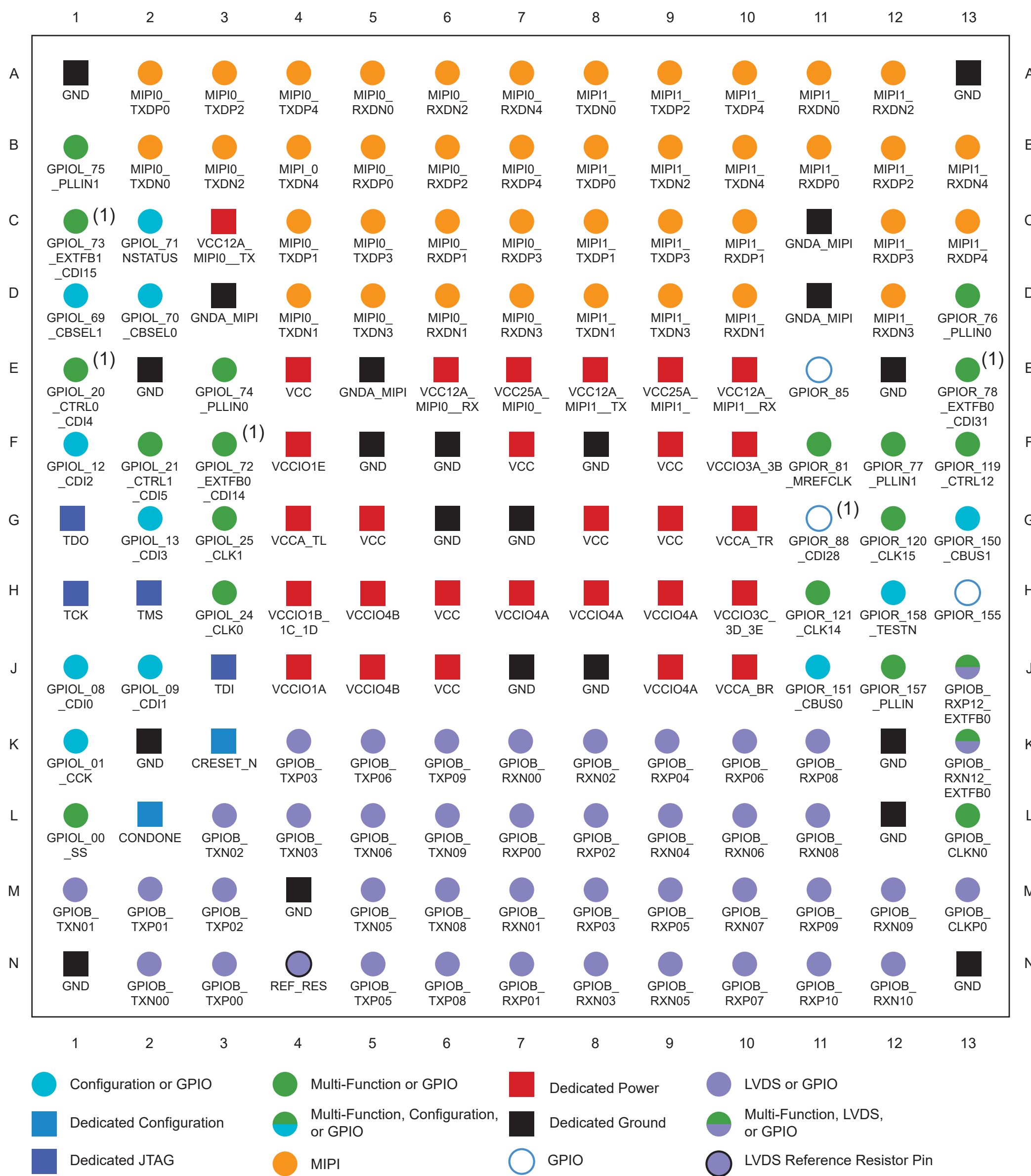
5. EXACT SHAPE OF EACH CORNER IS OPTIONAL.



169-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 21: 169-Ball FBGA Pinout Diagram



Note (1) In this package, this pin is not used for configuration functions.

Figure 22: 169-Ball FBGA I/O Bank Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	MIPI0_ TXDP0	MIPI0_ TXDP2	MIPI0_ TXDP4	MIPI0_ RXDN0	MIPI0_ RXDN2	MIPI0_ RXDN4	MIPI1_ TXDN0	MIPI1_ TXDP2	MIPI1_ TXDP4	MIPI1_ RXDN0	MIPI1_ RXDN2	GND
B	GPIOL_75 _PLLIN1	MIPI0_ TXDN0	MIPI0_ TXDN2	MIPI_0 TXDN4	MIPI0_ RXDP0	MIPI0_ RXDP2	MIPI0_ RXDP4	MIPI1_ TXDP0	MIPI1_ TXDN2	MIPI1_ TXDN4	MIPI1_ RXDP0	MIPI1_ RXDP2	MIPI1_ RXDN4
C	GPIOL_73 _EXTFB1 _CDI15	GPIOL_71 NSTATUS	VCC12A_ MIPI0__TX	MIPI0_ TXDP1	MIPI0_ TXDP3	MIPI0_ RXDP1	MIPI0_ RXDP3	MIPI1_ TXDP1	MIPI1_ TXDP3	MIPI1_ RXDP1	GNDA_MIPI	MIPI1_ RXDP3	MIPI1_ RXDP4
D	GPIOL_69 _CBSEL1	GPIOL_70 _CBSEL0	GNDA_MIPI	MIPI0_ TXDN1	MIPI0_ TXDN3	MIPI0_ RXDN1	MIPI0_ RXDN3	MIPI1_ TXDN1	MIPI1_ TXDN3	MIPI1_ RXDN1	GNDA_MIPI	MIPI1_ RXDN3	GPIOR_76 _PLLIN0
E	GPIOL_20 _CTRL0 _CDI4	GND	GPIOL_74 _PLLIN0	VCC	GNDA_MIPI	VCC12A_ MIPI0__RX	VCC25A_ MIPI0_	VCC12A_ MIPI1__TX	VCC25A_ MIPI1_	VCC12A_ MIPI1__RX	GPIOR_85	GND	GPIOR_78 _EXTFB0 _CDI31
F	GPIOL_12 _CDI2	GPIOL_21 _CTRL1 _CDI5	GPIOL_72 _EXTFB0 _CDI14	VCCIO1E	GND	GND	VCC	GND	VCC	VCCIO3A_3B	GPIOR_81 _MREFCLK	GPIOR_77 _PLLIN1	GPIOR_119 _CTRL12
G	TDO	GPIOL_13 _CDI3	GPIOL_25 _CLK1	VCCA_TL	VCC	GND	GND	VCC	VCC	VCCA_TR	GPIOR_88 _CDI28	GPIOR_120 _CLK15	GPIOR_150 _CBUS1
H	TCK	TMS	GPIOL_24 _CLK0	VCCIO1B_ 1C_1D	VCCIO4B	VCC	VCCIO4A	VCCIO4A	VCCIO4A	VCCIO3C_ 3D_3E	GPIOR_121 _CLK14	GPIOR_158 _TESTN	GPIOR_155
J	GPIOL_08 _CDI0	GPIOL_09 _CDI1	TDI	VCCIO1A	VCCIO4B	VCC	GND	GND	VCCIO4A	VCCA_BR	GPIOR_151 _CBUS0	GPIOR_157 _PLLIN	GPIOB_ RXP12_ EXTFB0
K	GPIOL_01 _CCK	GND	CRESET_N	GPIOB_ TXP03	GPIOB_ TXP06	GPIOB_ TXP09	GPIOB_ RXN00	GPIOB_ RXN02	GPIOB_ RXP04	GPIOB_ RXP06	GPIOB_ RXP08	GND	GPIOB_ RXN12_ EXTFB0
L	GPIOL_00 _SS	CONDONE	GPIOB_ TXN02	GPIOB_ TXN03	GPIOB_ TXN06	GPIOB_ TXN09	GPIOB_ RXP00	GPIOB_ RXP02	GPIOB_ RXN04	GPIOB_ RXN06	GPIOB_ RXN08	GND	GPIOB_ CLKN0
M	GPIOB_ TXN01	GPIOB_ TXP01	GPIOB_ TXP02	GND	GPIOB_ TXN05	GPIOB_ TXN08	GPIOB_ RXN01	GPIOB_ RXP03	GPIOB_ RXP05	GPIOB_ RXN07	GPIOB_ RXP09	GPIOB_ RXN09	GPIOB_ CLKP0
N	GND	GPIOB_ TXN00	GPIOB_ TXP00	REF_RES	GPIOB_ TXP05	GPIOB_ TXP08	GPIOB_ RXP01	GPIOB_ RXN03	GPIOB_ RXN05	GPIOB_ RXP07	GPIOB_ RXP10	GPIOB_ RXN10	GND

Bank 1A | Bank 1A VCCIO | Bank 2A | Bank 3A | Bank 3A_3B VCCIO | Bank 4A | Bank 4A VCCIO

Bank 1B | Bank 1B_1C_1D VCCIO | Bank 2B | Bank 3C | Bank 3C_3D_3E VCCIO | Bank 4B | Bank 4B VCCIO

Bank 1E | Bank 1E VCCIO | Other Dedicated Power and Ground

Figure 23: 169-Ball FPGA Package Marking

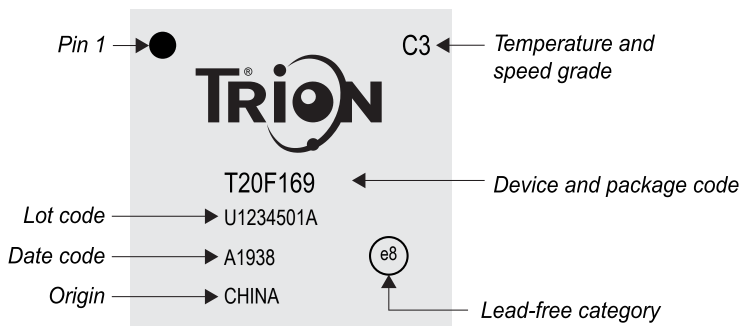
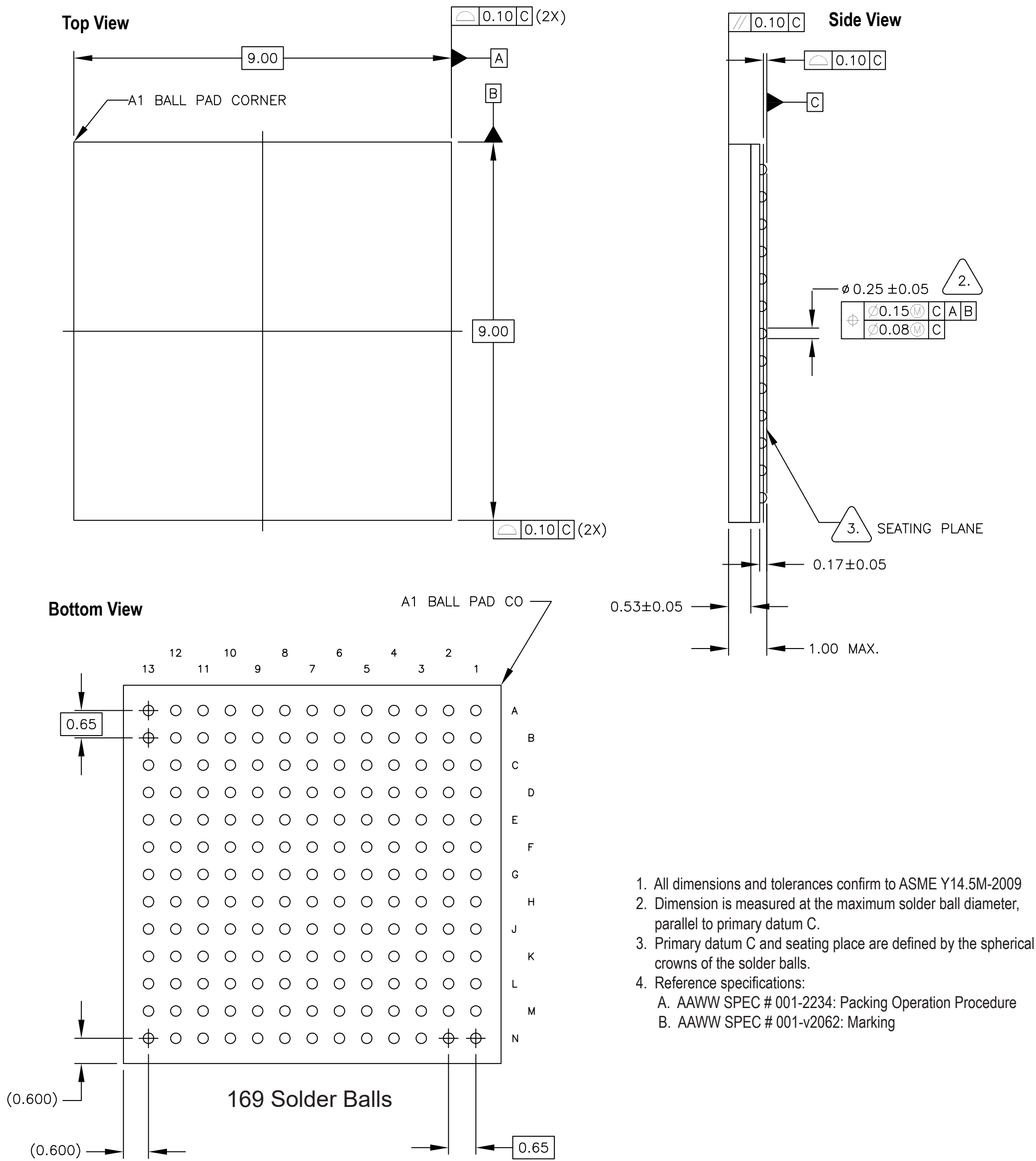


Figure 24: 169-Ball FBGA Package Outline



256-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 25: 256-Ball FBGA Pinout Diagram

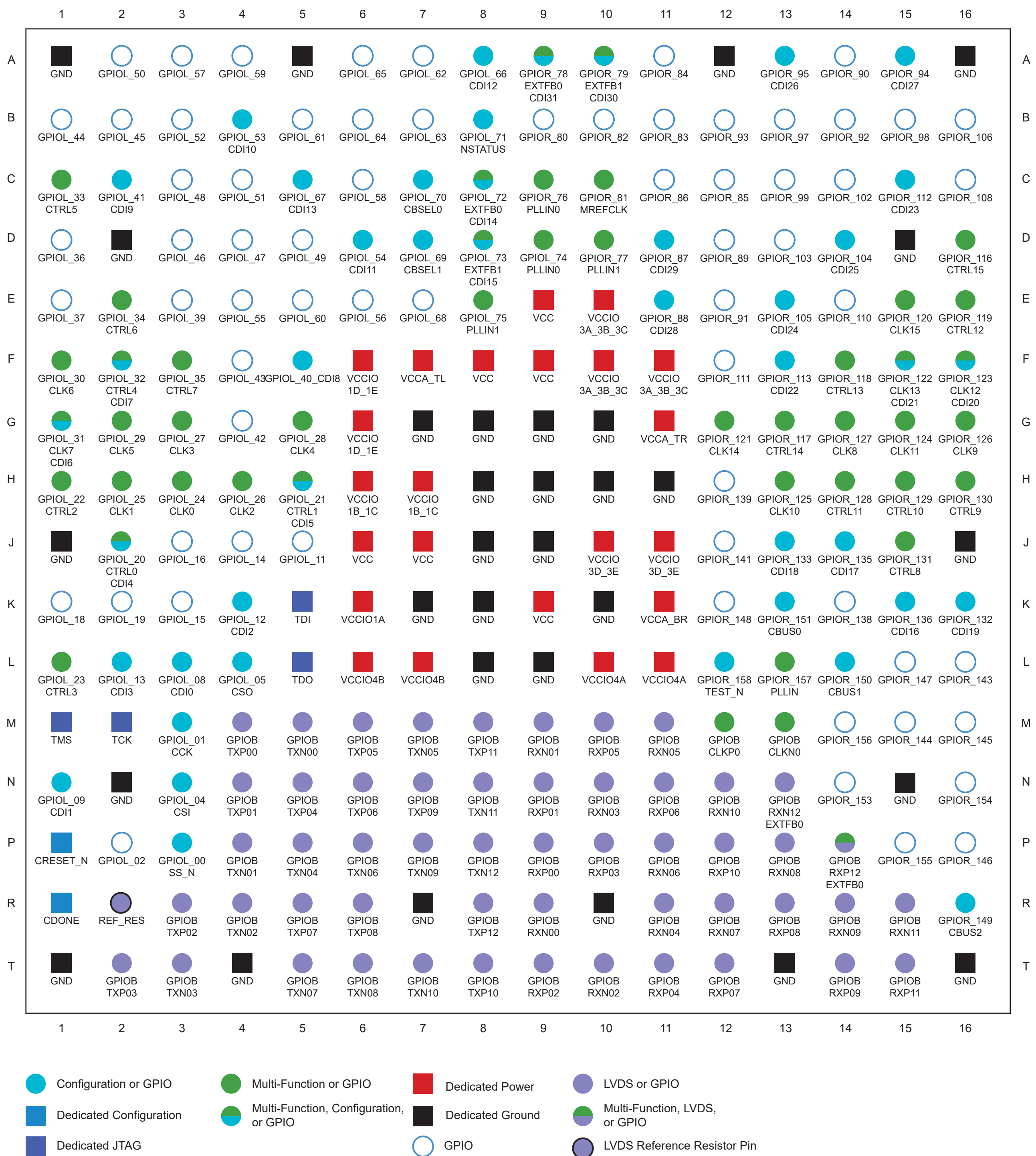


Figure 26: 256-Ball FBGA I/O Bank Diagram

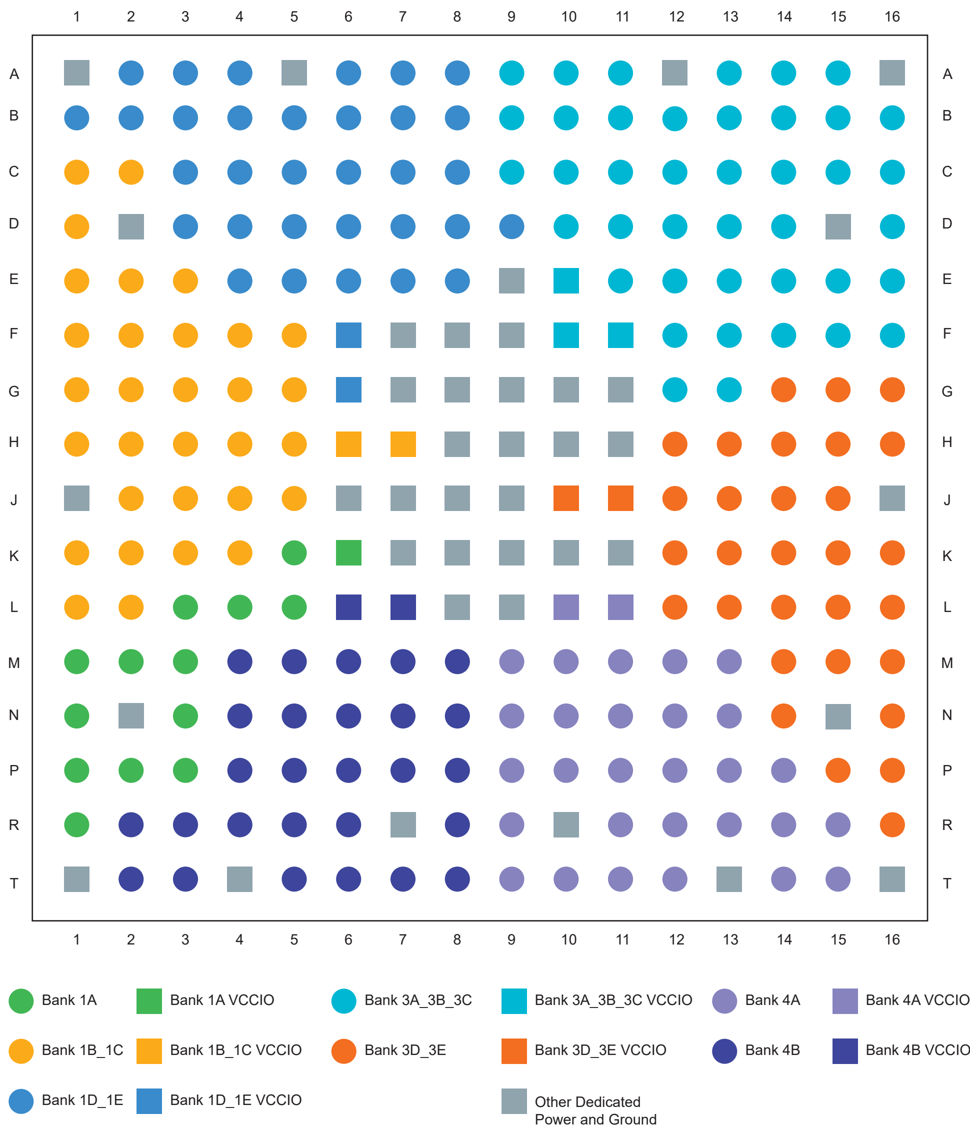


Figure 27: 256-Ball FPGA Package Marking

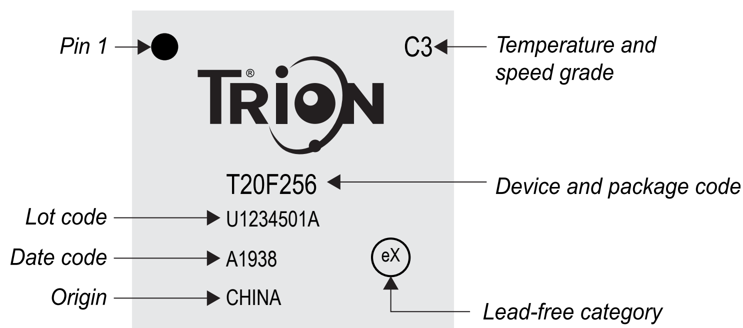
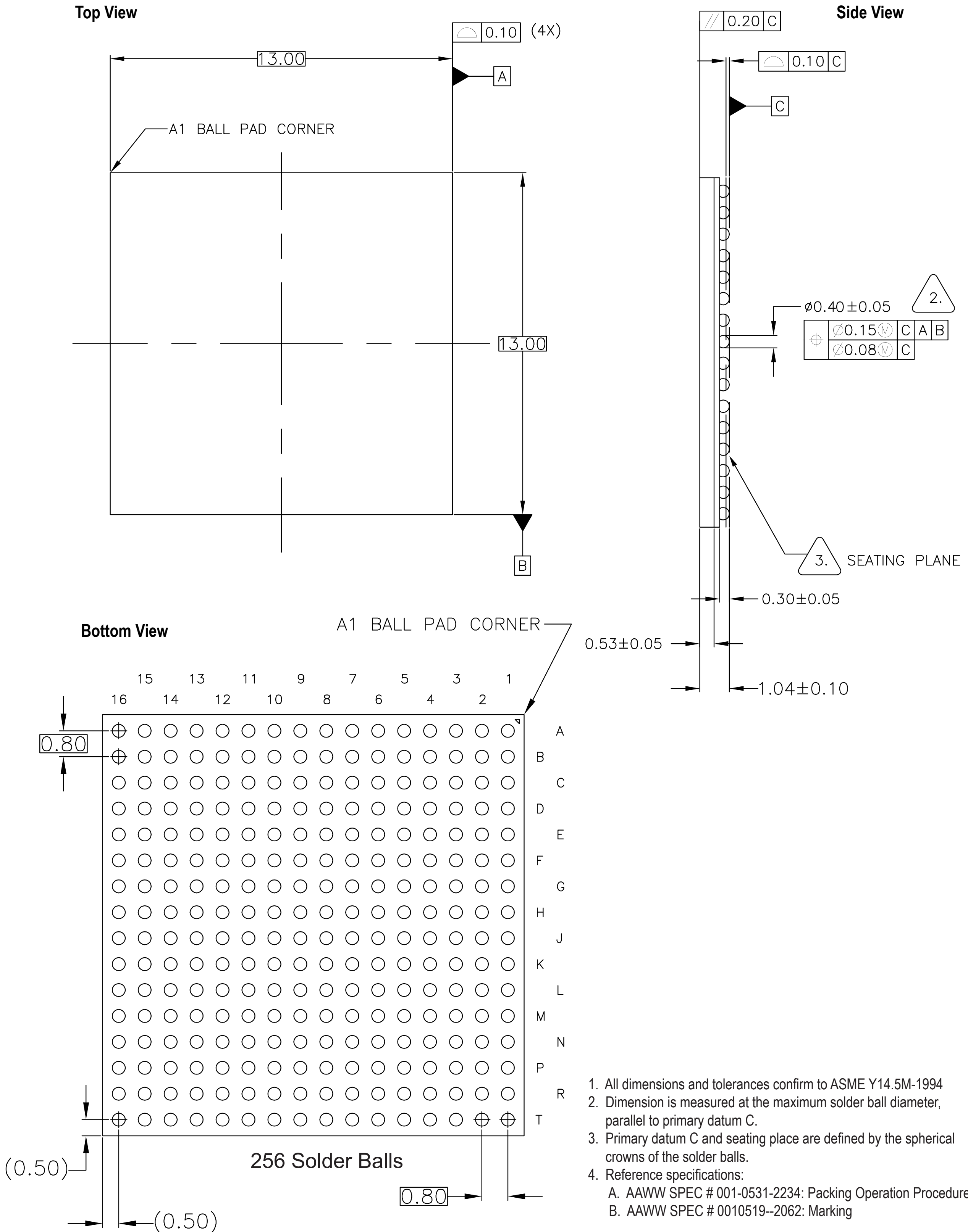


Figure 28: 256-Ball FBGA Package Outline



324-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package.

Note: Some pin names and I/O banks differ between T20/T35 and T55/T85/T120 FPGAs; however, you can still migrate between FPGAs in this package.

T20 and T35 FPGAs

Pinout and I/O Banks

Figure 29: 324-Ball FBGA Pinout Diagram (T20 and T35)

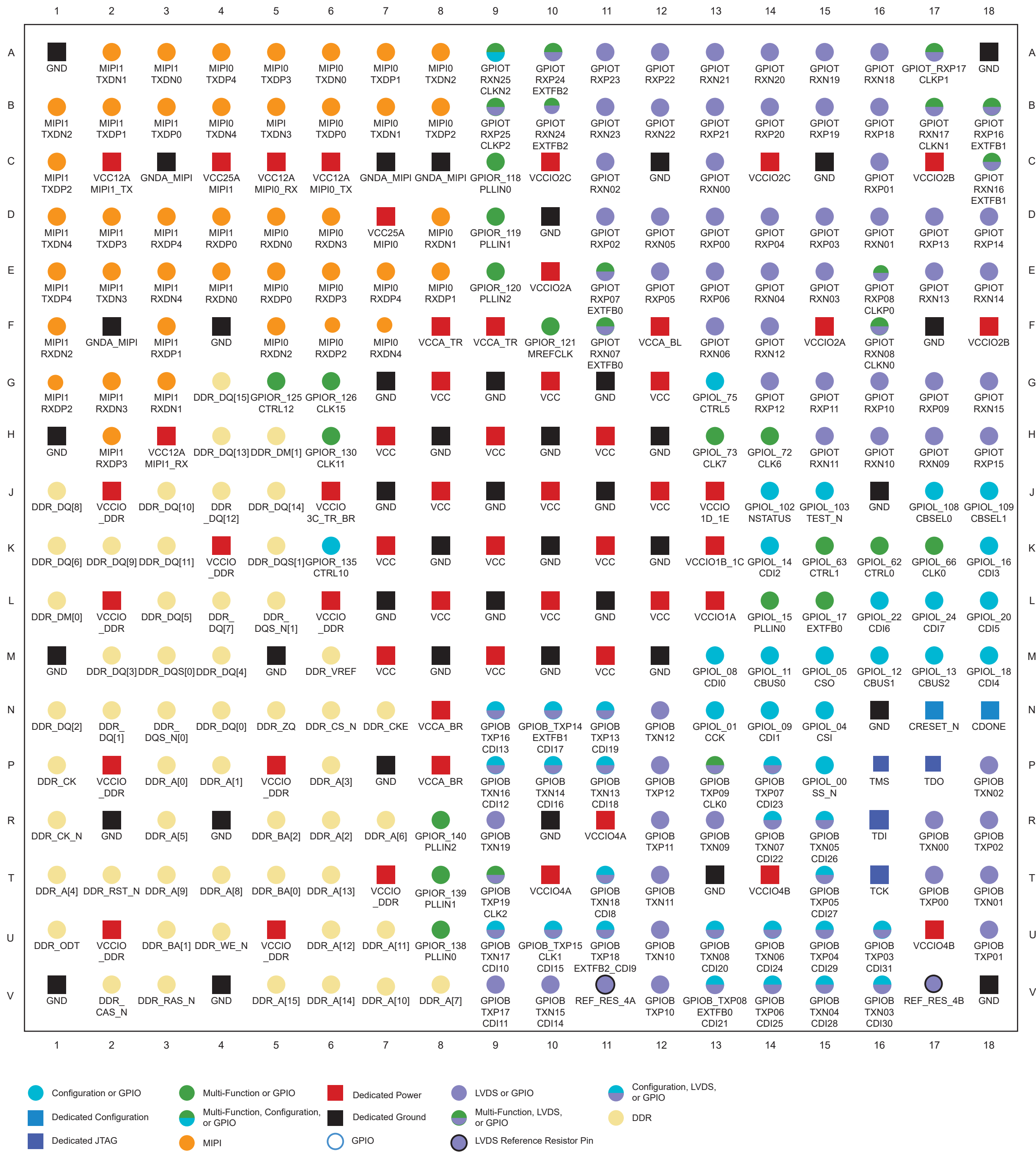
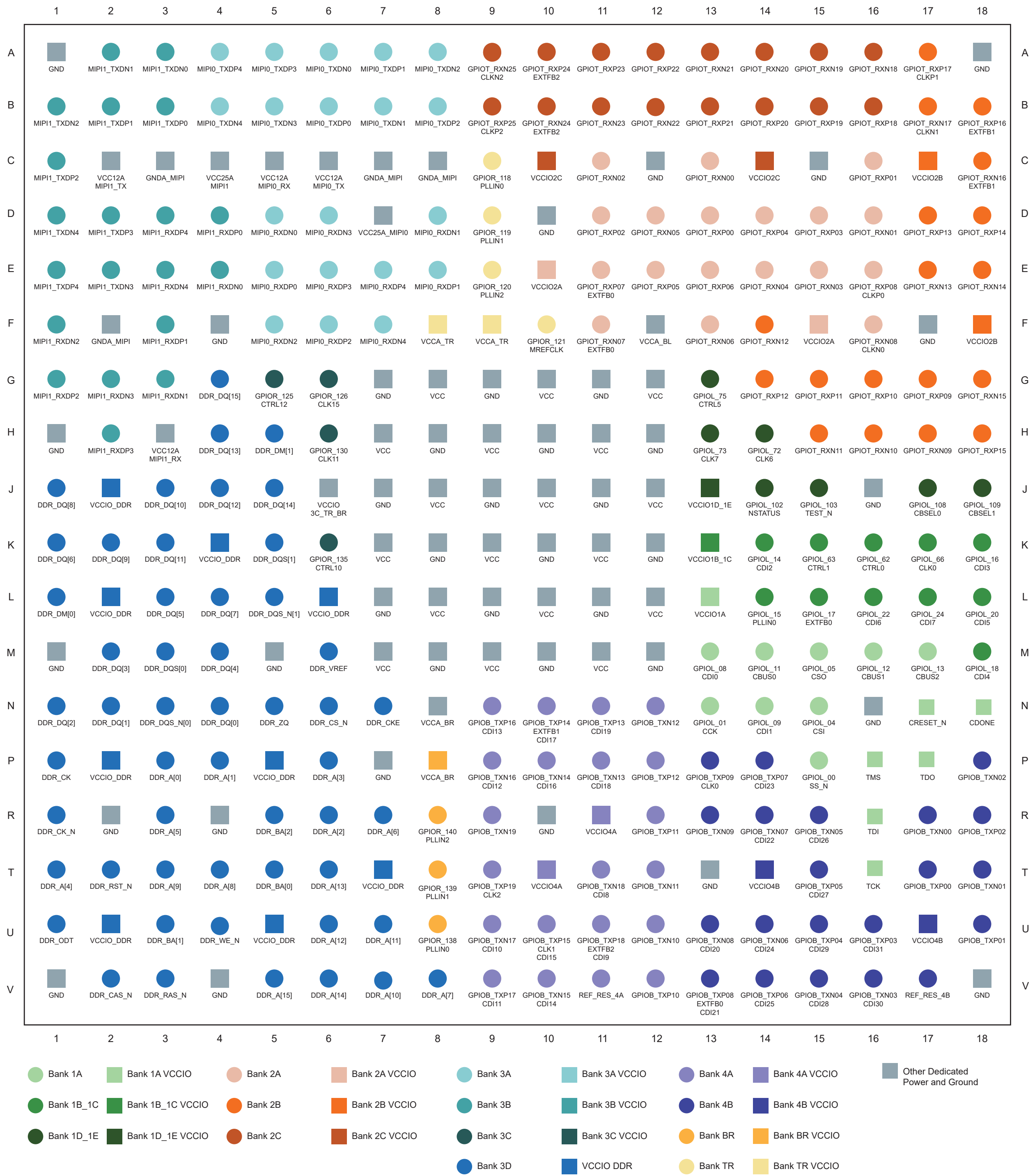


Figure 30: 324-Ball FBGA I/O Bank Diagram (T20 and T35)



Package Outline and Marking

Figure 31: 324-Ball FBGA Package Outline (T20 and T35)

Top View

0.10 (4X)
12.00
A
A1 BALL PAD CORNER
12.00
B

Side View

0.10 C
0.10 C
C
ϕ 0.30 ±0.03 2.
ϕ0.12 M C A M B M
ϕ0.05 M C
3. SEATING PLANE
0.173 MIN.
(0.223 NOM.)
0.40±0.04
0.97MAX

A1 BALL PAD CORNER
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R T U V
0.65
(0.48)
0.65
(0.48)

Bottom View
324 Solder balls

4. REFERENCE SPECIFICATIONS:
A. AAWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE
B. AAWW SPEC #001-0519-2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994

NOTES: UNLESS OTHERWISE SPECIFIED

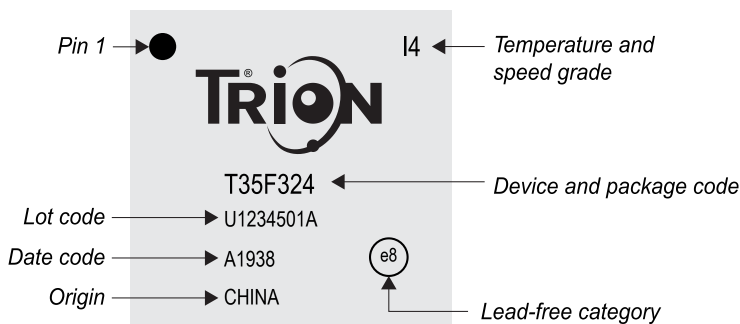
THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR
±1°

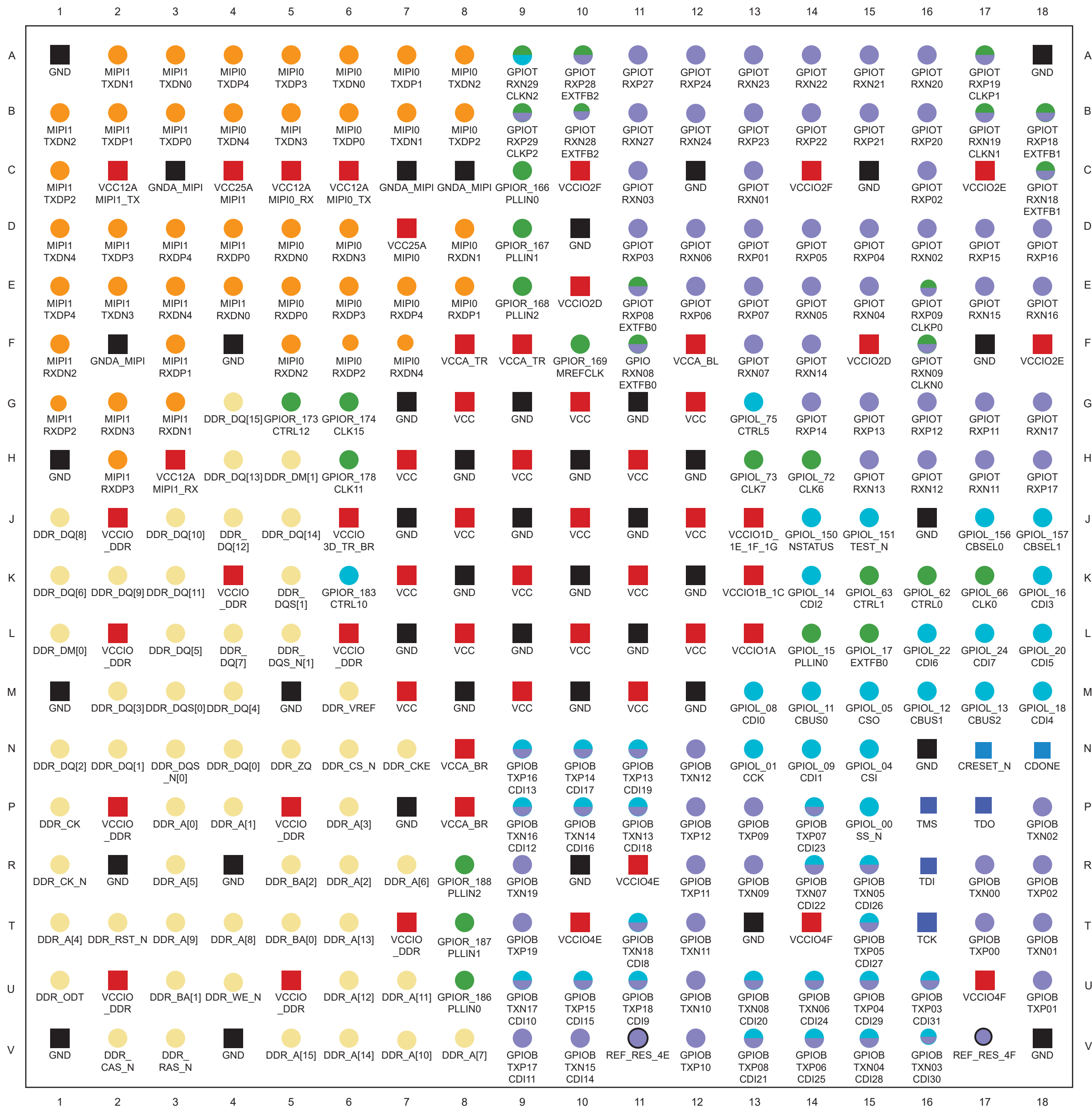
Figure 32: 324-Ball FPGA Package Marking (T20 and T35)



T55, T85, and T120 FPGAs

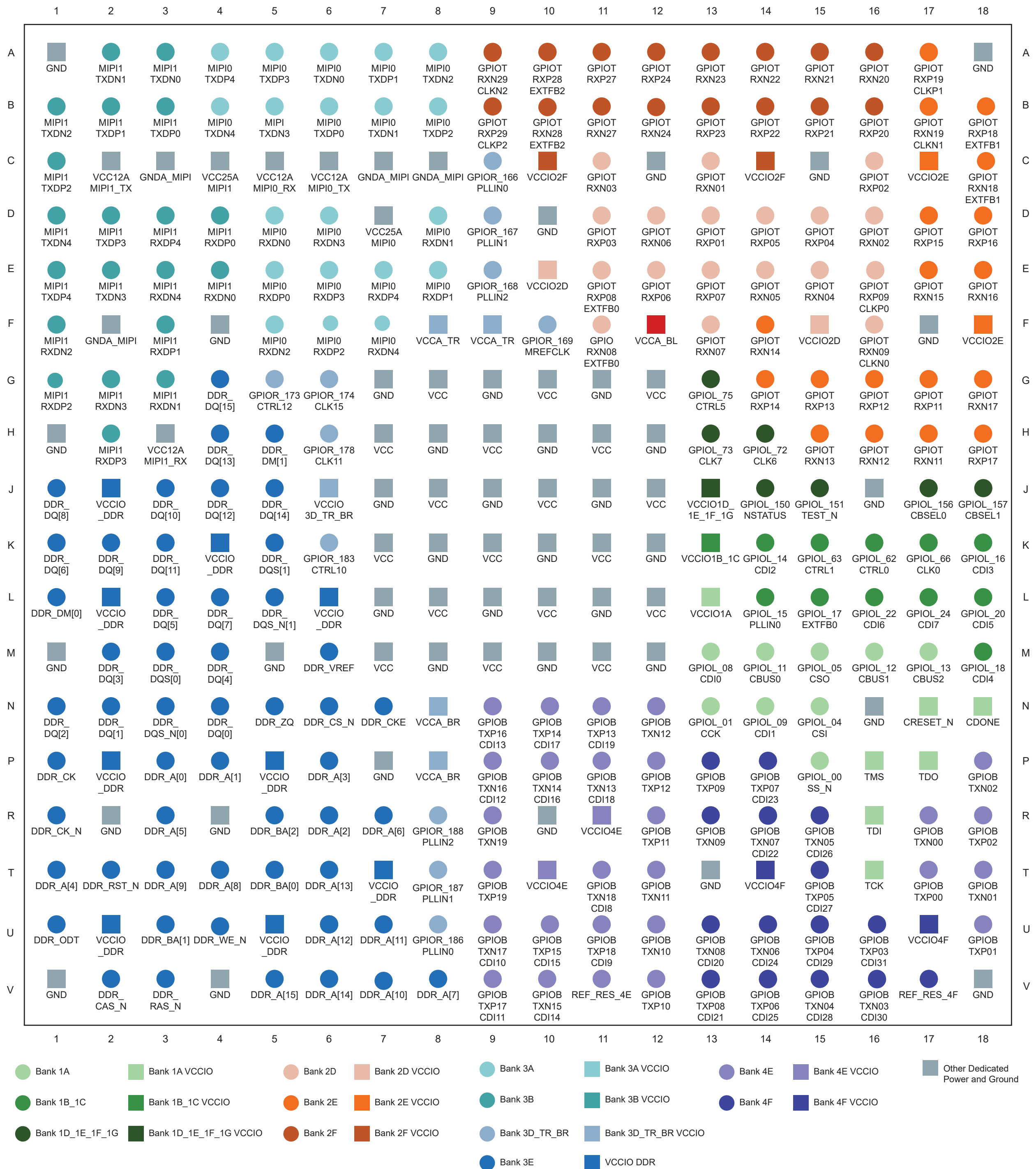
Pinout and I/O Banks

Figure 33: 324-Ball FBGA Pinout Diagram (T55, T85, and T120)



- Configuration or GPIO
- Dedicated Configuration
- Dedicated JTAG
- Multi-Function or GPIO
- Multi-Function, Configuration, or GPIO
- MIPI
- Dedicated Power
- Dedicated Ground
- GPIO
- LVDS or GPIO
- Multi-Function, LVDS, or GPIO
- LVDS Reference Resistor Pin
- Configuration, LVDS, or GPIO
- DDR

Figure 34: 324-Ball FBGA I/O Bank Diagram (T55, T85, and T120)



Package Outline and Marking

Figure 35: 324-Ball FBGA Package Outline (T55, T85, and T120)

Top View

0.10 (4X)
12.00
A
A1 BALL PAD CORNER
12.00
B

Side View

0.10 C
0.10 C
C
ϕ 0.30 ±0.03
2.
Ø0.12 M C A M B M
Ø0.05 M C
3. SEATING PLANE
0.173 MIN.
(0.223 NOM.)
0.40±0.04
1.07MAX

A1 BALL PAD CORNER
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R T U V
0.65
(0.48)
0.65
(0.48)

Bottom View
324 Solder balls

4. REFERENCE SPECIFICATIONS:
A. AAWW SPEC #001−0531−2234: PACKING OPERATION PROCEDURE
B. AAWW SPEC #001−0519−2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994

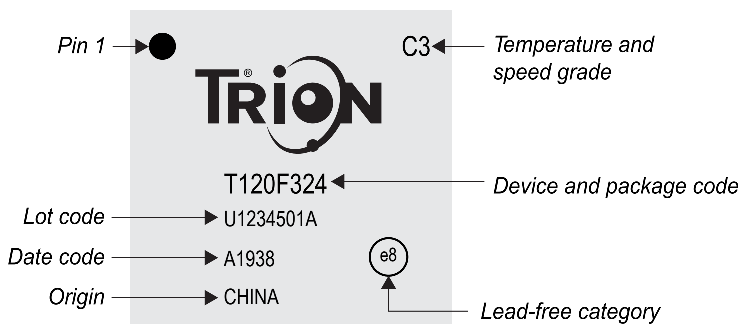
NOTES: UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS

DECIMAL	ANGULAR
X.X ±0.1	±1°
X.XX ±0.05	
X.XXX ±0.030	

Figure 36: 324-Ball FPGA Package Marking (T55, T85, and T120)



400-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

Figure 37: 400-Ball FBGA Pinout Diagram

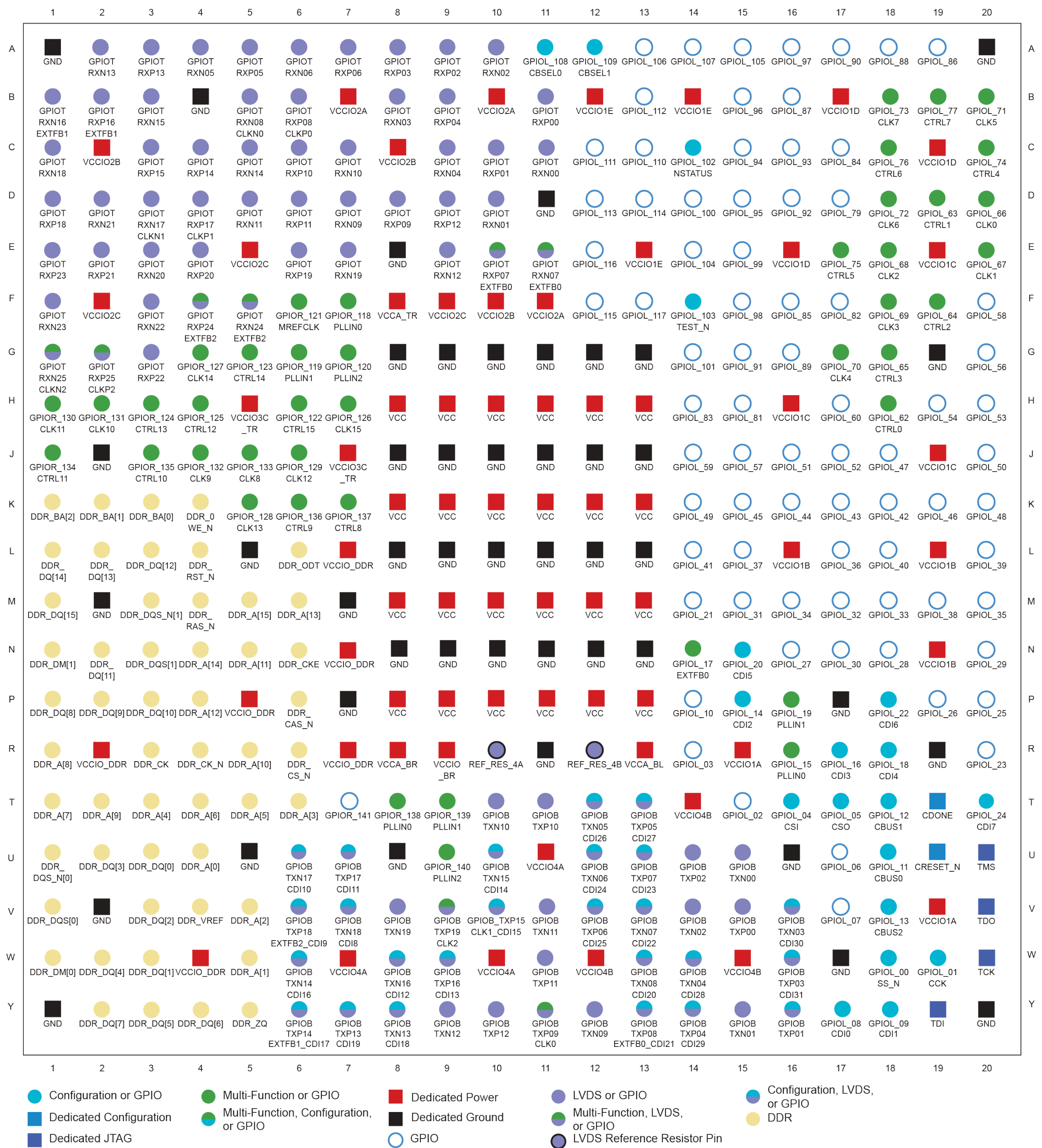


Figure 38: 400-Ball FBGA I/O Bank Diagram

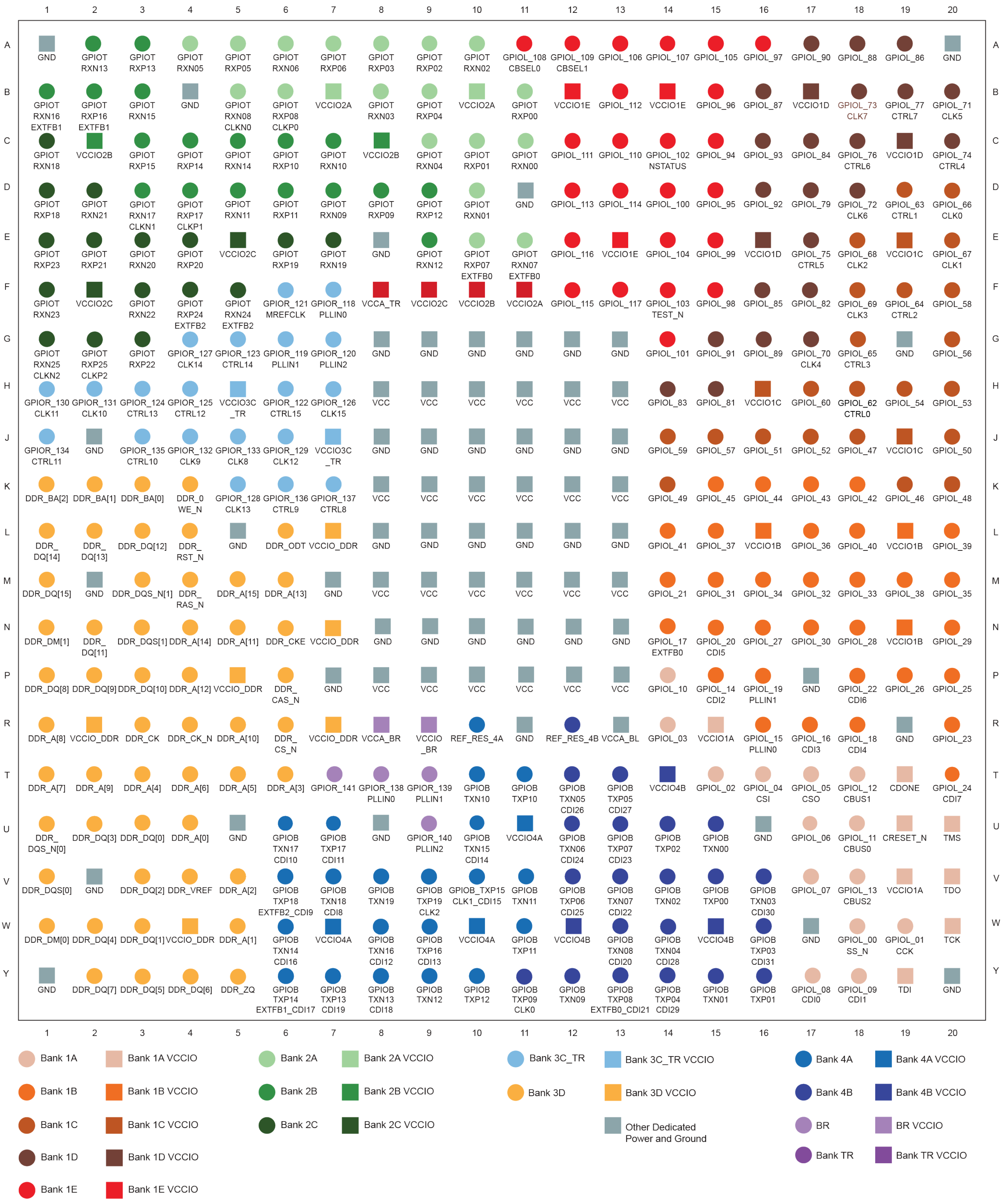


Figure 39: 400-Ball FBGA Package Outline

Top View

A1 BALL PAD CORNER

16.00

16.00

0.10 (2X) A

0.10 (2X) B

Side View

// 0.10 C

0.15 C

C

ø 0.30±0.05 2.

ø0.12 Ⓜ C A B

ø0.05 Ⓜ C

3. SEATING PLANE

0.53±0.05

0.173 MIN.
(0.223 NOM.)

1.10 MAX.

A1 BALL PAD CORNER

20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

A B C D E F G H J K L M N P R T U V W Y

0.80

(0.40)

(0.40)

0.80

Bottom View
400 Solder balls

4. REFERENCE SPECIFICATIONS:
A. AAWW SPEC #001–0531–2234: PACKING OPERATION PROCEDURE
B. AAWW SPEC #001–0519–2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994

NOTES: UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

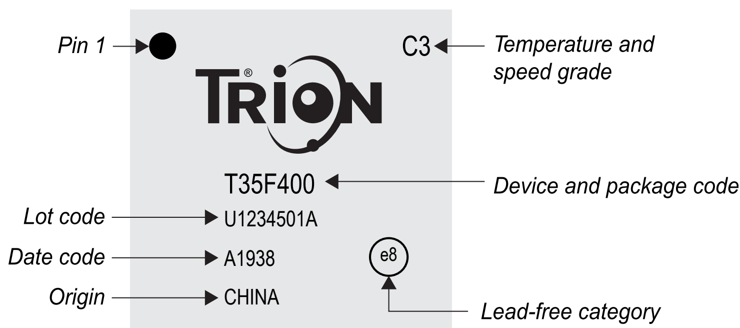
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR
±1°

INTERPRET DIM AND TOL PER
ASME Y14.5M – 1994

Figure 40: 400-Ball FPGA Package Marking



484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 41: 484-Ball FBGA Pinout Diagram

Figure 42: 484-Ball FBGA I/O Bank Diagram

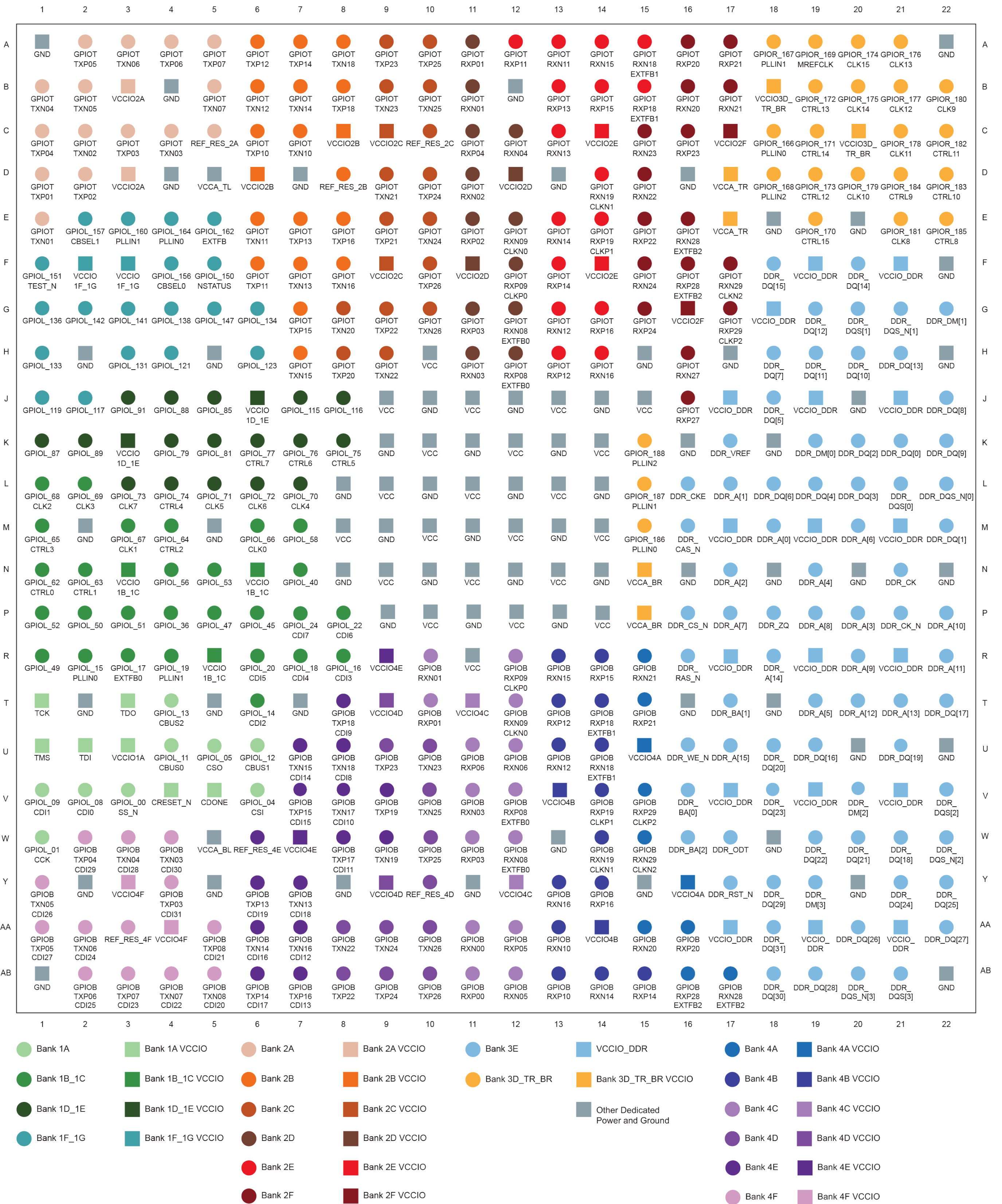


Figure 43: 484-Ball FBGA Package Outline

Top View

18.00

TERMINAL A1 CORNER INDEX AREA

18.00

0.15 C (2X)

A

B

Side View

0.10 C

0.15 C

C

ø0.40±0.05

ø0.15 Ⓜ C A B

ø0.08 Ⓜ C

3. SEATING PLANE

0.21 MIN. (0.31 NOM.)

0.70±0.05

1.22±0.100

A1 BALL PAD CORNER

0.80

(0.600)

(0.600)

0.80

Bottom View
484 Solder balls

4. REFERENCE SPECIFICATIONS:
A. AAWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE
B. AAWW SPEC #001-0519-2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994

NOTES: UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

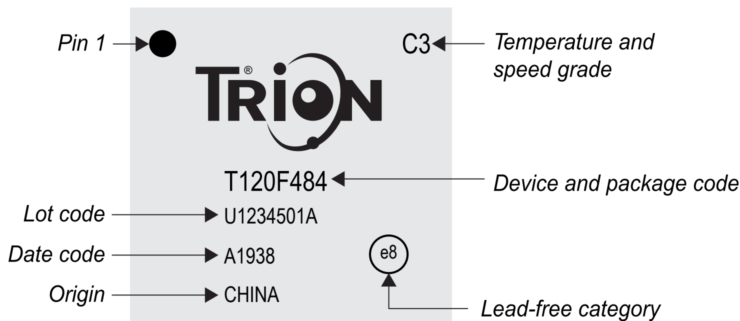
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR
±1°

INTERPRET DIM AND TOL PER ASME Y14.5M – 1994

Figure 44: 484-Ball FPGA Package Marking



576-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

Figure 45: 576-Ball FBGA Pinout Diagram

Figure 46: 576-Ball FBGA I/O Bank Diagram

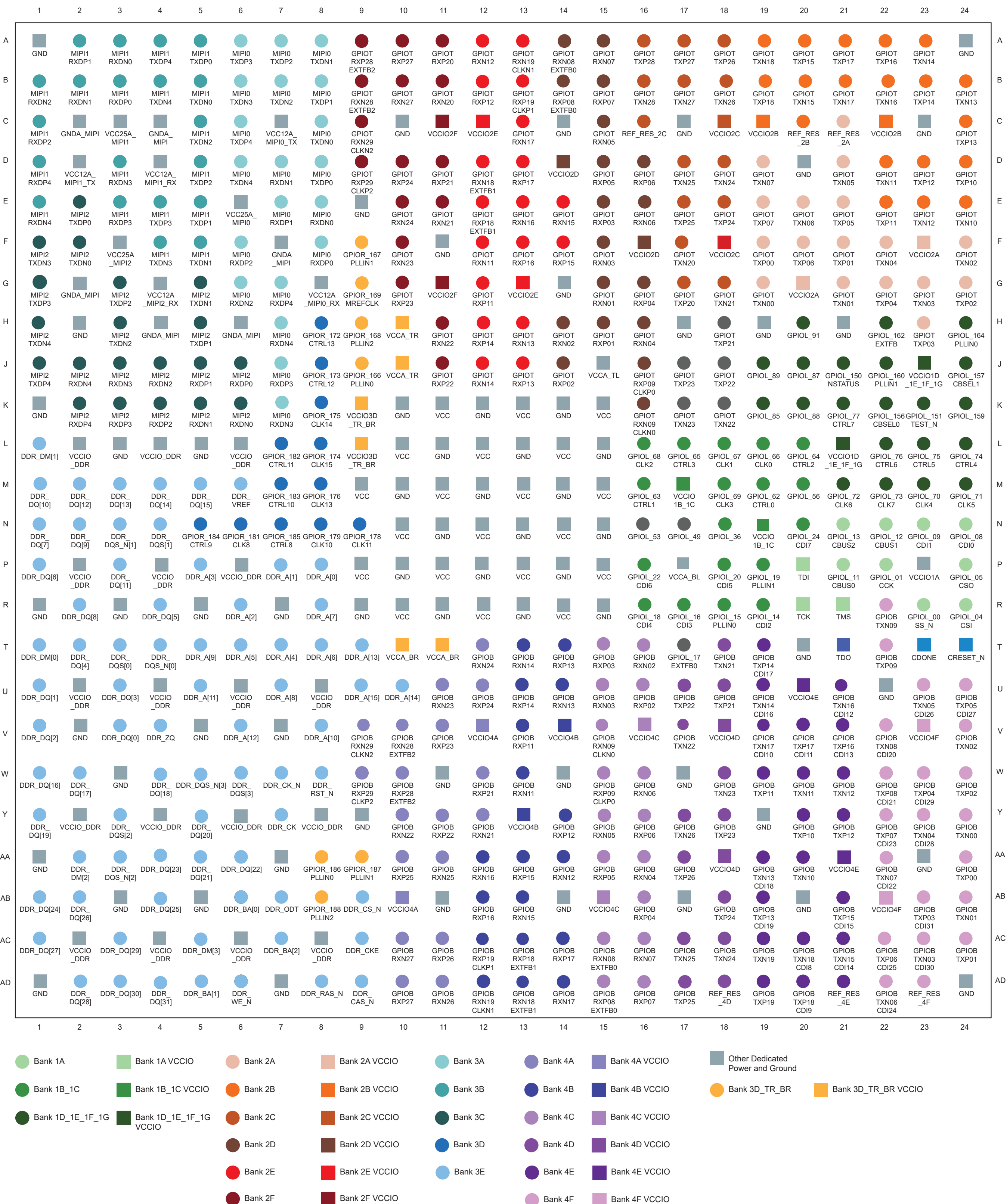


Figure 47: 576-Ball FBGA Package Outline

Top View

Side View

A1 BALL PAD CORNER

16.00

16.00

0.10 (4X)

A

B

0.10 C

0.10 C

C

ϕ 0.30 ±0.03 (2.)

ϕ0.12Ⓜ C AⓂ BⓂ

ϕ0.05Ⓜ C

(3.) SEATING PLANE

0.173 MIN.
(0.223 NOM.)

1.20MAX

0.53±0.04

A1 BALL PAD CORNER

24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

A B C D E F G H J K L M N P R T U V W Y AA AB AC AD

0.65

(0.53)

0.65

(0.53)

Bottom View
576 Solder balls

4. REFERENCE SPECIFICATIONS:
   A. AAWW SPEC #001–0531–2234: PACKING OPERATION PROCEDURE
   B. AAWW SPEC #001–0519–2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994

NOTES: UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

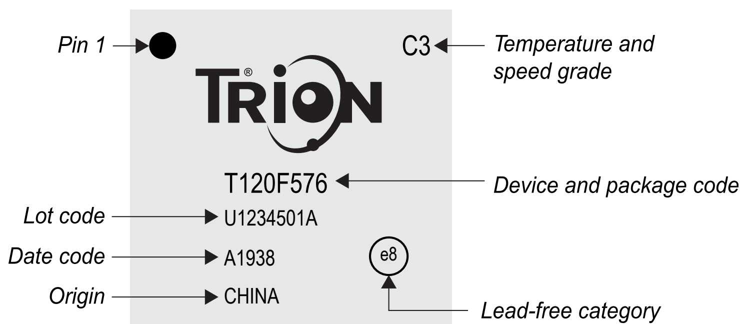
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.030

ANGULAR
±1°

INTERPRET DIM AND TOL PER ASME Y14.5M – 1994

Figure 48: 576-Ball FPGA Package Marking



Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for Elitestek® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its profile, which depends upon the board design and the reflow equipment used. You must characterize each PCB to find a reliable profile.

Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

Elitestek does not recommend BGA reballing. Reballed BGA packages will void the original Elitestek® specifications.

Peak Reflow Temperatures

Table 8: Peak Reflow Temperature (T_p) by Package

Package	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
FBGA	49	3	260
WLCSP	80	1	260
FBGA	81	3	260
LQFP	100	3	260
FBGA	169	3	260
FBGA	256	3	260
FBGA	324	3	260
FBGA	400	3	260
FBGA	484	3	260
FBGA	576	3	260
LQFP	144	3	260

Table 9: Peak Reflow Temperature (T_p) by Package

Package	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
FBGA	3	260

Note: These packages are "green" and RoHS compliant.

Reflow Profile for SMT Packages

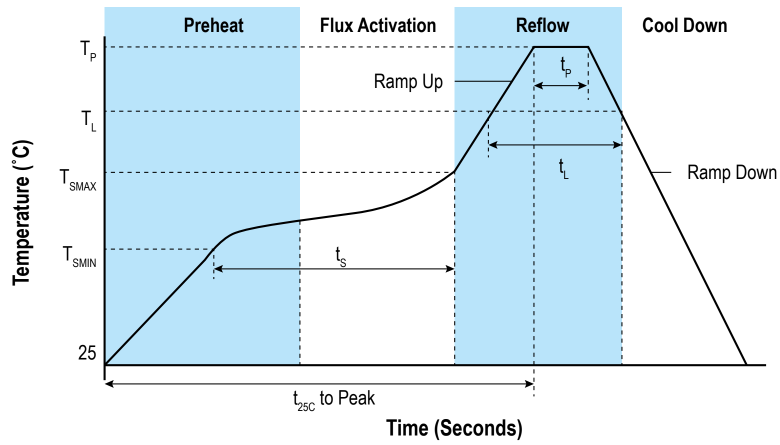
The reflow process usually includes four phases:

1. **Preheat Phase**—The preheat phase brings the assembly from 25 °C to T_S. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
    - **Solder Ball Spattering**—Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
    - **Bridging**—Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase**—As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase**—The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase**—Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 10: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_P	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
t_{25C} to T_p	Time from 25 °C to peak temperature	8 minutes maximum

Figure 49: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. Elitestek® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors, such as die size, paddle size, airflow, power applied, printed circuit board design, the proximity of other devices, and user applications. Because of this, Elitestek FPGAs do not come with preset thermal solutions.

Table 11: Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Θ_{JA}/W Still Air	Θ_{JA} (200 LFM)/W	Θ_{JA} (500 LFM)/W	Θ_{JB}/W	Θ_{JC}/W
T4, T8	FBGA49	3 x 3	90.446	84.782	81.797	56.464	46.431
	FBGA81	5 x 5	80.476	75.363	72.797	55.352	32.583
T8, T20	LQFP144	20 x 20	42.82	37.68	35.50	31.12	10.51
T13, T20	LQFP100	14 x 14	51.29	45.64	43.40	37.70	15.21
	FBGA169	9 x 9	38.25	33.33	31.60	23.64	12.39
	FBGA256	13 x 13	24.24	20.52	17.59	31.57	11.85
T20	WLCSP80	4.5 x 3.5	44.94	39.35	37.54	18.91	0.12
T20, T35	FBGA324	12 x 12	20.69	17.89	16.89	10.12	2.59
	FBGA400	16 x 16	18.70	16.95	15.92	12.45	11.10
T55, T85, T120	FBGA324	12 x 12	16.9	14.4	13.5	8.04	2.01
	FBGA484	18 x 18	15.85	12.83	11.99	6.10	4.10
	FBGA576	16 x 16	15.376	13.648	12.568	6.601	1.712

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance
- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

PCB Guidelines for BGA Packages

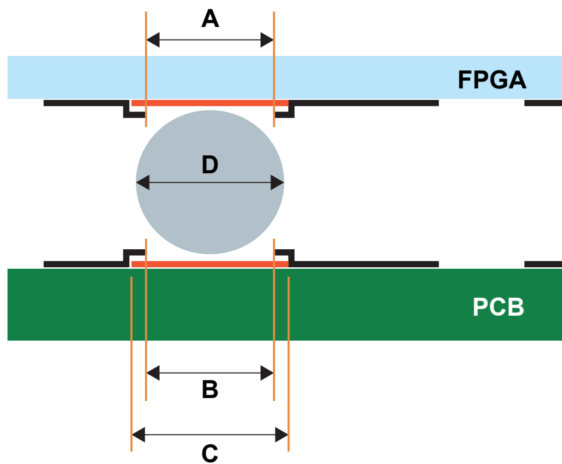
PCB Solder Pad Guidelines

Elitestek provides solder mask defined (SMD) and non-solder mask defined (NSMD) diameter information. Use this data when creating your board landing pads.

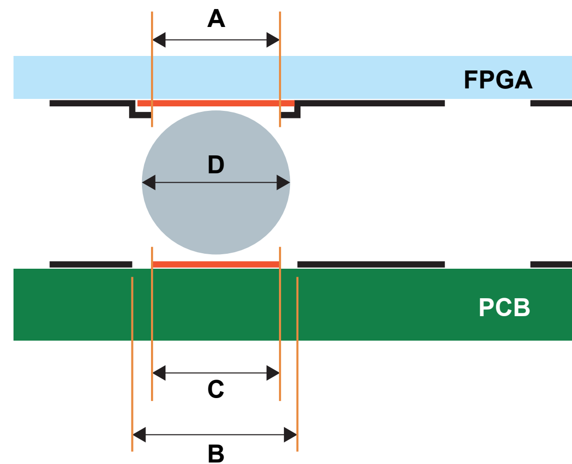
Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better "grip" area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball.

Figure 50: SMD and Non-SMD Pad Specification

Solder-Mask Defined



Non-Solder-Mask Defined



Legend:

A: BGA package solder mask opening
B: Optimum PCB solder mask opening
C: Optimum PCB pad size
D: Solder ball diameter

Table 12: PCB Solder Pad Recommendations

Package	Pitch (mm)	A BGA Package Solder Mask Opening (mm)	SMD		Non-SMD		D Solder Ball Diameter (mm)
			B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	
F49	0.4	0.2	0.2	0.275	0.3	0.2	0.25
W80	0.4	N.A.	0.175	0.225	0.25	0.175	0.2
F81	0.5	0.245	0.245	0.325	0.4	0.2	0.25
F169	0.65	0.25	0.25	0.35	0.4	0.2	0.25
F256	0.8	0.37	0.37	0.5	0.5	0.35	0.4
F324 (T20, T35	0.65	0.275	0.275	0.335	0.4	0.25	0.3
F324 (T55, T85, T120	0.65	0.275	0.275	0.38	0.4	0.25	0.3
F400	0.8	0.275	0.275	0.38	0.4	0.25	0.3
F484	0.8	0.35	0.35	0.45	0.5	0.35	0.4
F576	0.65	0.275	0.275	0.38	0.4	0.25	0.3

Routing between Pads on the Top Layer

You can route signal trace between solder pads on the top layer of the PCB while meeting the clearance requirement.

Figure 51: Routing Traces between Pads on the Top Layer

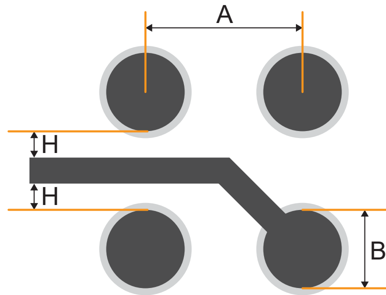


Table 13: Routing Measurements

Measure-ment	Description	Ball Count										Unit
		F49	W80	F81	F169	F256	F324 (T20, T35)	F324 (T55, T85, T120)	F400	F484	F576	
A	Ball pitch.	0.4	0.4	0.5	0.65	0.8	0.65	0.65	0.8	0.8	0.65	mm
	Ball ϕ.	0.25	0.2	0.25	0.25	0.4	0.3	0.3	0.3	0.4	0.3	mm
B	Width of the solder landing pad ϕ (SMD)	0.275	0.225	0.325	0.35	0.5	0.335	0.38	0.38	0.45	0.38	mm
	Width of the solder landing pad ϕ (NSMD)	0.2	0.175	0.2	0.2	0.35	0.25	0.25	0.25	0.35	0.25	mm
H (min.)	Minimum space between the trace and the landing pad (SMD)	[4]	[4]	0.05	0.08	0.08	0.1	0.08	0.1	0.1	0.08	mm
	Minimum space between the trace and the landing pad (NSMD)	[4]	[4]	0.08	0.1	0.1	0.1	0.1	0.1	0.1	0.1	mm

[4] The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an “offset via,” is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 52: Via Dimensions

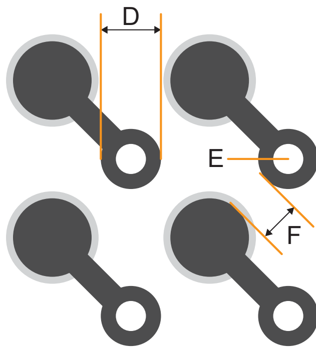


Table 14: Via Measurements

Measure-ment	Description	Ball Count										Unit
		F49	W80	F81	F169	F256	F324 (T20, T35)	F324 (T55, T85, T120)	F400	F484	F576	
D	Via capture pad width.	0.16	0.16	0.22	0.3	0.4	0.3	0.3	0.3	0.4	0.3	mm
E	Finished via ϕ.	0.1	0.1	0.13	0.15	0.25	0.15	0.2	0.2	0.25	0.2	mm
F (min.)	Space between the landing pad and via.	(5)	(5)	0.08	0.12	0.11	0.14	0.11	0.14	0.12	0.11	mm

(5) The via is under the pad, no traces between landing pads.

Routing through Different PCB Layers

You can route a trace between two solder pads at the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 53: BGA Trace Routing for Top and Second Layers

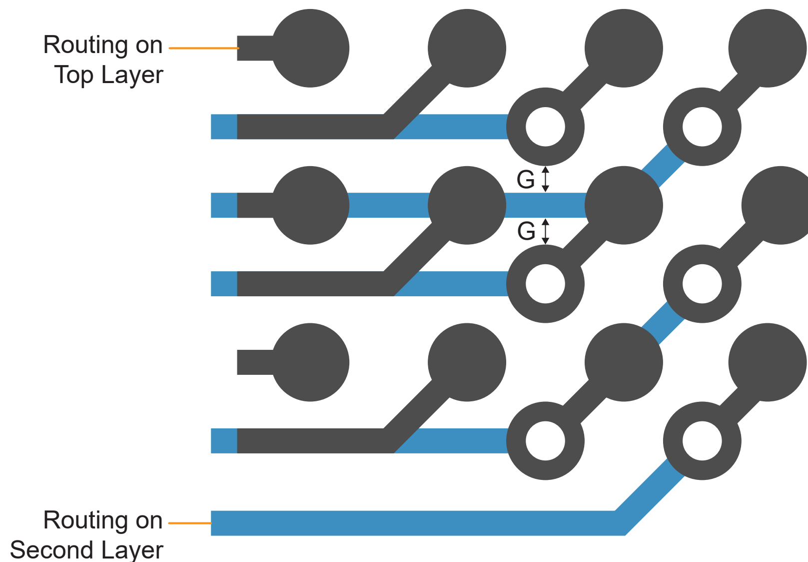


Table 15: Routing Measurements

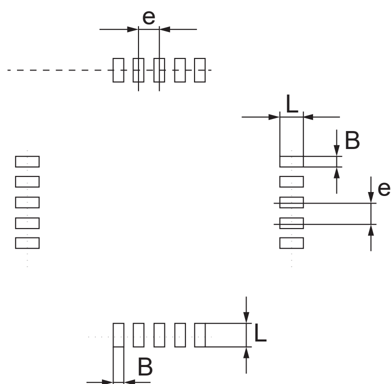
Measure-ment	Description	Ball Count										Unit
		F49	W80	F81	F169	F256	F324 (T20, T35)	F324 (T55, T85, T120)	F400	F484	F576	
G (min.)	Minimum space required between via trace and spacing.	0.08	0.08	0.085	0.01	0.1	0.1	0.1	0.1	0.1	0.1	mm

PCB Guidelines for QFP Packages

PCB Solder Pad (LQFP Packages)

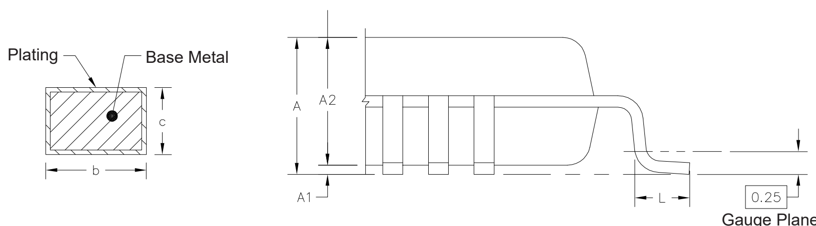
Elitestek provides LQFP lead dimension information. Use this data when creating your board layout so that the board pads match the landing pads.

Figure 54: Recommended PCB Landing Pad Guideline



Package	L	B	e
LQFP 144-pin	1.35 mm	0.29 mm	0.5 BSC
LQFP 100-pin	1.35 mm	0.29 mm	0.5 BSC

Figure 55: LQFP Lead Dimensions



	Symbol	Min	Nom	Max
Total thickness	A	–	–	1.6
Stand-off	A1	0.05	–	0.15
Mold thickness	A2	1.35	1.4	1.45
Lead width	b	0.17	0.22	0.27
L/F thickness	c	0.09	–	0.2
	L	0.45	0.6	0.75

Trion® FPGAs Solder Ball

Refer to the table for the recommended type of solder ball used for Trion® FPGAs:

Table 16: Trion® FPGAs Solder Ball

Device	Solder Ball Type
T4/T8F49	SAC105
T4/T8F81	SAC105
T13/T20F169	SAC105
T13/T20F256	SAC105 or SAC305
T20W80	SAC405
T20/T35F324	SAC1205
T20/T35F400	SAC1205
T55/T85/T120F324	SAC1205
T55/T85/T120F484	SAC 105
T55/T85/T120F576	SAC1205

Green Packaging

Elitestek FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. Elitestek refers to these products as "green" packaging.

Tape and Reel Packaging

Elitestek offers BGA and WLCSP devices in tape and reel packaging.

Table 17: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
FBGA49	12	9.3	8	13	5,000
	12	9.3	8	7	1,500
FBGA81	12	9.3	8	13	5,000
	12	9.3	8	7	1,500
WLCSP80	12	9.5	8	13	2,500

Figure 56: Pin 1 Location (BGA49 and BGA81 Packages)

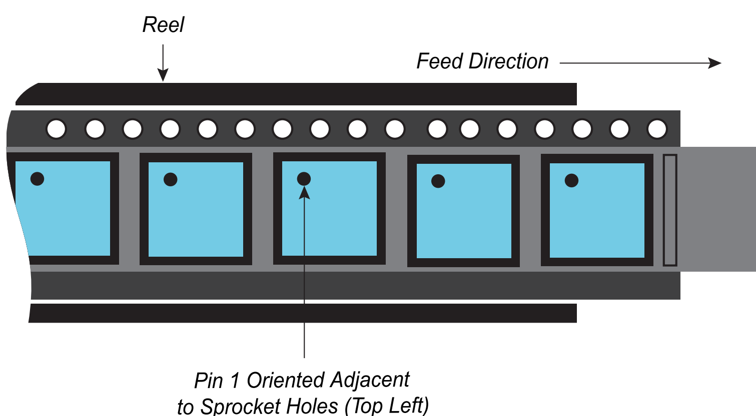
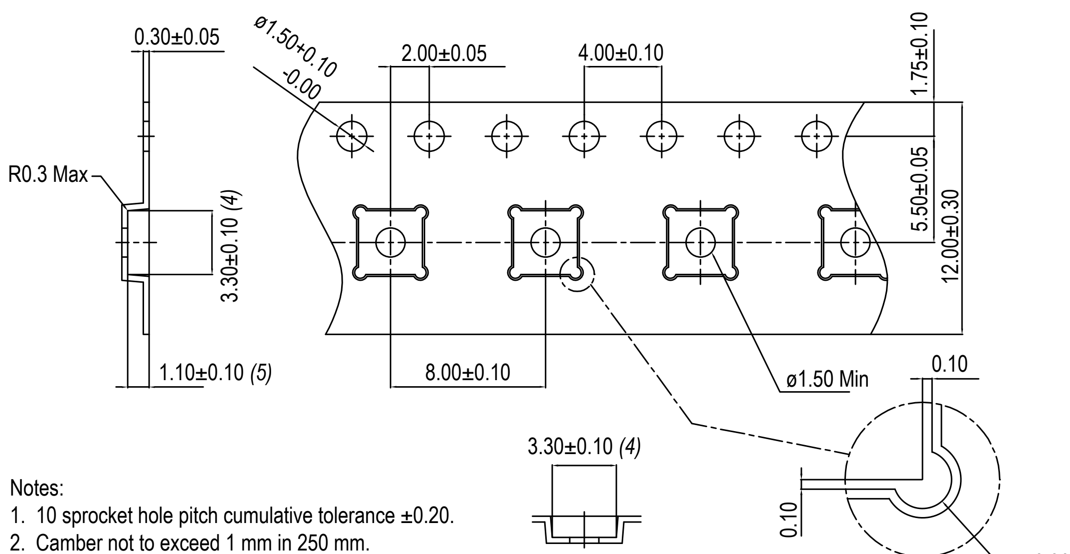
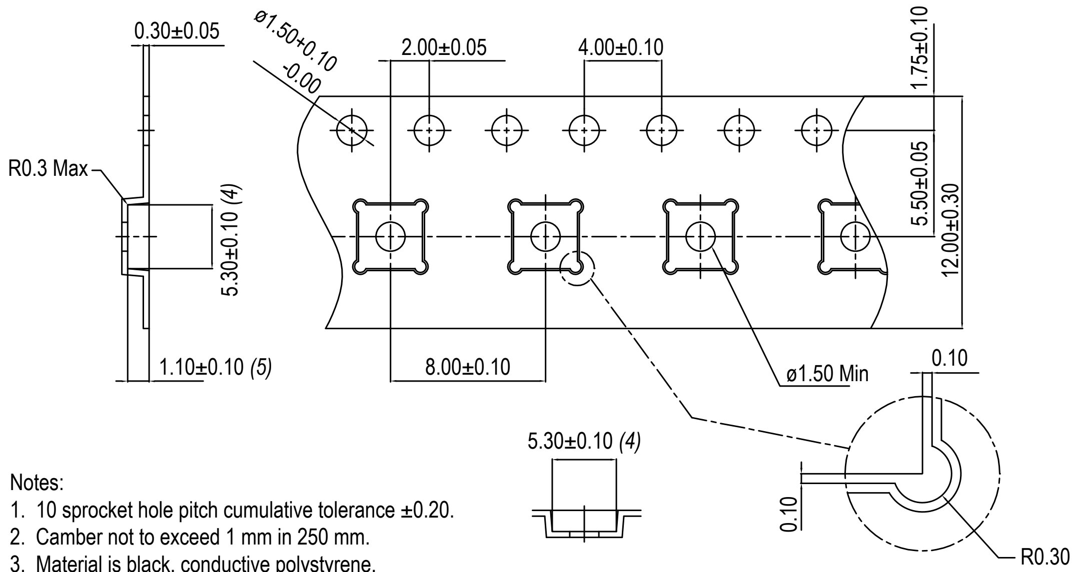


Figure 57: Tape Outline (BGA49 Packages)



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Camber not to exceed 1 mm in 250 mm.
3. Material is black, conductive polystyrene.
4. Measured on a plane 0.3 mm above the bottom of the pocket.
5. Measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be the same position.

Figure 58: Tape Outline (BGA81 Packages)



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Camber not to exceed 1 mm in 250 mm.
3. Material is black, conductive polystyrene.
4. Measured on a plane 0.3 mm above the bottom of the pocket.
5. Measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be the same position.

Figure 59: Pin 1 Location (WLCSP80 Packages)

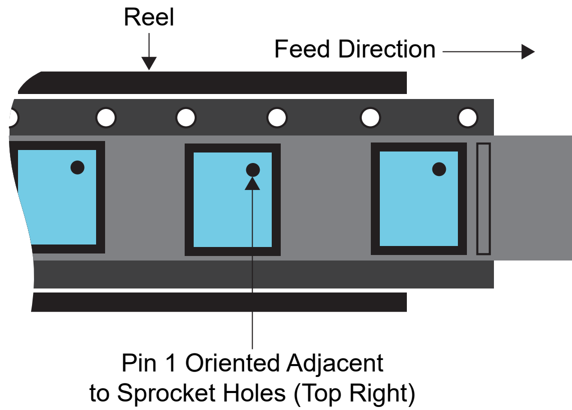
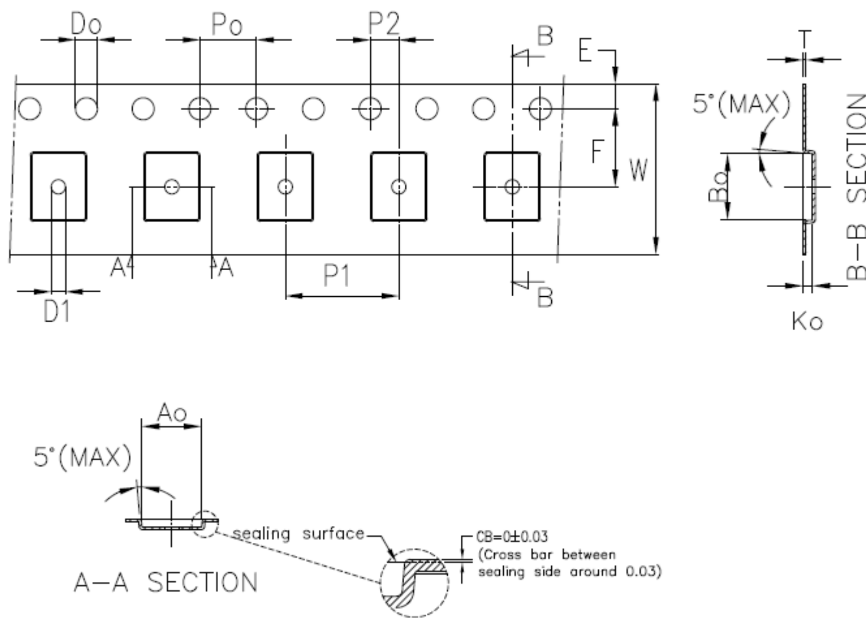


Figure 60: Tape Outline (WLCSP80 Packages)



Unit: mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.76±0.05	4.66±0.05	0.66±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	$1.50^{+0.10}_{-0}$	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity $\geq 1.0*10^5$ & $\leq 1.0*10^8$ ohm/sq.

Tray Packaging

Elitestek offers BGA and LQFP devices in tray packaging.

Table 18: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Minimum Quantity per Stack
FBGA256	119	7 x 17	10 + 1	1,190
FBGA169	260	10 x 26	10 + 1	2,600
LQFP100	90	6 x 15	10 + 1	900
LQFP144	60	12 x 5	10 + 1	600
FBGA324	168	21 x 8	10 + 1	1,680
FBGA400	84	14 x 6	10 + 1	840
FBGA484	84	14 x 6	10 + 1	840
FBGA576	84	14 x 6	10 + 1	840

Revision History

Table 19: Revision History

Date	Version	Description
February 2025	5.2	Fixed issue with wrong tables appearing in document. (DOC-2348)
December 2024	5.1	Changed co-planarity specification for T20 and T35 in F324 packages from 0.8 to 0.10 µm. (DOC-2281)
February 2024	5.0	Added in new section Trion® FPGAs Solder Ball. (DOC-1710) Updated pinout descriptions.
September 2023	4.9	Updated CCK pin description. (DOC-1451)
August 2023	4.8	Updated package outline for 49-Ball and 576-Ball FBGA Package Specifications. Added in package thickness of 1.07mm for 324-Ball Package Specifications. (ADV-2307-001) (DOC-1350)
June 2023	4.7	Updated Trion T13/T20 Q100F3. (DOC-1164)
February 2023	4.6	Corrected side view dimensions for F256 package. (DOC-813) Corrected routing and via dimensions for the F169 package. (DOC-804) Added 1,500 quantity tape and reel information for T4 and T8 FPGAs in BGA49 and BGA81 packages. Added PCB data for F400 packages. (DOC-928) Updated routing measurements. (DOC-928)
April 2022	4.5	Corrected typo for pin A9 in BGA400 package pinout and I/O banks. (DOC-784)
March 2022	4.4	Corrected typos for pins G6 and H15 in BGA400 package pinout and I/O banks. (DOC-756) Noted that BGA324, BGA400, and BGA576 are flip-chip packages. (DOC-756)
March 2022	4.3	Removed thermal pad from LQFP144 Recommended PCB Landing Pad Guideline; this package does not have a thermal pad. (DOC-751)
February 2022	4.2	Fixed typo in LQFP144 package pinout and I/O banks. Pin 31 was incorrectly marked as 34.
February 2022	4.1	Added recommended PCB landing pad guideline for LQFP packages. Corrected color coding for VCCIO4A in the BGA169 I/O bank diagram. (DOC-719) Correct the F (min.) via measurement for the BGA484 and BGA256 packages. (DOC-710)
December 2021	4.0	Fix incorrect pin names for T55/T85/T120 FPGAs in the BGA324 package. (DOC-671)
November 2021	3.9	Fixed incorrect color coding for I/O banks VCCIO_1F_1G in the BGA484 package. (DOC-639)
November 2021	3.8	Corrected symbols for pins L19 and R15 for the 400 BGA package. (DOC-564)
August 2021	3.7	Corrected pin numbering for the WLCSP80 package. (DOC-504) Corrected pitch for F576 in the PCB Solder Pad Recommendations table. (DOC-504) Updated PCB solder pad recommendations (DOC-504) Corrected pin A9 for F256 package pinout. (DOC-493)
July 2021	3.6	Rotated package outline, pinout, and I/O banks figures for the WLCSP80 to make it easier to identify pin 1.
June 2021	3.5	Added thermal resistance data for WLCSP80 package. (DOC-439) Added tape and reel information for WLCSP80. (DOC-439) Added peak reflow temperature for WLCSP80. Corrected typos in BGA256 pinout and fixed mislabeled banks in BGA256 I/O banks. (DOC-452)
December 2020	3.4	Added WLCSP80 package information.
August 2020	3.3	Updated routing measurements and via measurements.
July 2020	3.2	Corrected the BGA169 pinout.

Date	Version	Description
July 2020	3.1	Updated solder ball co-planarity limit from 0.1 to 0.15. Updated 81-ball FPGA package marking.
May 2020	3.0	Added guidelines for traces, pads, and vias for PCB design. Added BGA400 package information. Updated side view BGA576 package dimensions.
February 2020	2.1	Fixed typos in BGA576 pinout and I/O bank diagrams.
January 2020	2.0	Added BGA324, BGA484, and BGA576 package information.
October 2019	1.6	Added LQFP144 package information.
August 2019	1.5	Updated BGA169 and BGA256 package marking.
June 2019	1.4	Added 169 ball FBGA package information.
February 2019	1.3	Added Thermal resistance, solder pad dimensions, and peak reflow data for the 256 BGA package. Aded information on tray packaging. Clarified PLL ground pin in the 81 ball BGA diagram and pinout. Updated 256 ball FBGA package marking.
November 2018	1.2	Added 256 ball FBGA package information.
August 2018	1.1	Updated BGA81 pin figure.
July 2018	1.0	Initial release.