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T4 Data Sheet

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Contents

Introduction

The T4 FPGA features the high-density, low-power Elitestek® Quantum® architecture wrapped with an I/O interface in a small footprint package for easy integration. T4 FPGAs support mobile, consumer, and IoT edge markets that need low power, low cost, and a small form factor. With ultra-low power T4 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, and power management.

Features

- High-density, low-power Quantum® architecture
- Built on SMIC 40 nm process
- Less than 150 µA typical core leakage current at 1.1 V
- Ultra-small footprint package options
- FPGA interface blocks
  - GPIO
  - PLL
  - Oscillator
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces
- Flexible on-chip clocking
  - 12 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T4 FPGA Resources

LEs[1]	Global Clock Networks	Global Control Networks	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
3,888	Up to 16	Up to 8	76.8	15	4

[1] Logic capacity in equivalent LE counts.

Table 2: T4 FPGA Package-Dependent Resources

Resource	F49	F81
Available GPIO	33	55
Global clocks from GPIO pins	4	8
Global controls from GPIO pins	5	8
PLL (simple)	1	1
Oscillator	1	1
MPM	1 (optional)	1 (optional)

Learn more: Refer to the Trion Packaging User Guide for the package outlines and markings.

Available Package Options

Table 3: Available Packages

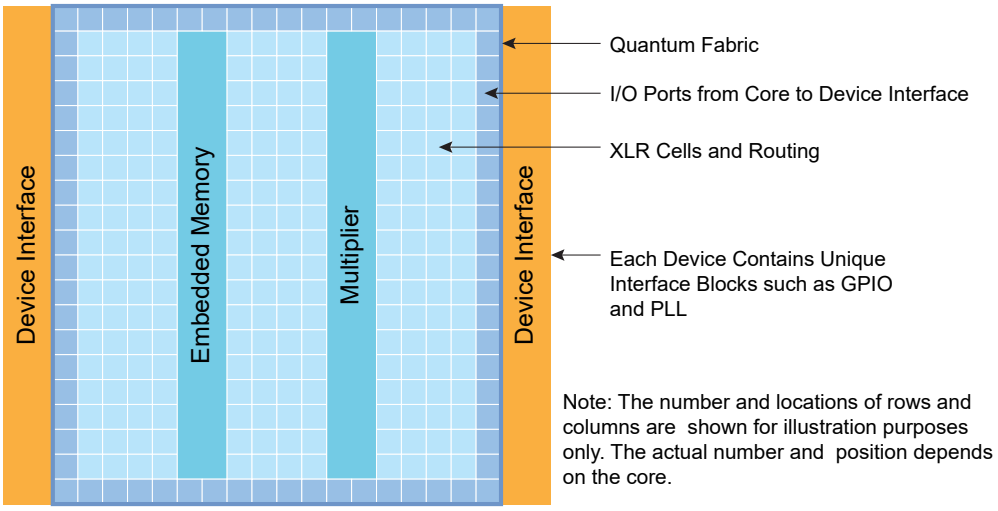
Package	Dimensions (mm x mm)	Pitch (mm)
49-ball FBGA[(2)]	3 x 3	0.4
81-ball FBGA	5 x 5	0.5

(2) This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

Device Core Functional Description

T4 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Elitestek has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: logic elements, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of XLR cells, memory, and multipliers. A control block within the FPGA handles configuration.

Figure 1: T4 FPGA Block Diagram



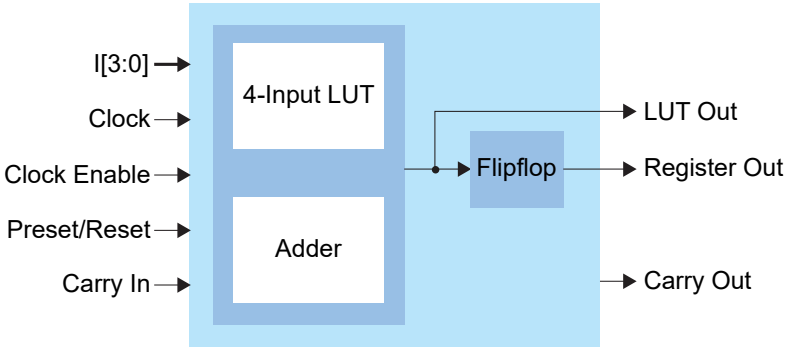
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum® architecture. The Elitestek XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The logic cell comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple logic cells to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Cell Block Diagram



Embedded Memory

The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

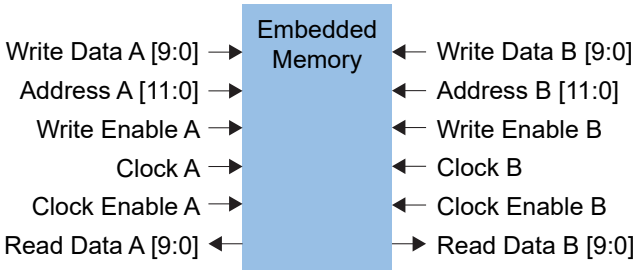
Note: The block RAM content is random and undefined if it is not initialized.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

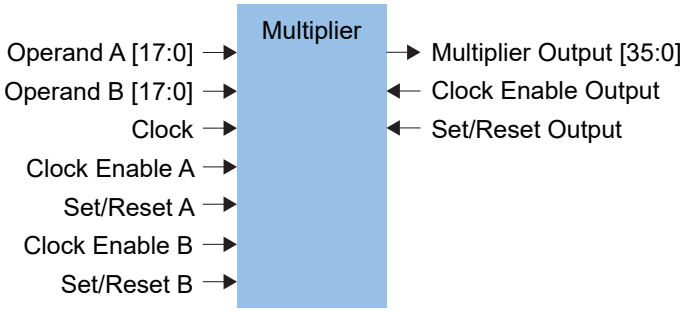
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram

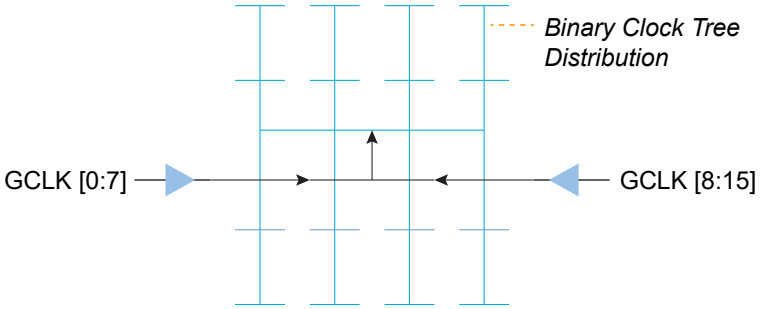


Global Clock Network

The Quantum® core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, oscillator output, and core-generated clocks can drive the global clock network.

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T4 global clock network using the global clock GPIO pins, PLL outputs, oscillator output, and core-generated clocks. Similarly, the T4 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the T4 for information on the location and names of these pins.

Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum® architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

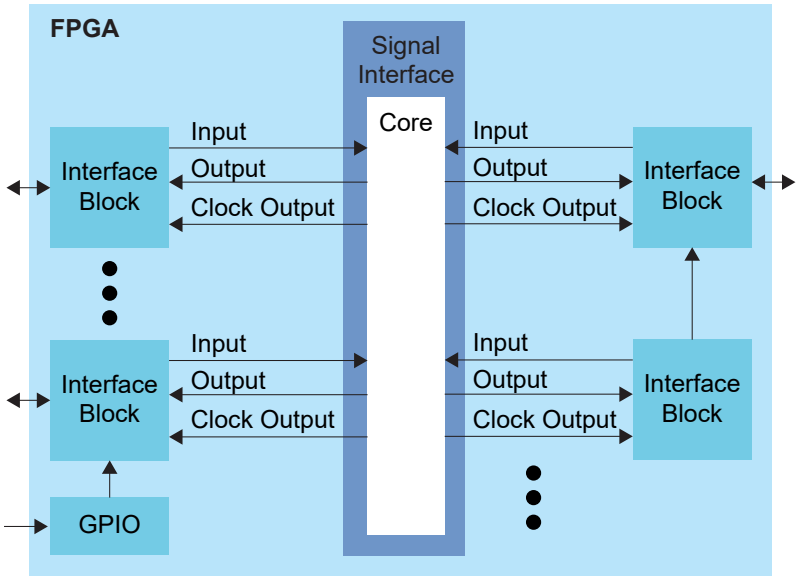
Learn more: The following sections describe the available device interface features in T4 FPGAs. Refer to the Trion® Interfaces User Guide for details on the Efinity® Interface Designer settings.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block.

The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration of the Efinity® Interface Designer.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the different types of interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 4: GPIO Modes

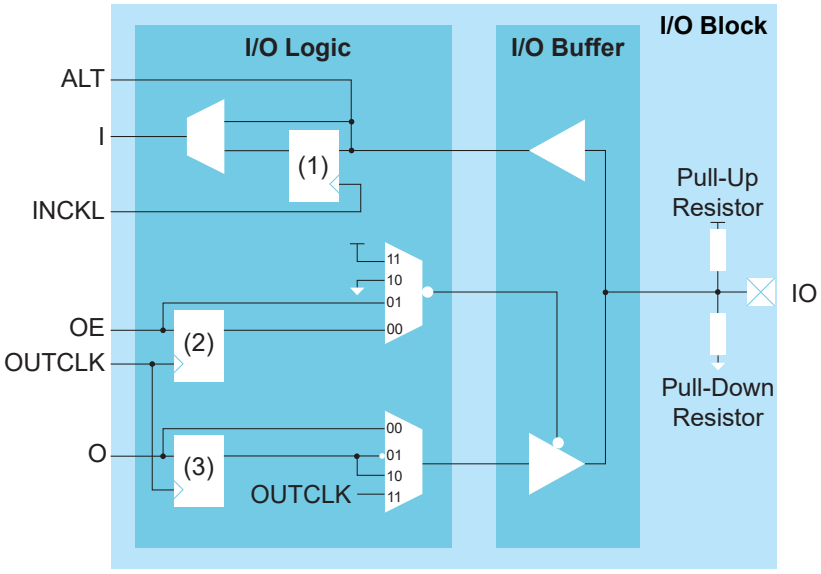
GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

Table 5: Supported Features for GPIO

Package	GPIO	LVDS as GPIO
F49 F81	Schmitt Trigger Variable Drive Strength Pull-up Pull-down Slew Rate	–

Simple I/O Buffer

Figure 7: I/O Interface Block



Notes:
1. Input Register
2. Output Enable Register
3. Output Register

Table 6: GPIO Signals

Signal	Direction	Description
I	Output	Input data from the GPIO pad to the core fabric.
ALT	Output	Alternative input connection (in the Interface Designer, the input **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLL_CLKIN.
O	Input	Output data to GPIO pad from the core fabric.
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE register. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input register. This clock is not visible in the user netlist.

Table 7: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

I/O Banks

Elitestek FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

Table 8: I/O Banks by Package

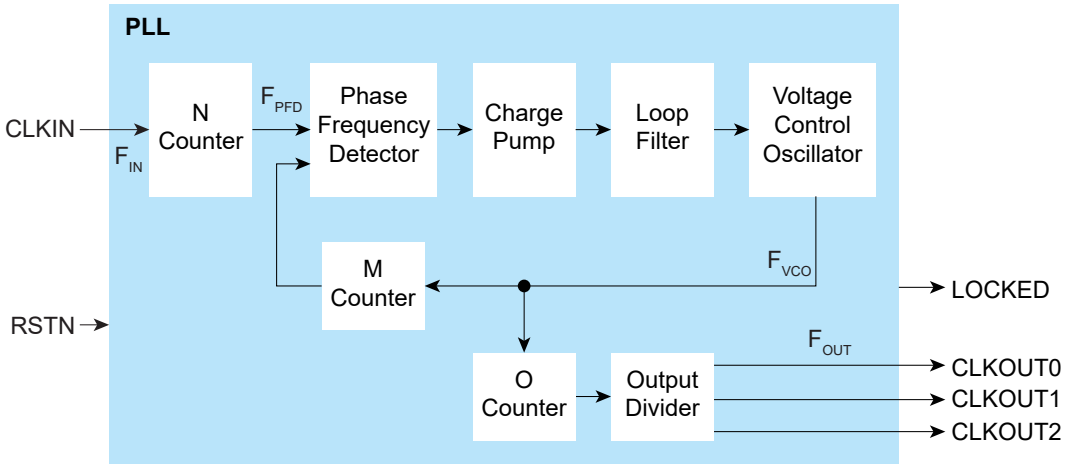
Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
F49, F81	1A - 1C, 2A, 2B	1.8, 2.5, 3.3	–	–

Learn more: Refer to the T4 for information on the I/O bank assignments.

PLL

The T4 has 1 PLL to synthesize clock frequencies. The PLL's reference clock input comes from a dedicated GPIO's alternate input pin. The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), post-divider counter (O counter), and an output divider per clock output.

Figure 8: T4 PLL Block Diagram



The counter settings define the PLL output frequency:	where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = F_{VCO} / (O \times \text{Output divider})$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency

Note: The reference clock must be between 10 and 50 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,200 MHz.

Unlike other Trion® FPGAs, the T4 PLL output locks on the *negative* clock edge (not the positive edge). When you are using two or more clock outputs, they are aligned on the falling edge. If the core register receiving the clock is positive edge triggered, Elitestek recommends inverting the clock outputs so they are correctly edge aligned.

Figure 9: PLL Output Aligned with Negative Edge

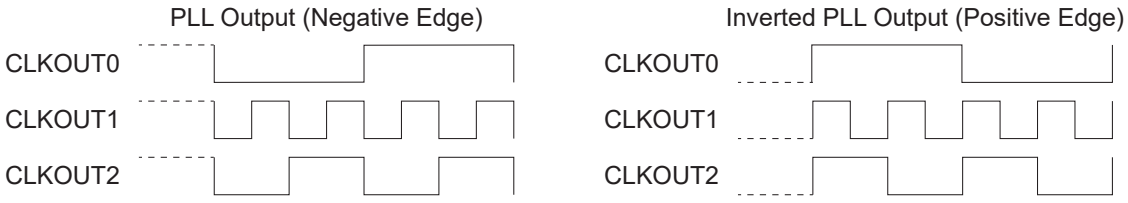


Table 9: PLL Pins

Port	Direction	Description
CLKIN	Input	Reference clock. This port is also a GPIO pin; the GPIO pins' alternate function is configured as a reference clock.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED[3]	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status. This signal is analog asynchronous.

Table 10: PLL Settings

Configure these settings in the Efinity® Interface Designer.

Setting	Allowed Values	Notes
N counter	1 - 15 (integer)	Pre-divider
M counter	1 - 255 (integer)	Multiplier
O counter	1, 2, 4, 8	Post-divider
Output divider	2, 4, 8, 16, 32, 64, 128, 256	Output divider per output

Oscillator

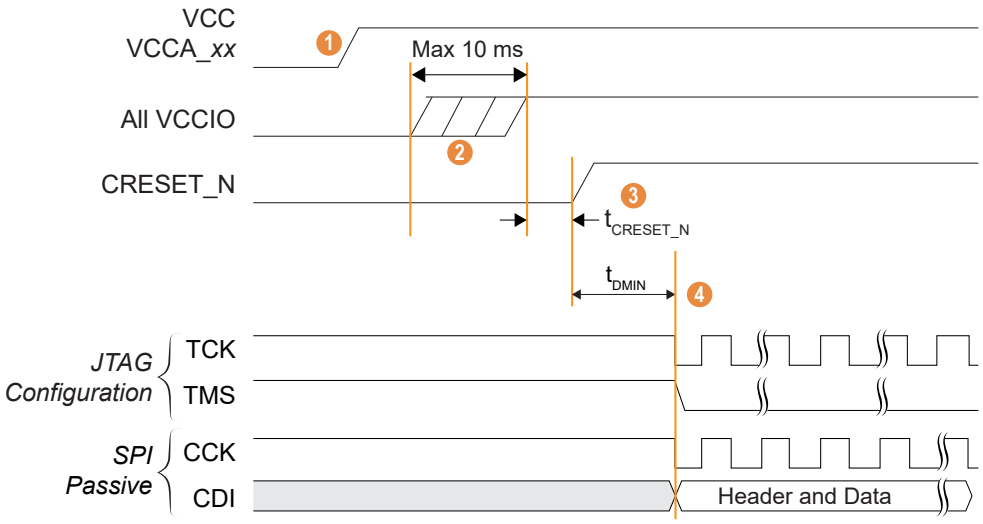
The T4 has 1 low-frequency oscillator tailored for low-power operation. The oscillator runs at nominal frequency of 10 kHz. Designers can use the oscillator to perform always-on functions with the lowest power possible. Its output clock is available to the GCLK network.

[3] The circuitry that generates the lock signal relies on a reference clock edge to transition the lock signal. A sudden removal of the reference clock will result in there being no positive clock edge with which to change the lock state from 1 back to 0. Therefore, the lock signal will remain on 1.

Power Up Sequence

Elitestek® recommends the following power up sequence when powering Trion® FPGAs:

Figure 10: Trion® FPGAs Power Up Sequence



1. Power up VCC and VCCA_xx first.
2. When VCC and VCCA_xx are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.

Important: Ensure the power ramp rate is within VCCIO/10 V/ms to 10 V/ms.

3. After all power supplies are stable, hold CRESET_N low for a duration of t_{CRESET_N} before asserting CRESET_N from low to high to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).
4. FPGA configuration can begin after there has been a t_{DMIN} minimum delay after CRESET_N goes high (see **SPI Passive** on page 24 and **JTAG** on page 25 for the delay specification).

When you are not using the GPIO or PLL resources, connect the pins as shown in the following table.

Note: Refer to **Configuration Timing** on page 22 for timing information.

Power Supply Current Transient

You may observe an inrush current on the dedicated power rail during power-up. You must ensure that the power supplies selected in your board meets the current requirement during power-up and the estimated current during user mode. Use the Power Estimator to calculate the estimated current during user mode.

Table 11: Maximum Power Supply Current Transient

Power Supply	Maximum Power Supply Current Transient[4][5]	Unit
VCC	18	mA

[4] Inrush current for other power rails are not significant in Trion® FPGAs.
[5] Measured at room temperature.

Unused Resources and Features

Table 12: Connection Requirements for Unused Resources

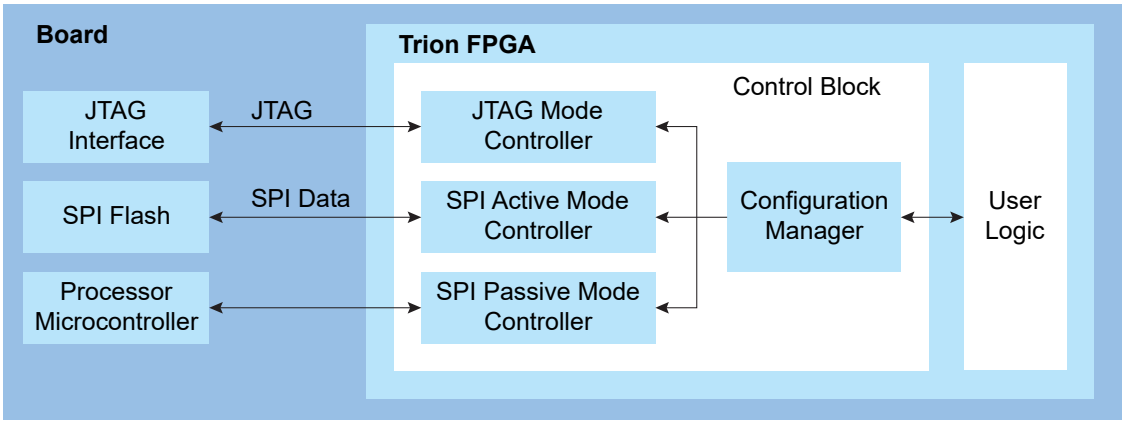
Unused Resource	Pin	Note
GPIO Bank	VCCIOxx	Connect to either 1.8 V, 2.5 V, or 3.3 V.
PLL	VCCA_PLL	Connect to VCC (1.2 V).

Configuration

The T4 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T4 FPGA(s) in SPI active, SPI passive, or JTAG mode.

Learn more: Refer to AN 006: Configuring Trion FPGAs for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 11: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 µs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 13: T4 Configuration Modes by Package

Configuration Mode	Width	F49	F81
Active	X1	✓	✓
	X2	✓	✓
	X4	✓	✓
Passive	X1	✓	✓
	X2	✓	✓
	X4	✓	✓
	X8	✓	✓
JTAG	X1		✓

Mask-Programmable Memory Option

The T4 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

DC and Switching Characteristics

Table 14: Absolute Maximum Ratings [6]

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
V_{IN}	I/O input voltage	-0.5	4.6	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.[7]	–	10	mA
T_J	Operating junction temperature	-40	125	°C
T_{STG}	Storage temperature, ambient	-55	150	°C

Table 15: Recommended Operating Conditions [6]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
V_{IN}	I/O input voltage[8]	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

Table 16: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	VCCIO/10	10	V/ms

Table 17: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

[6] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
[7] Should not exceed a total of 120 mA per bank.
[8] Values applicable to both input and tri-stated output configuration.

Table 18: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic

Voltage	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 19: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

CDONE has a drive strength of 1.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	5.1	4.4
2	19.1	10.5	12.2	10.5	6.8	5.8
3	23.9	13.3	15.2	13.4	8.6	7.3
4	28.7	15.8	18.2	15.9	10.3	8.6

Table 20: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

I/O Standard	Internal Pull-Up			Internal Pull-Down			Units
	Min	Typ	Max	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	30	47	83	kΩ
2.5 V LVCMOS	35	55	120	37	62	118	kΩ
1.8 V LVCMOS	70	90	200	80	99	300	kΩ

Table 21: Single-Ended I/O Rise and Fall Time

Data are based on the following IBIS simulation setup:

- Weakest drive strength model
- Typical simulation corner setting
- RLC circuit with 6.6 pF capacitance, 16.6 nH inductance, 0.095 ohm resistance, and 25 °C temperature

Note: For a more accurate data, you need to perform the simulation with your own circuit.

I/O Standard	Rise Time (T_R)		Fall Time (T_F)		Units
	Slow Slew Rate Enabled	Slow Slew Rate Disabled	Slow Slew Rate Enabled	Slow Slew Rate Disabled	
3.3 V LVTTL/LVCMOS	1.13	1.02	1.24	1.17	ns
2.5 V LVCMOS	1.4	1.3	1.44	1.31	ns
1.8 V LVCMOS	2.14	2.01	2.05	1.85	ns

Table 22: Maximum Toggle Rate

Elitestek recommends that you perform simulations using the IBIS model to determine the maximum toggle rate for your design.

I/O Standard	Max Toggle Rate	Units
3.3 V LVTTL/LVCMOS	400	Mbps
2.5 V LVCMOS	400	Mbps
1.8 V LVCMOS	400	Mbps

Table 23: Block RAM Characteristics

Symbol	Description	C2, I2 Speed Grade	Units
f_{MAX}	Block RAM maximum frequency.	275	MHz

Table 24: Multiplier Block Characteristics

Symbol	Description	C2, I2 Speed Grade	Units
f_{MAX}	Multiplier block maximum frequency.	275	MHz

ESD Performance

Refer to the Trion Reliability Report for ESD performance data.

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 25: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz
F_{OUT}	Output clock frequency.	0.25	–	400	MHz
F_{VCO}	PLL VCO frequency.	500	–	1200	MHz

Table 26: PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	40	50	60	%
t_{OPJIT} (PK - PK)	Output clock period jitter (PK-PK).	–	100	–	ps
t_{INDT}	Input clock duty cycle.	45	–	55	%
t_{ILJIT} (PK - PK)	Input clock long-term jitter (PK-PK)	–	–	800	ps
t_{LOCK}	PLL pull in plus lock-in time.	–	–	0.5	ms

Internal Oscillator

The internal oscillator has the following specifications.

Table 27: Internal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
F_{CLKOSC}	Oscillator clock frequency.	–	10	–	kHz
D_{CHOSC}	Duty cycle.	45	50	55	%

Configuration Timing

The T4 FPGA has the following configuration timing specifications. Refer to AN 006: Configuring Trion FPGAs for detailed configuration information.

Table 28: Timing Parameters for All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[9][10] Test condition at 10 kΩ pull-up resistance and 10 pF output loading on CDONE pin.	12	–	[11]	µs

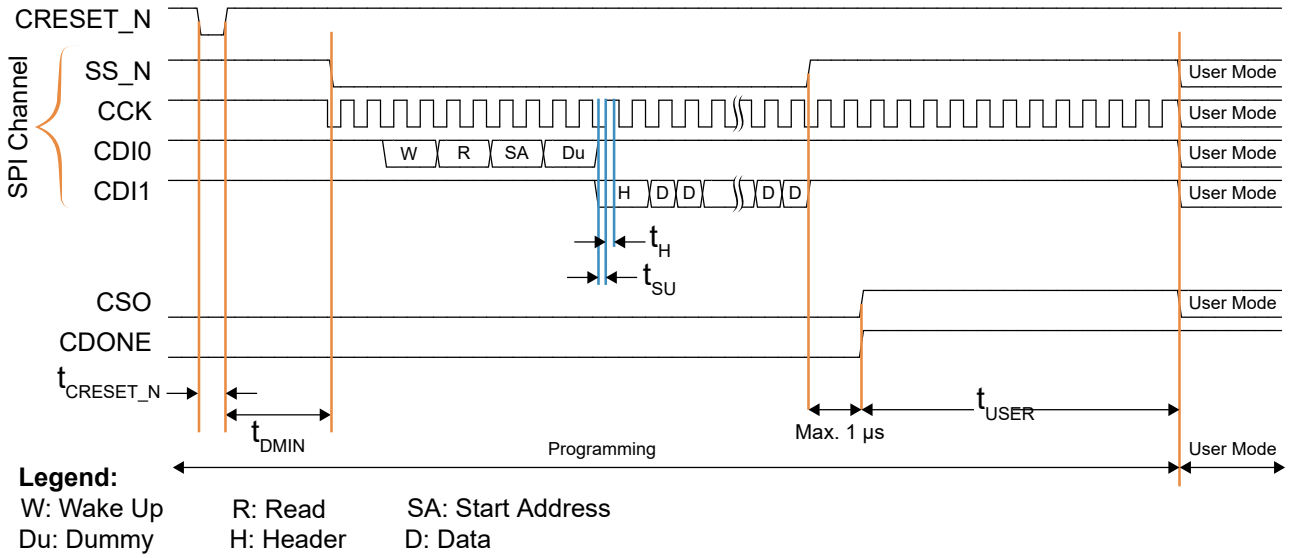
[9] The FPGA may go into user mode before t_{USER} has elapsed. However, Elitestek recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

[10] For JTAG programming, the min t_{USER} configuration time is required after CDONE goes high and FPGA receives the ENTERUSER instruction from JTAG host (TAP controller in UPDATE_IR state).

[11] See **Maximum tUSER for SPI Active and Passive Modes** on page 25

SPI Active

Figure 12: SPI Active Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI active configuration.

Table 29: Active Mode Timing Parameters

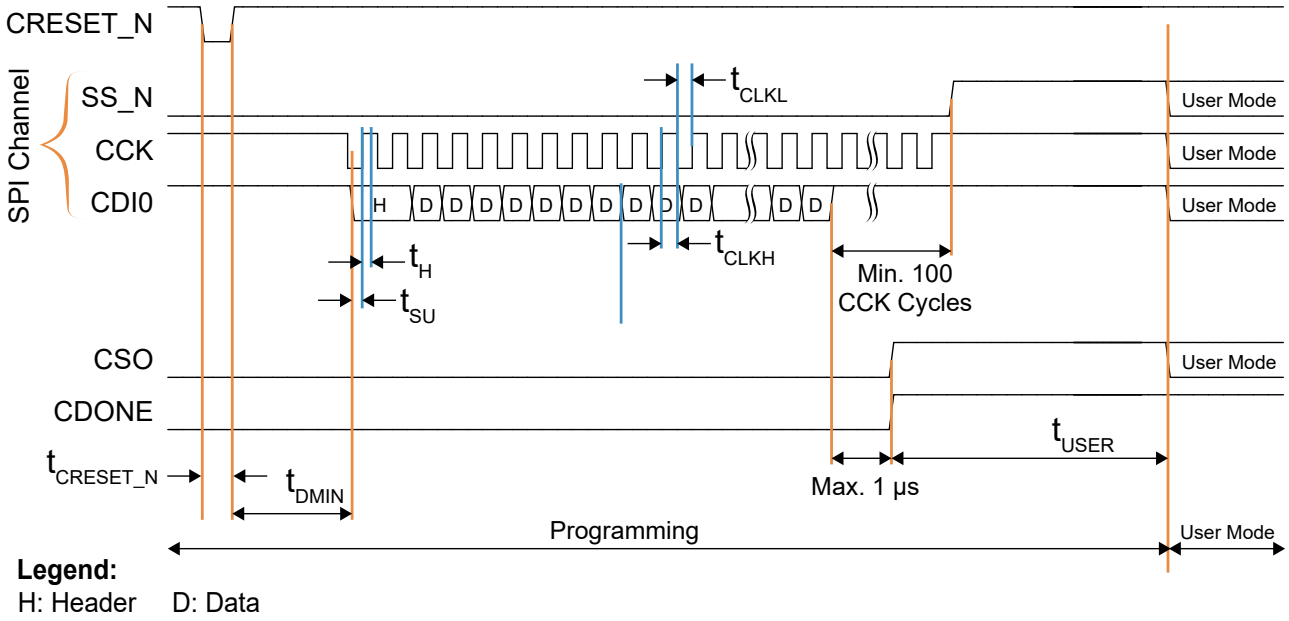
Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency[12].	DIV4	14	20	26	MHz
		DIV8	7	10	13	MHz
t_{SU}	Setup time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	7.5	–	–	ns
t_H	Hold time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	–	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 14 for details on the power-up requirements.

[12] For parallel daisy chain x2 and x4, the active configuration clock frequency, fMAX_M, must be set to DIV4.

SPI Passive

Figure 13: SPI Passive Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI passive configuration.

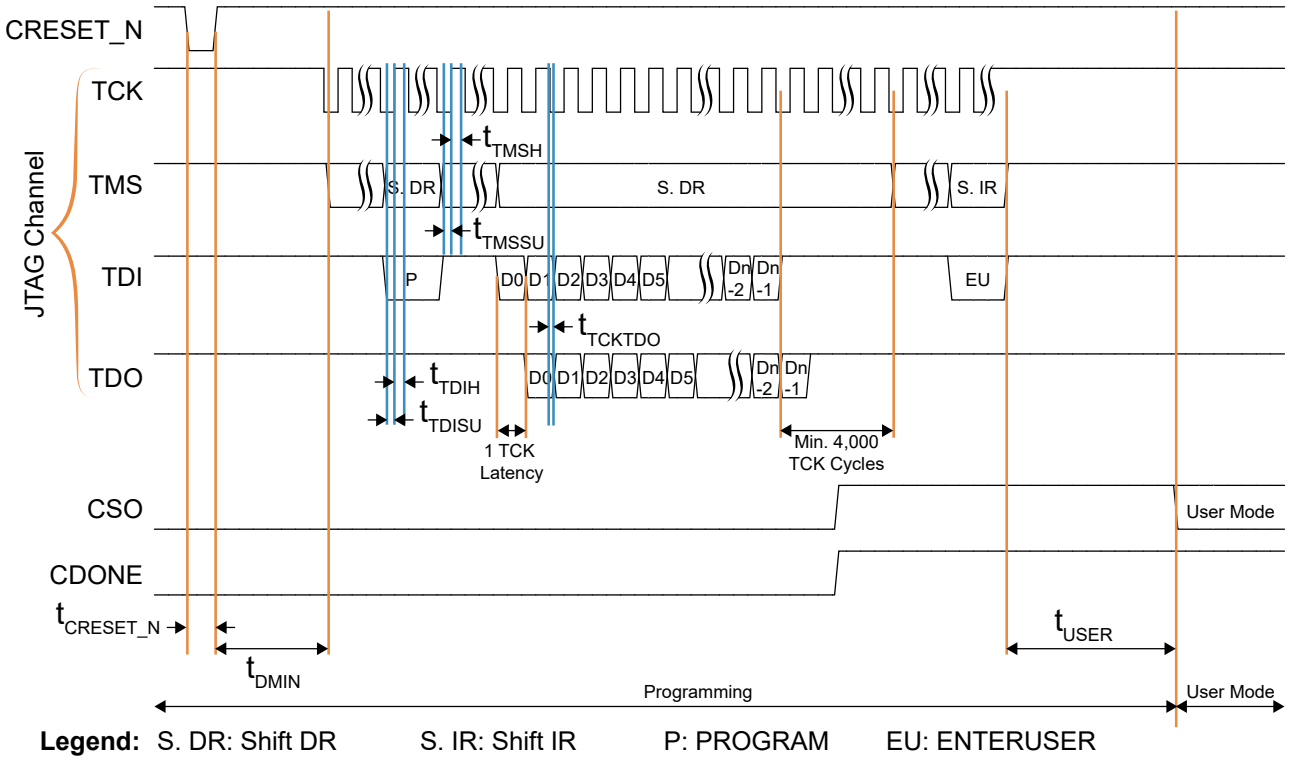
Table 30: Passive Mode Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode X1 configuration clock frequency.	–	–	25	MHz
	Passive mode X2, X4 or X8 configuration clock frequency.	–	–	50	MHz
t_{CLKH}	Configuration clock pulse width high.	0.48*1/ f_{MAX_S}	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	0.48*1/ f_{MAX_S}	–	–	ns
t_{SU}	Setup time.	4	–	–	ns
t_H	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 14 for details on the power-up requirements.

JTAG

Figure 14: JTAG Programming Waveform



Legend: S. DR: Shift DR S. IR: Shift IR P: PROGRAM EU: ENTERUSER

The SPI bus must be inactive during JTAG configuration.

Important: Refer to **Power Up Sequence** on page 14 for power-up details.

Table 31: JTAG Mode Timing Parameters

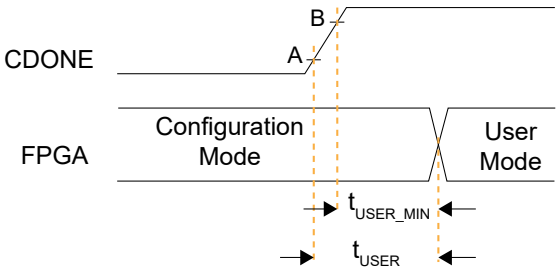
Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	25	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1	–	–	ns
t_{TMSSU}	TMS setup time.	3	–	–	ns
t_{TMSH}	TMS hold time.	1	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[13]	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 14 for details on the power-up requirements.

Maximum t_{USER} for SPI Active and Passive Modes

The following waveform illustrates the minimum and maximum values for t_{USER}.

[13] 0 pf output loading.



- *Point A*—User-defined trigger point to start counter on t_{USER}
- *Point B*—V_{IH} (with Schmitt Trigger) of Trion I/Os

The maximum t_{USER} value can be derived based on the following formula:

Table 32: t_{USER} Maximum

Configuration Setup	t_{USER} Maximum
Single Trion FPGA	$t_{USER} = t_{(from\ A\ to\ B)} + t_{USER\_MIN}$
Slave FPGA in a dual-Trion FPGA SPI chain	
Master FPGA in a dual-Trion FPGA SPI chain	t_{USER} = (1344 / SPI_WIDTH) * CCK period + t_{USER_MIN} + $t_{(from\ A\ to\ B)}$

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 33: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCA_PLL	Power	–	PLL analog power supply.
VCCIO	Power	–	I/O pin power supply.
GND	Ground	–	Ground.
GNDA_PLL	Ground	–	PLL ground pin.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock.
MREFCLK	Alternate	Input	MIPI TX PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single-ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: Indicates the bank; left (L) or right (R). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function.

Table 34: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration except for `TCK` and `TDO`.

Pins	Direction	Description	External Weak Pull- Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

Note: All dedicated configuration pins have Schmitt Trigger buffer. See **Table 18: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic** on page 19 for the Schmitt Trigger buffer specifications.

Table 35: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. CBUS has an internal weak pull-up. However, Elitestek recommends that you use an external pull-up accordingly. See *Selecting the Configuration Mode* in AN 006: Configuring Trion FPGAs	Pull up or pull down[14]
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	Pull up or pull down [15]
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	Optional[16]
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI (31:0) connects to the data bus in parallel.	Optional[16]
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for all configuration modes. CSI must remain high throughout all configuration modes.	Pull up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Logic low indicates a configuration error due to ID mismatch.	N/A
SS_N	Input	SPI configuration mode select. The FPGA senses the value of SS_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: SPI Passive mode; connect to external weak pull down. 1: SPI Active mode; connect to external weak pull up. In active configuration mode, SS_N is an active-low chip select to the flash device (CDI0 - CDI3).	Optional[16]
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. F49 and F81 packages only.	N/A

(14) Optional for x1 mode.
(15) Not applicable to single-image or remote update.
(16) Optional unless pull-up is required by external load.

Pin States

GPIO pins have as internal pull up/down (see **Figure 7: I/O Interface Block** on page 10). The following table shows the pin state during reset, configuration, and when unused in user mode.

Table 36: I/O Pin States

Pin Type	During Reset (CRESET_N Low)	During Configuration (CRESET_N High, CDONE Low)	When Unused in User Mode (Default)
User Pins			
GPIO	Input tri-state with weak pull up.	Input tri-state with weak pull up.	Input tri-state with weak pull up.[17]
LVDS used as GPIO	Input tri-state with no weak pull up or pull down.	Input tri-state with no weak pull up or pull down.	Input tri-state with weak pull up.
Dual-Purpose Configuration Pins			
CSO	0	0[18]	Input tri-state with weak pull up.
NSTATUS	1	1[19]	Input tri-state with weak pull up.
CCK	Input tri-state with weak pull up.	SPI active output clock. SPI passive input with weak pull up.	Input tri-state with weak pull up.
CDI0	Input tri-state with weak pull up.	SPI active output. SPI passive input with weak pull up.	Input tri-state with weak pull up.

As shown in **Power Up Sequence** on page 14, `CRESET_N` must be kept low during power up.

Note: Refer to the following tables for details:
Table 20: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance on page 19

Efinity Software Support

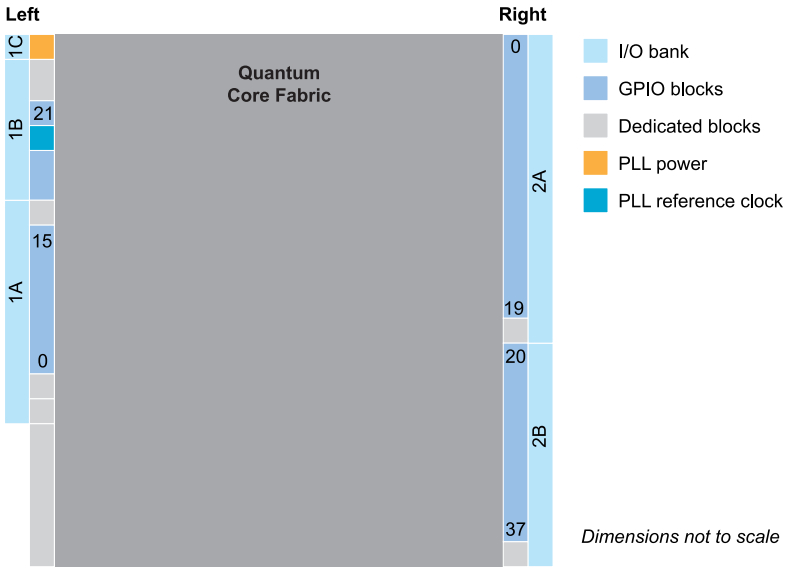
The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The Efinity® software supports simulation flows using the ModelSim, NCSim, or free iVerilog simulators. An integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores helps you probe signals in your design. The software-generated bitstream file configures the T4 FPGA. The software supports the Verilog HDL, SystemVerilog, and VHDL languages.

T4 Interface Floorplan

Note: The numbers in the floorplan figures indicate the GPIO number ranges. Some packages may not have all GPIO pins in the range bonded out. Refer to the T4 pinout for information on which pins are available in each package.

(17) You can change it to weak pull-down in the Interface Designer.
(18) CSO is driven to 1 when the bitstream is done transmitting (CDONE = 1).
(19) NSTATUS is driven to 0 if the FPGA detects an incorrect JTAG ID.

Figure 15: Floorplan Diagram for F49 and F81 Packages



Ordering Codes

Refer to the Trion Selector Guide for the full listing of T4 ordering codes.

Revision History

Table 37: Revision History

Date	Version	Description
April 2025	3.10	Fixed typo in **Table 29: Active Mode Timing Parameters** on page 23. (DOC-2500)
April 2025	3.9	Updated LVDS used as GPIO state in Pin States topic. Updated configuration timing waveforms. (DOC-2325) Moved information about unused resources to **Unused Resources and Features** on page 15.
November 2024	3.8	Updated GPIO interface pin names (IN to I and OUT to O). (DOC-2086) Fixed typo in **Table 35: Dual-Purpose Configuration Pins** on page 28. (DOC-2038) Footnote added to **Table 9: PLL Pins** on page 13. (DOC-1939) Added Pin States topic. (DOC-2087) SPI and JTAG pins should not be active at the same time for configuration. (DOC-2046) Renamed package prefix to match Efinity software (e.g., BGA changesd to F).
February 2024	3.7	Updated SPI passive timing waveform. Added note about external DC-biased circuit is required if the incoming LVDS signals are AC-coupled and link to Trion Hardware Design Checklist and Guidelines. (DOC-1532)
October 2023	3.6	Updated Maximum Toggle Rate table by adding recommendation to run simulation for actual toggle rate. (DOC-1468) Updated 2.5 V and 1.8 LVCMOS Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance. (DOC-1476)
February 2023	3.5	Updated power up sequence diagram. (DOC-954)
April 2022	3.4	Updated test condition load to maximum load in Maximum Toggle Rate Table. (DOC-781)
March 2022	3.3	Updated supported maximum VCO frequency to 1,200 MHz. (DOC-722) Updated behaviour description for unused GPIO pins during user mode. (DOC-720) Added note about the block RAM content is random and undefined if it is not initialized. (DOC-729) Updated power supply ramp rate and power up sequence diagram. (DOC-631)
January 2022	3.2	Corrected power supply ramp rate. (DOC-699)
January 2022	3.1	Added maximum I/O pin input current, I_{IN}, and maximum per bank specs. (DOC-652) Added PLL input clock duty cycle, t_{INDT}, specs. (DOC-661) Updated CDONE pin direction as bidirectional. (DOC-672)
November 2021	3.0	Added storage temperature, T_{STG} spec. (DOC-560) Updated maximum JTAG mode TCK frequency, f_{TCK}. (DOC-574) Updated CSI pin description. (DOC-546) Updated t_{CLKH} and t_{CLKL}, and corrected SPI Passive Mode (x1) Timing Sequence waveform. (DOC-590) Updated minimum Power Supply Ramp Rates. (DOC-631) Updated Maximum Toggle Rate table. (DOC-630)
September 2021	2.10	Added Single-Ended I/O Rise and Fall Time specs. (DOC-522) Added note to Active mode configuration clock frequency stating that for parallel daisy chain x2 and x4 configuration, f_{MAX_M}, must be set to DIV4. (DOC-528) Added Maximum t_{USER} for SPI Active and Passive Modes topic. (DOC-535)
August 2021	2.9	Removed Static Supply Current parameter. (DOC-456) Added internal weak pull-up and pull-down resistor specs. (DOC-485) Added note in Pinout Description stating all dedicated configuration pins have Schmitt Trigger buffer. (DOC-507) Updated table title for Single-Ended I/O Schmitt Trigger Buffer Characteristic. (DOC-507)
June 2021	2.8	Updated CRESET_N pin description. (DOC-450)
April 2021	2.7	Updated PLL specs; t_{ILJIT} (PK - PK) and t_{DT}. (DOC-403)

Date	Version	Description
March 2021	2.6	The simple PLL output is negative edge aligned. (DOC-400)
February 2021	2.5	Added I/O input voltage, V_{IN} specification. (DOC-389)
December 2020	2.4	Updated NSTATUS pin description. (DOC-335) Added a table to Power Up Sequence topic describing pin connection when PLL or GPIO is not used. (DOC-325) Updated f_{MAX_S} for passive configuration modes. (DOC-350)
September 2020	2.3	Updated pinout links.
August 2020	2.2	Removed typical standby (low power [LP] option) from static supply current table and updated typical standby value. Updated t_{USER} timing parameter values and added a note about the conditions for the values. Updated description for GPIO pins state during configuration. Added operating junction temperature for industrial speed grade. Updated block RAM and multiplier block maximum frequencies to include I2 speed grade. Added maximum power supply current transient during power-up.
July 2020	2.1	Updated the term DSP to multiplier. Updated timing parameter symbols in boundary scan timing waveform to reflect JTAG mode parameter symbols. Added supported GPIO features. Updated power up sequence description about holding CRESET_N low. Updated PLLCLK pin name to PLL_CLKIN.
February 2020	2.0	Added f_{MAX} for DSP blocks and RAM blocks. Added Trion power-up sequence. Updated number of global clocks and controls that can come from GPIO pins in package resources table.
December 2019	1.9	Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported.
October 2019	1.8	Added waveforms for configuration timing.
August 2019	1.7	Removed ESD table and added link to Trion Reliability Report. Minor formatting changes.
February 2019	1.6	Removed incorrect footnote about LVDS under Available Package Options.
November 2018	1.5	Updated PLL interface description. Added floorplan information. Updated configuraiton timing and PLL timing information.
August 2018	1.4	Updated configuration pin table. Renamed RST PLL pin as RSTN.
August 2018	1.3	Updated standby current specifications. Updated ordering codes.
July 2018	1.2	• Updated the PLL timing specification to add F_{PFD}. • Clarified the slew rate description.
May 2018	1.1	Added ordering code information.
April 2018	1.0	Initial release.